

Important notice

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Kind regards,

Team Nexperia

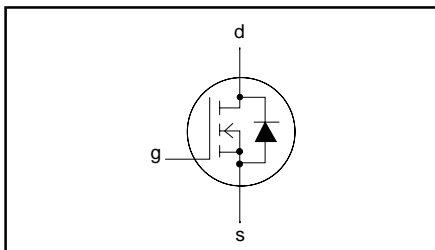
N-channel TrenchMOS™ transistor

PHT6NQ10T

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 100\text{ V}$
$I_D = 6.5\text{ A}$
$R_{DS(ON)} \leq 90\text{ m}\Omega$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect transistor in a plastic envelope using 'trench' technology.

Applications:-

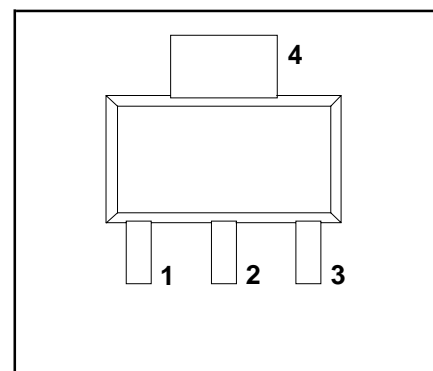
- Motor and relay drivers
- d.c. to d.c. converters

The PHT6NQ10T is supplied in the SOT223 surface mounting package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

SOT223



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	-	100	V
V_{DGR}	Drain-gate voltage	$T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current (dc)	$T_{sp} = 25\text{ }^\circ\text{C}$ $T_{amb} = 25\text{ }^\circ\text{C}$	-	6.5	A
I_D	Continuous drain current (dc)	$T_{sp} = 100\text{ }^\circ\text{C}$ $T_{amb} = 100\text{ }^\circ\text{C}$	-	3	A
I_{DM}	Pulsed drain current		-	4.1	A
P_D	Total power dissipation		-	1.9	A
T_j, T_{stg}	Operating junction and storage temperature		-	26	A
		$T_{sp} = 25\text{ }^\circ\text{C}$ $T_{amb} = 25\text{ }^\circ\text{C}$	-	8.3	W
			-	1.8	W
			-65	150	$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance junction to solder point	surface mounted, FR4 board	12	15	K/W
$R_{th\ j-amb}$	Thermal resistance junction to ambient	surface mounted, FR4 board	70	-	K/W

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ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

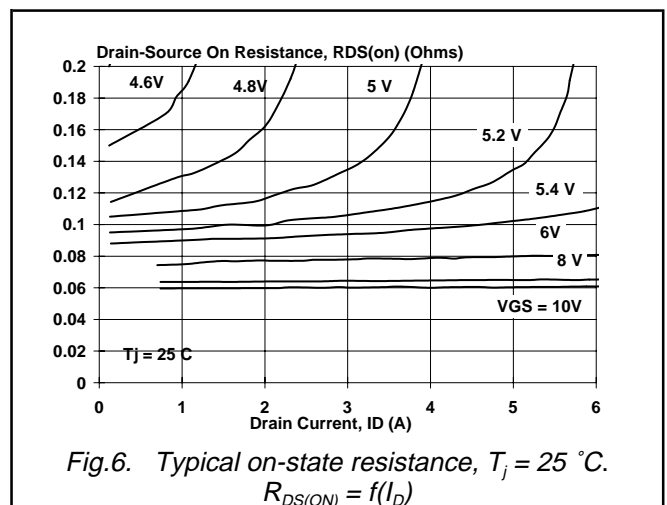
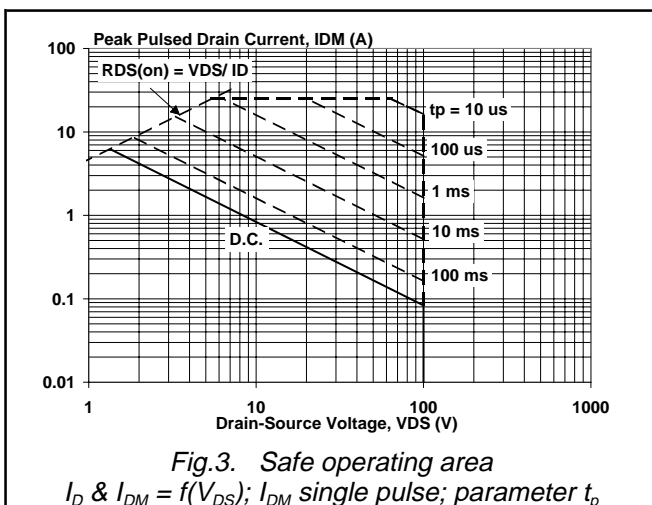
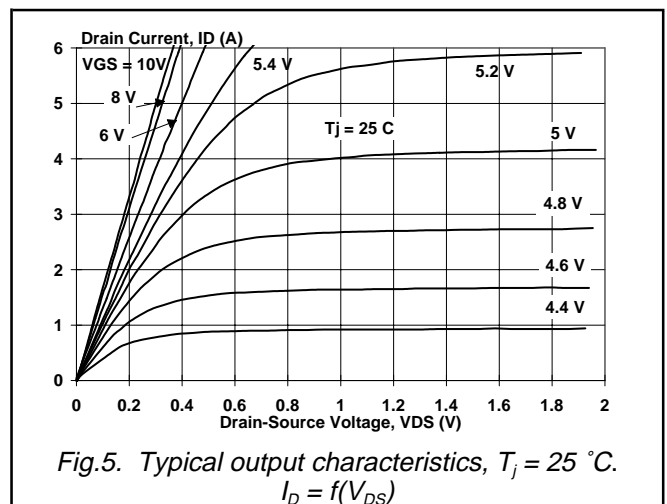
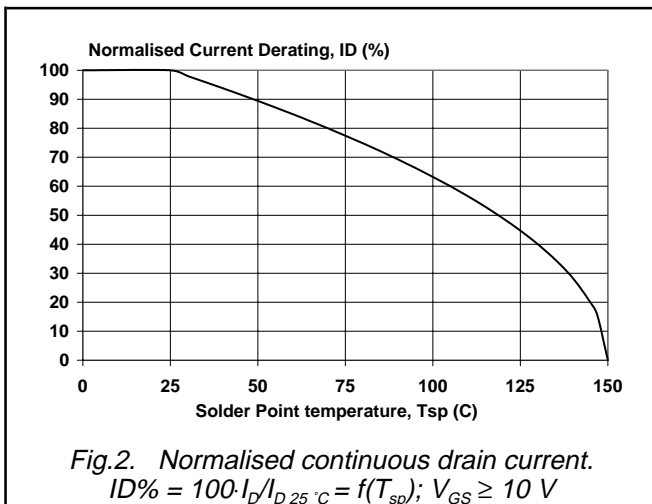
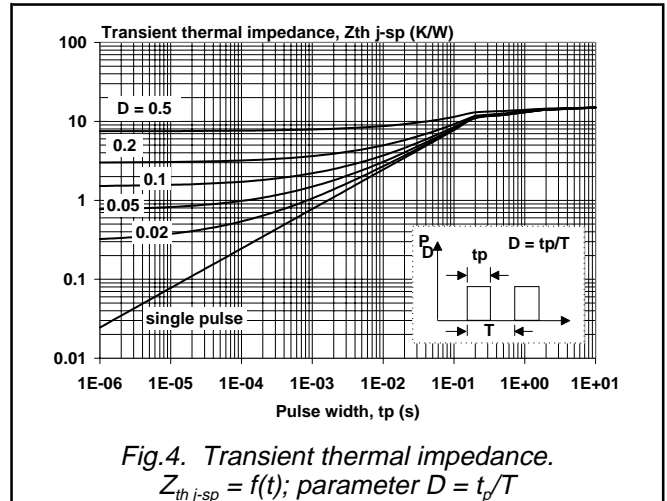
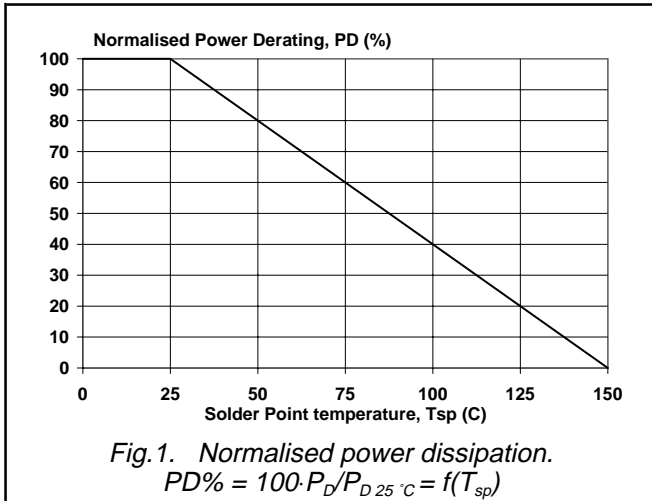
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA};$ $T_j = -55^\circ\text{C}$	100 89	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$ $T_j = 150^\circ\text{C}$ $T_j = -55^\circ\text{C}$	2 1.2 -	3 -	4 -	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 3\text{ A}$ $T_j = 150^\circ\text{C}$	- -	57 -	90 216	m Ω m Ω
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}$	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V};$ $T_j = 150^\circ\text{C}$	-	0.05	10 500	μA μA
$Q_{g(tot)}$	Total gate charge	$I_D = 6\text{ A}; V_{DD} = 80\text{ V}; V_{GS} = 10\text{ V}$	-	21	-	nC
Q_{gs}	Gate-source charge		-	2.5	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	8.2	-	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 50\text{ V}; R_D = 8.2\ \Omega;$	-	6	-	ns
t_r	Turn-on rise time	$V_{GS} = 10\text{ V}; R_G = 5.6\ \Omega$	-	15	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	20	-	ns
t_f	Turn-off fall time		-	10	-	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	633	-	pF
C_{oss}	Output capacitance		-	103	-	pF
C_{rss}	Feedback capacitance		-	61	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	$T_{sp} = 25^\circ\text{C}$	-	-	5.5	A
I_{SM}	Pulsed source current (body diode)		-	-	26	A
V_{SD}	Diode forward voltage	$I_F = 6\text{ A}; V_{GS} = 0\text{ V}$	-	0.8	1.2	V
t_{rr}	Reverse recovery time	$I_F = 6\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	55	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = 0\text{ V}; V_R = 25\text{ V}$	-	135	-	nC

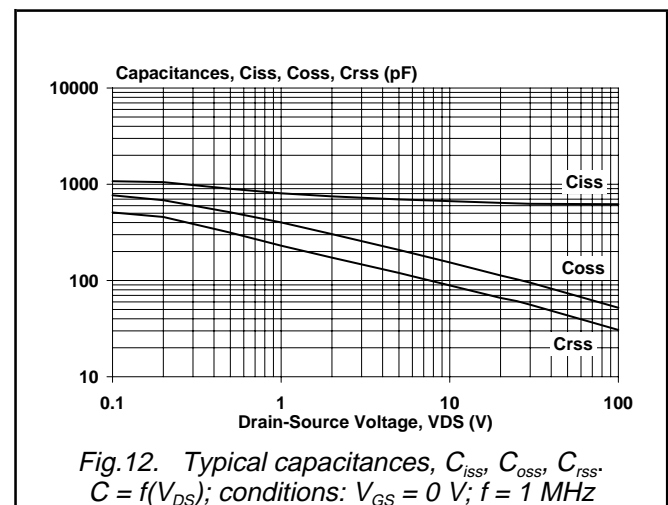
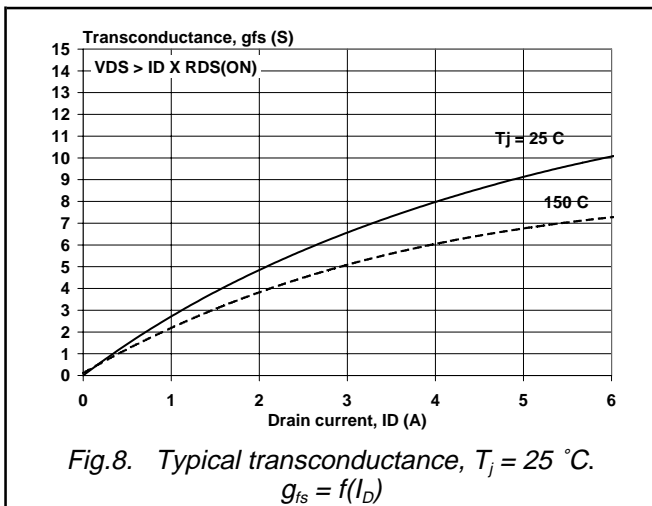
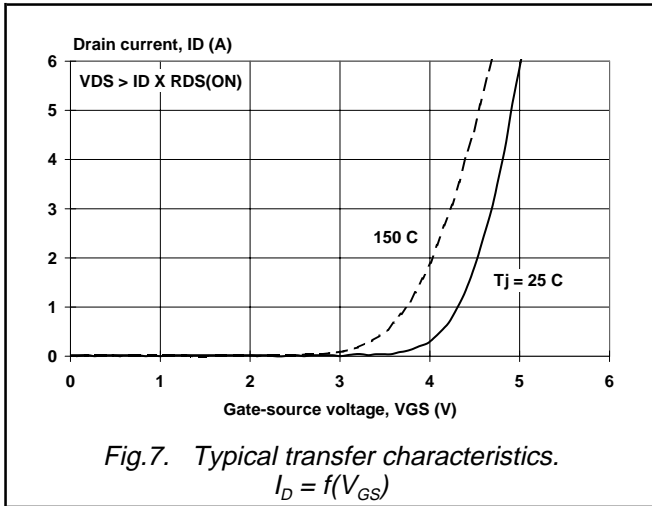
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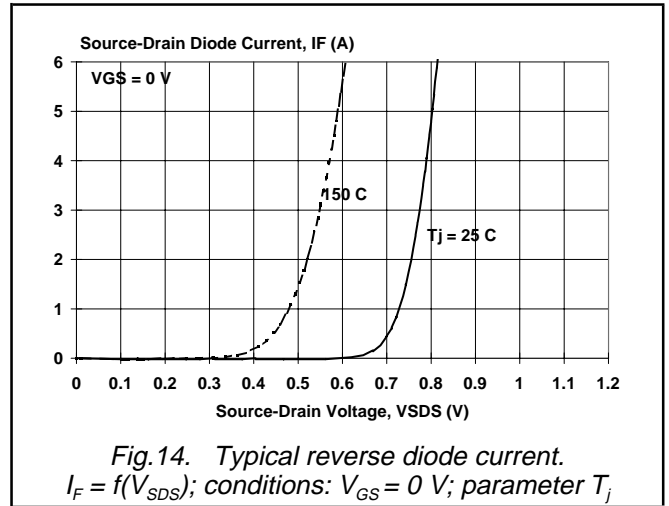
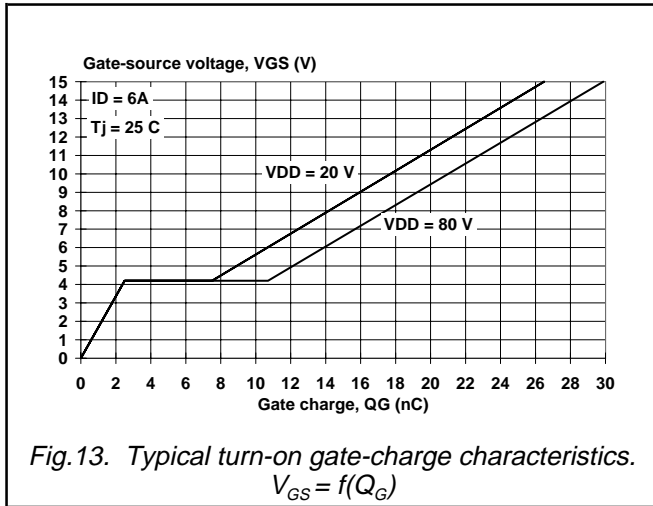
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N-channel TrenchMOS™ transistor

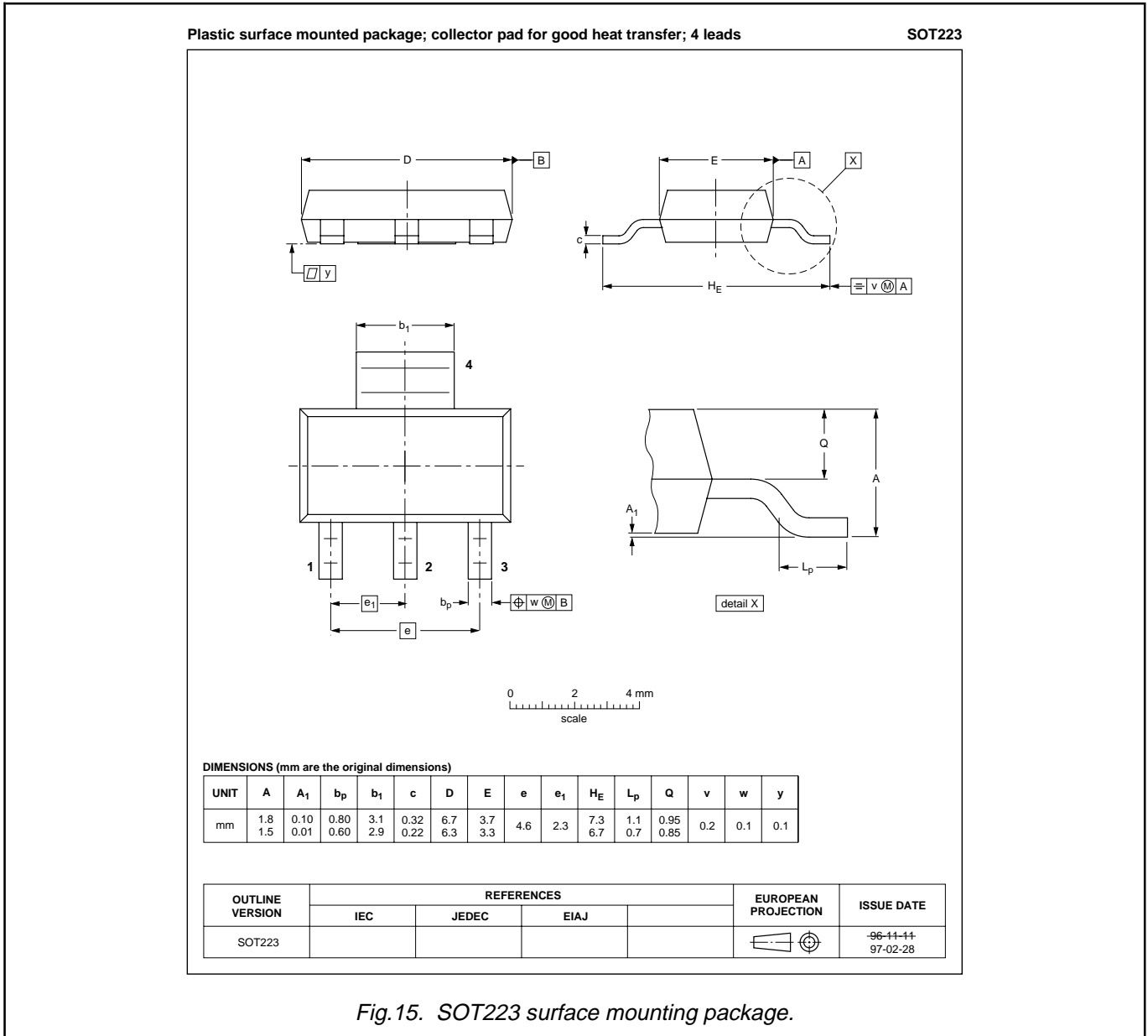
PHT6NQ10T



N-channel TrenchMOS™ transistor

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MECHANICAL DATA



Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to Discrete Semiconductor Packages, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

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PHT6NQ10T

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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[>>Nexperia\(安世\)](#)