PMBT3904RA

40 V, 200 mA double NPN switching transistor

13 September 2018 Product data sheet

1. General description

Double NPN switching transistor in an ultra small DFN1412-6 (SOT1268) leadless Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Leadless ultra small SMD plastic package
- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm

3. Applications

- General-purpose switching and amplification

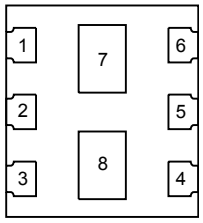
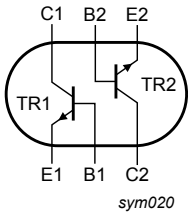
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	40	V
I_C	collector current			-	-	200	mA
h_{FE}	DC current gain	V_{CE} = 1 V; I_C = 10 mA		100	180	300	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 Transparent top view DFN1412-6 (SOT1268)	
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMBT3904RA	DFN1412-6	plastic, thermal enhanced ultra thin small outline package; no leads; 6 terminals; 1.4 mm x 1.2 mm x 0.47 mm body	SOT1268

7. Marking

Table 4. Marking codes

Type number	Marking code
PMBT3904RA	C6

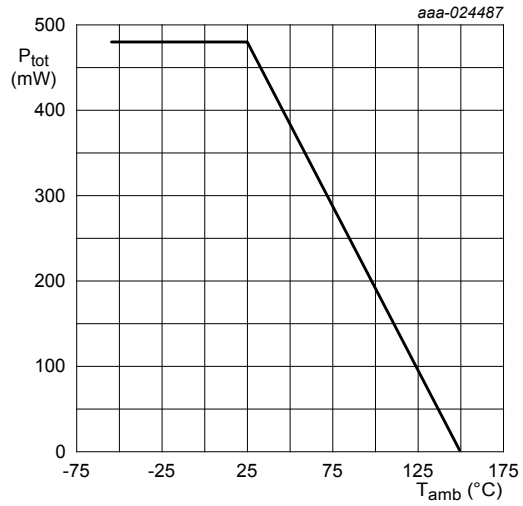
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{CBO}	collector-base voltage	open emitter		-	60	V
V_{CEO}	collector-emitter voltage	open base		-	40	V
V_{EBO}	emitter-base voltage	open collector		-	6	V
I_C	collector current			-	200	mA
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	200	mA
I_{BM}	peak base current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	325	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	480	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

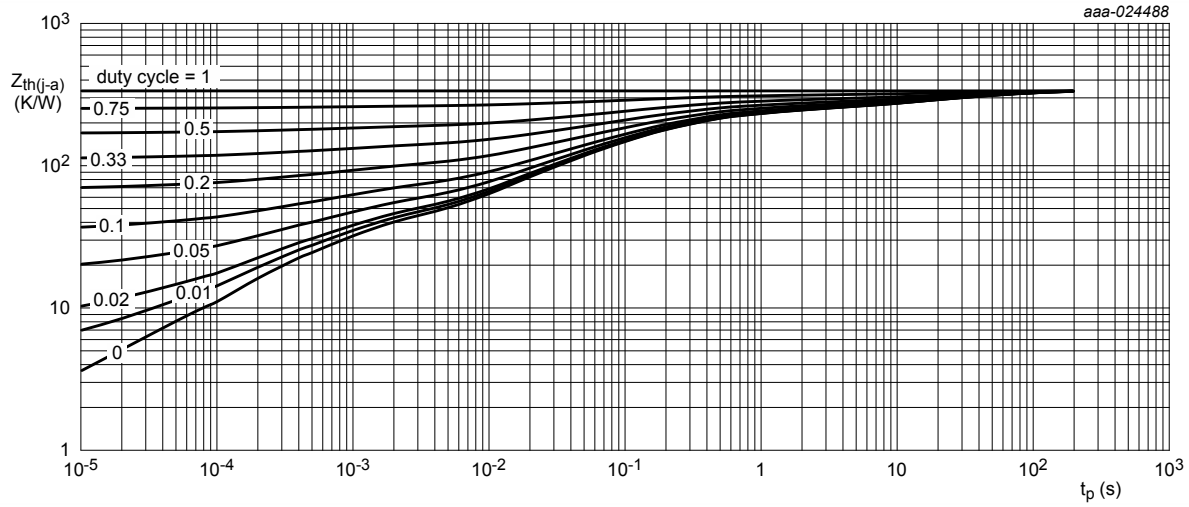
Fig. 1. Per device: Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	385	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	261	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

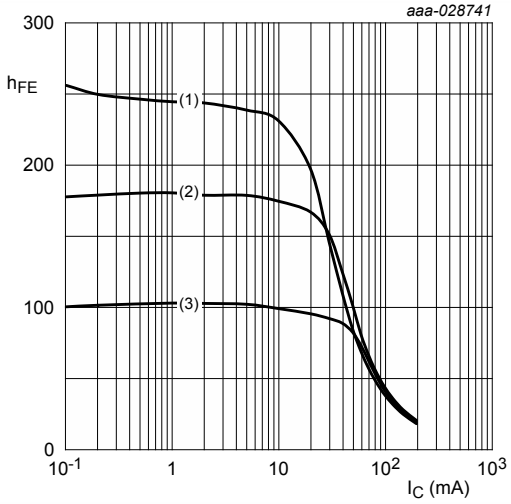
Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

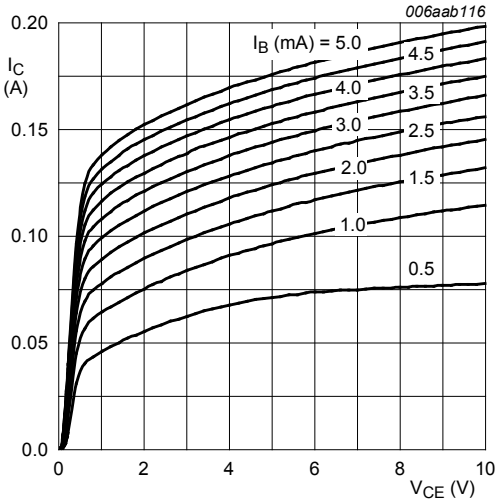
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 100 µA; I_E = 0 A		60	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 1 mA; I_B = 0 A		40	-	-	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_C = 0 A; I_E = 100 µA		6	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = 30 V; I_E = 0 A		-	-	50	nA
I_{EBO}	emitter-base cut-off current	V_{EB} = 6 V; I_C = 0 A		-	-	50	nA
h_{FE}	DC current gain	V_{CE} = 1 V; I_C = 100 µA		60	180	-	
		V_{CE} = 1 V; I_C = 1 mA		80	180	-	
		V_{CE} = 1 V; I_C = 10 mA		100	180	300	
		V_{CE} = 1 V; I_C = 50 mA		60	105	-	
		V_{CE} = 1 V; I_C = 100 mA; pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02		30	50	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 1 mA		-	75	200	mV
		I_C = 50 mA; I_B = 5 mA		-	120	300	mV
V_{BEsat}	base-emitter saturation voltage	I_C = 10 mA; I_B = 1 mA		650	750	850	mV
		I_C = 50 mA; I_B = 5 mA		-	850	950	mV
t_d	delay time	I_C = 10 mA; I_{Bon} = 1 mA; I_{Boff} = -1 mA		-	-	35	ns
t_r	rise time			-	-	35	ns
t_{on}	turn-on time			-	-	70	ns
t_s	storage time			-	-	200	ns
t_f	fall time			-	-	50	ns
t_{off}	turn-off time			-	-	250	ns
C_c	collector capacitance	V_{CB} = 5 V; I_E = 0 A; i_e = 0 A; f = 1 MHz		-	-	4	pF
C_e	emitter capacitance	V_{EB} = 0.5 V; I_C = 0 A; i_c = 0 A; f = 1 MHz		-	-	8	pF
f_T	transition frequency	V_{CE} = 20 V; I_C = 10 mA; f = 100 MHz		300	-	-	MHz



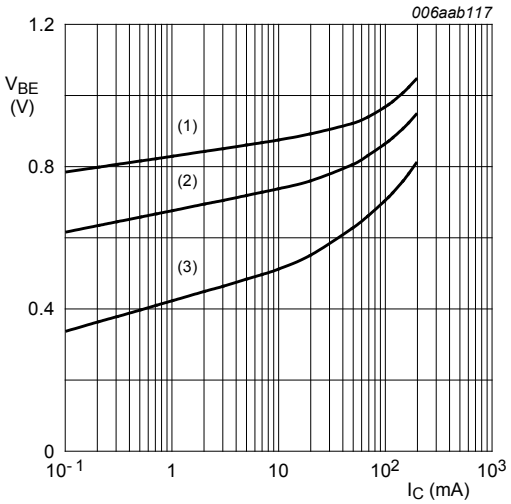
V_{CE} = 1 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 3. DC current gain as a function of collector current; typical values



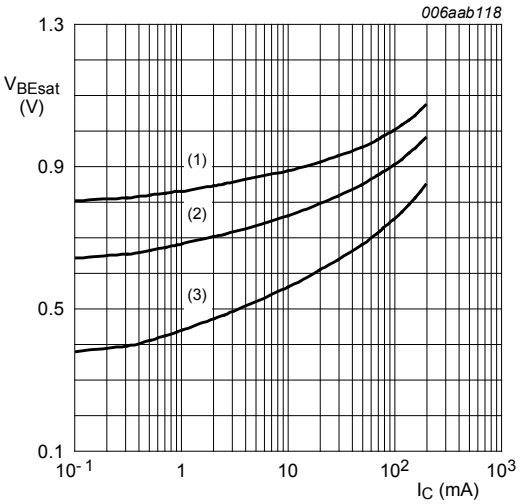
T_{amb} = 25 °C

Fig. 4. Collector current as a function of collector-emitter voltage; typical values



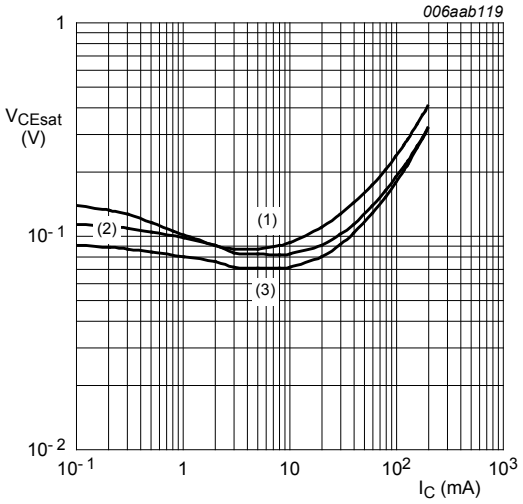
V_{CE} = 1 V
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 150 °C

Fig. 5. Base-emitter voltage as a function of collector current; typical values



I_C/I_B = 10
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 150 °C

Fig. 6. Base-emitter saturation voltage as a function of collector current; typical values



I_C/I_B = 10
(1) T_{amb} = 150 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 7. Collector-emitter saturation voltage as a function of collector current; typical values

11. Test information

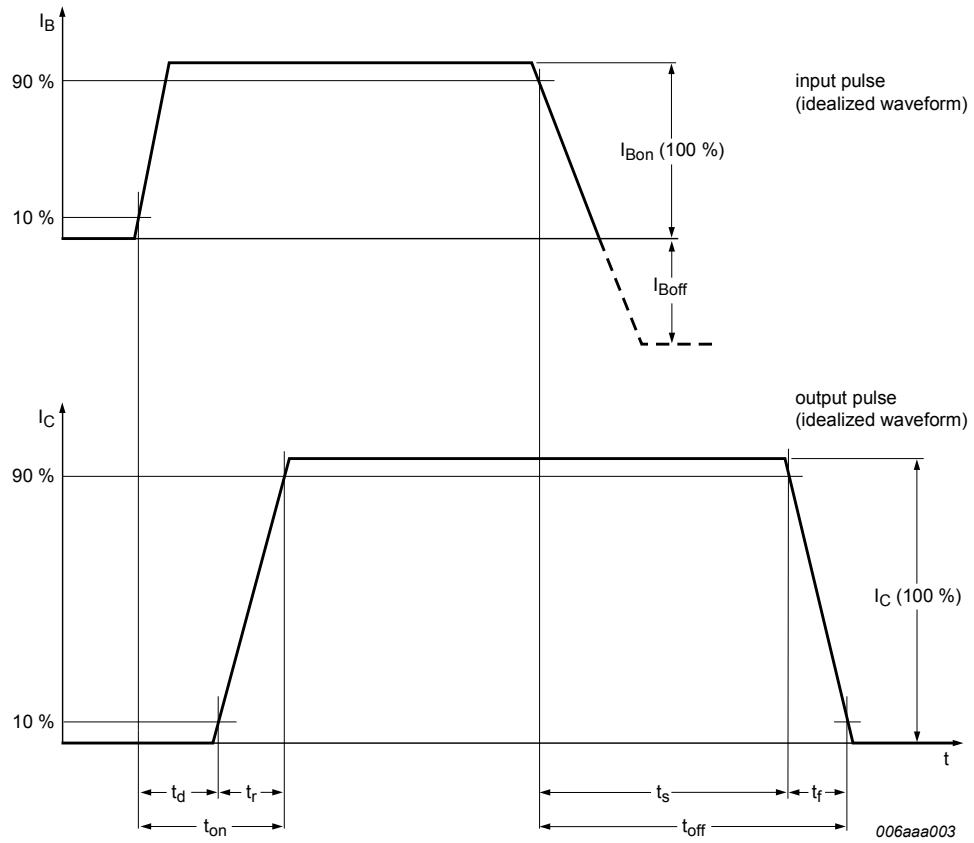


Fig. 8. Transistor switching time definition

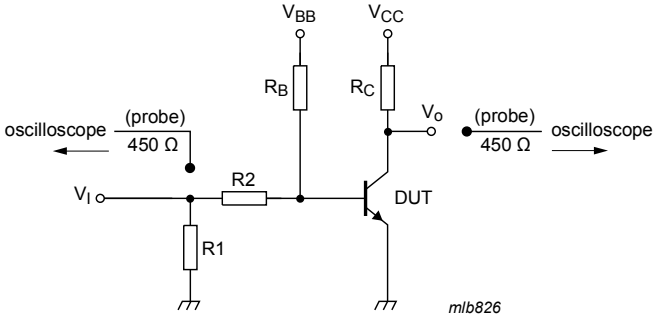
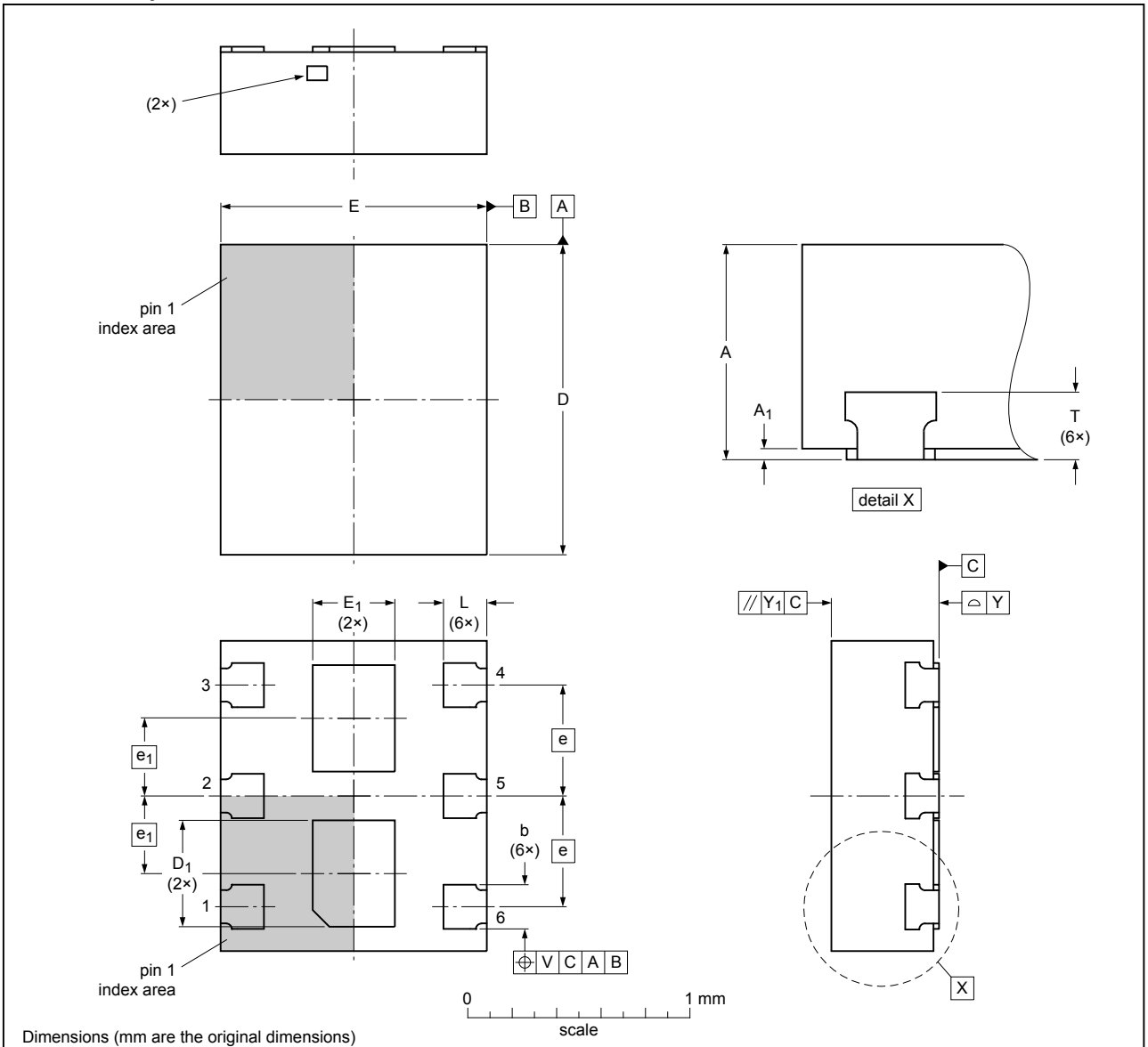


Fig. 9. Test circuit for switching times

12. Package outline

DFN1412-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.4 x 1.2 x 0.47 mm **SOT1268**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	b	D	D_1	E	E_1	e	e_1	L	T	V	Y	Y_1
mm	min	0.44	0.00	0.15	1.35	0.43	1.15	0.32			0.145	0.10			
	nom	0.47		0.20	1.40	0.48	1.20	0.37	0.5	0.35	0.195	0.16	0.1	0.05	0.05
	max	0.50	0.04	0.25	1.45	0.53	1.25	0.42			0.245	0.22			

Note
1. Dimension A is including plating thickness.

sot1268_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1268		---				~~18-08-23~~ 18-09-11

Fig. 10. Package outline DFN1412-6 (SOT1268)

13. Soldering

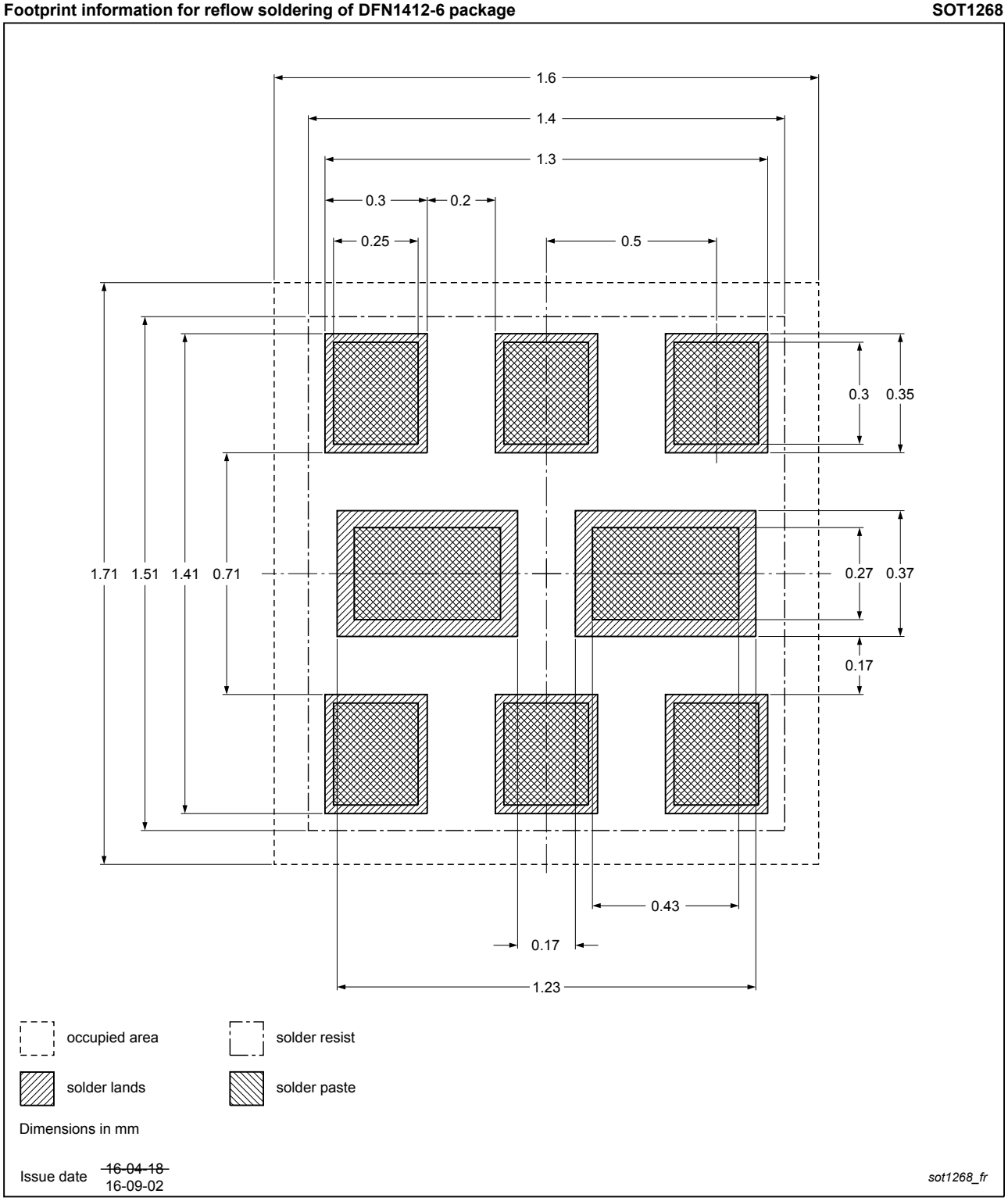


Fig. 11. Reflow soldering footprint for DFN1412-6 (SOT1268)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMBT3904RA v.1	20180913	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 13 September 2018

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