Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a 4 bumps Wafer Level Chip-Size Package (WLCSP) using Trench MOSFET technology.

2. Features and benefits

- · Low threshold voltage
- Ultra small package 0.78 x 0.78 x 0.35 mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- · Battery switch
- · High-speed line driver
- · High-side loadswitch
- · Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C		-	-	-20	V
V_{GS}	gate-source voltage			-8	-	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-	-4.2	Α
Static characte	Static characteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -3 \text{ A}; T_j = 25 \text{ °C}$		-	65	80	mΩ

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
A1	G	gate	1 2	D
A2	S	source	$A \bigcirc \bigcirc$	
B1	D	drain		G \downarrow \downarrow \downarrow
B2	S	source	В	
			Transparent top view WLCSP4 (WLCSP4_2-2)	S 017aaa259

6. Ordering information

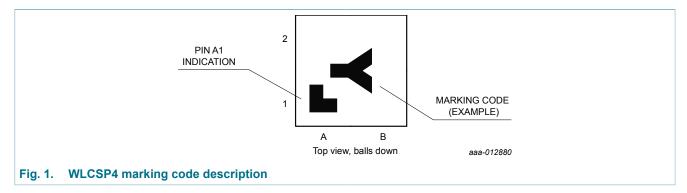
Table 3. Ordering information

Type number	Package	kage				
	Name	Description	Version			
PMCM4402UPE	WLCSP4	wafer level chip-size package; 4 bumps (2 x 2)	WLCSP4_2-2			

7. Marking

Table 4. Marking codes

Type number	Marking code
PMCM4402UPE	U



8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-4.2	Α
		V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-3.3	Α
		V_{GS} = -4.5 V; T_{amb} = 100 °C	[1]	-	-2.1	Α
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	-13	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	400	mW
			[1]	-	1.3	W
		T _{sp} = 25 °C		-	12.5	W
Tj	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain	n diode				<u>'</u>	
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.2	Α

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

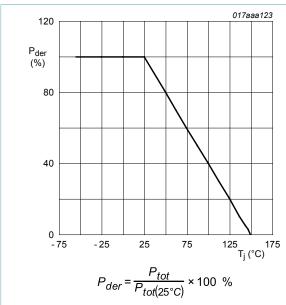


Fig. 2. Normalized total power dissipation as a function of junction temperature

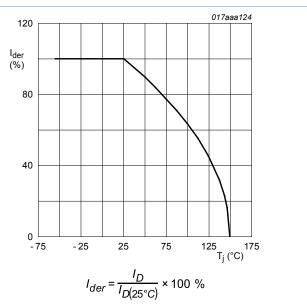
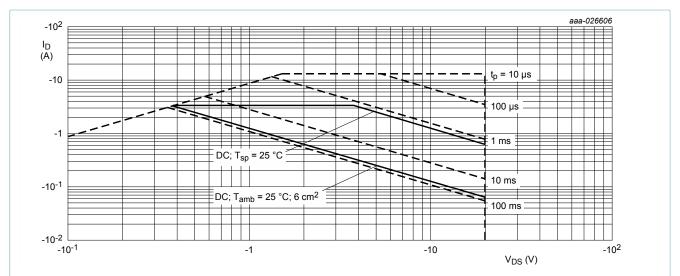


Fig. 3. Normalized continuous drain current as a function of junction temperature



Safe operating area; junction to ambient; continuous and peak drain currents as a function of drainsource voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient		[1]	-	250	300	K/W
			<u>[2]</u>	-	70	85	K/W
			<u>[3]</u>	-	85	100	K/W
		in free air; t ≤ 5 s	<u>[3]</u>	-	50	60	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	5	10	K/W

- Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint. Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain, 4-layer, 1 cm².
- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

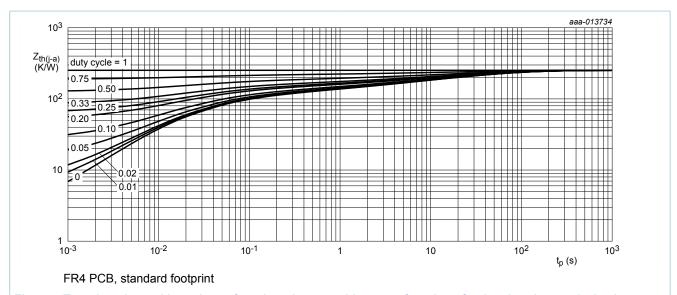


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

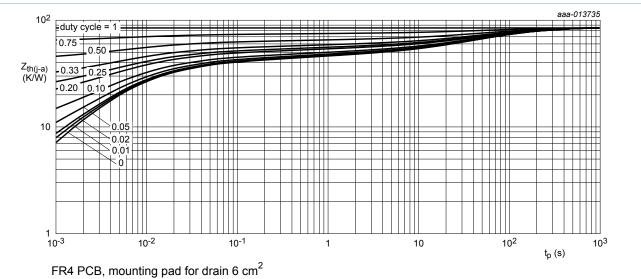


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	racteristics					
V _{(BR)DSS}	drain-source breakdown voltage	$I_D = -250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^{\circ}C$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	-0.4	-0.6	-0.9	V
I _{DSS}	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _j = 25 °C	-	-	-1	μΑ
I _{GSS}	gate leakage current	V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C	-	-	10	μΑ
		$V_{GS} = -8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	-	-10	μΑ
		V _{GS} = 4.5 V; V _{DS} = 0 V; T _j = 25 °C	-	-	1	μΑ
		V _{GS} = -4.5 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-1	μΑ
		V _{GS} = 2.5 V; V _{DS} = 0 V; T _j = 25 °C	-	-	200	nA
		$V_{GS} = -2.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-200	nA
R _{DSon}	drain-source on-state	$V_{GS} = -4.5 \text{ V}; I_D = -3 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	65	80	mΩ
	resistance	V _{GS} = -4.5 V; I _D = -3 A; T _j = 150 °C	-	93	114	mΩ
		V_{GS} = -2.5 V; I_{D} = -2 A; T_{j} = 25 °C	-	88	110	mΩ
		V_{GS} = -1.8 V; I_{D} = -0.1 A; T_{j} = 25 °C	-	120	180	mΩ
9 _{fs}	forward transconductance	V_{DS} = -6 V; I_{D} = -3 A; T_{j} = 25 °C	-	14	-	S
R _G	gate resistance	f = 1 MHz; T _j = 25 °C	-	6	-	Ω
Dynamic c	haracteristics					
Q _{G(tot)}	total gate charge	V_{DS} = -10 V; I_{D} = -3 A; V_{GS} = -4.5 V;	-	6.2	10	nC
Q_{GS}	gate-source charge	T _j = 25 °C	-	0.7	-	nC
Q_{GD}	gate-drain charge		-	2	-	nC
C _{iss}	input capacitance	$V_{DS} = -10 \text{ V; } f = 1 \text{ MHz; } V_{GS} = 0 \text{ V;}$	-	450	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	72	-	pF
C _{rss}	reverse transfer capacitance		-	66	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = -10 V; I_{D} = -3.3 A; V_{GS} = -4.5 V;	-	4	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 ^{\circ}C$	-	17	-	ns
t _{d(off)}	turn-off delay time		-	26	-	ns
t _f	fall time		-	11	-	ns
Source-dra	ain diode		'			
V_{SD}	source-drain voltage	I _S = -1.2 A; V _{GS} = 0 V; T _i = 25 °C	_	-0.8	-1.2	V

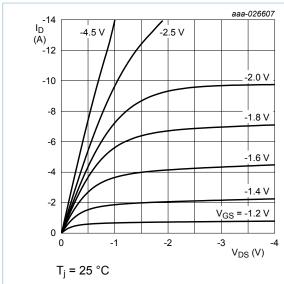


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

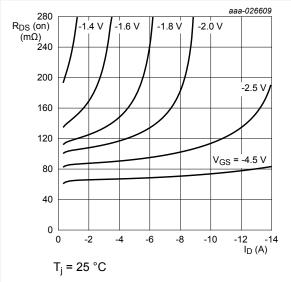


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

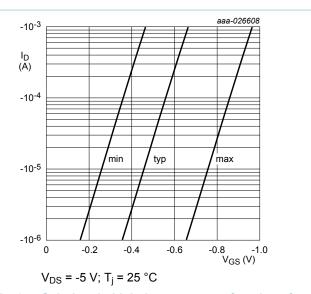


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

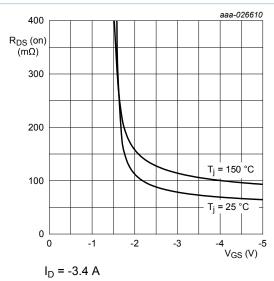


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

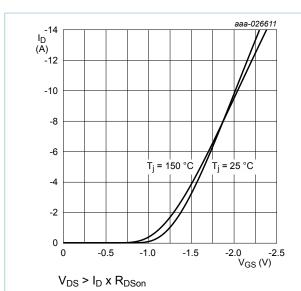


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

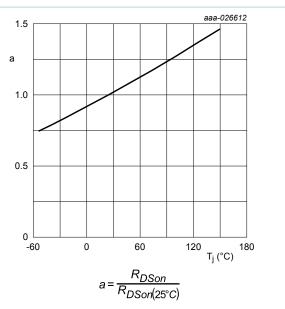


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

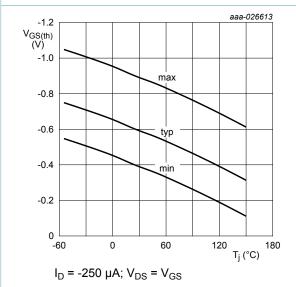


Fig. 13. Gate-source threshold voltage as a function of junction temperature

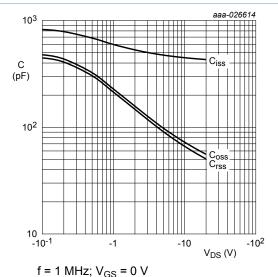


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

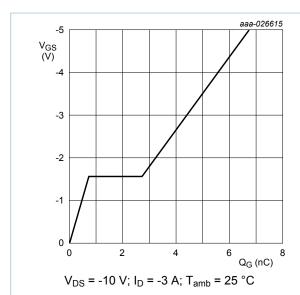


Fig. 15. Gate-source voltage as a function of gate charge; typical values

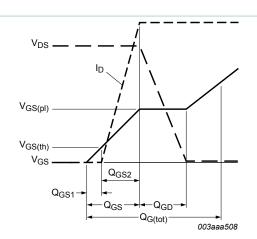


Fig. 16. MOSFET transistor: Gate charge waveform definitions

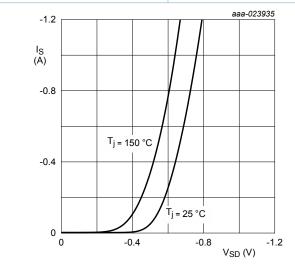
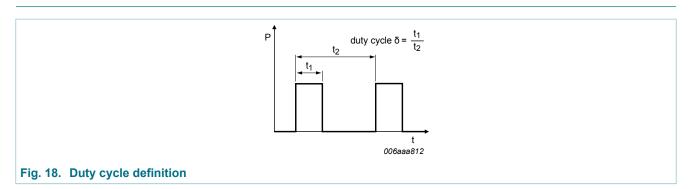


Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

 $V_{GS} = 0 V$



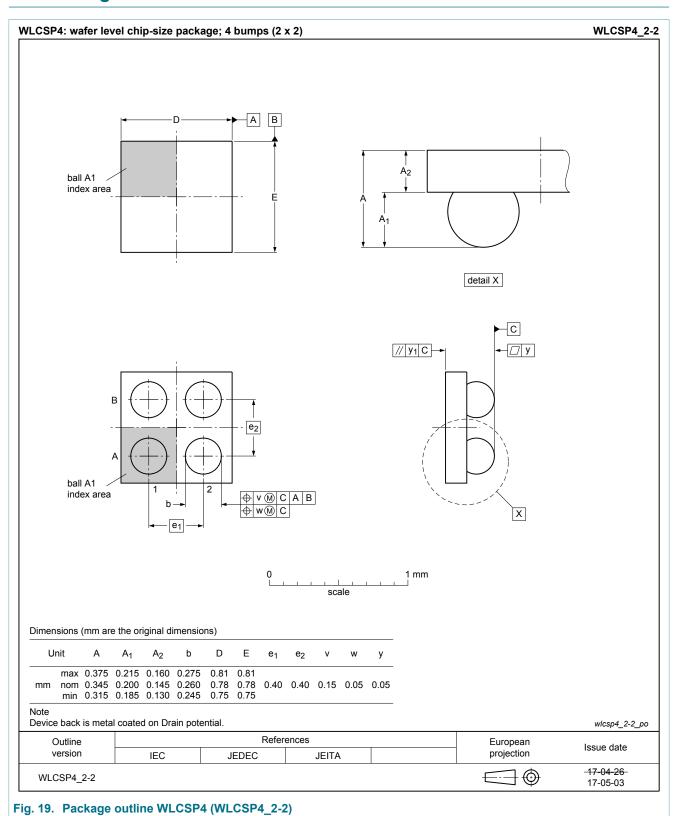
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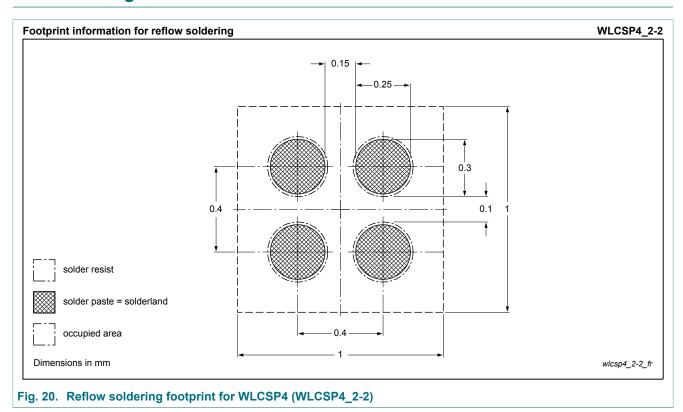
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12. Package outline



13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMCM4402UPE v.1	20170530	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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