



PMCM6501UPE

20 V, P-channel Trench MOSFET

3 July 2017

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a 6 bumps Wafer Level Chip-Size Package (WLCSP) using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Ultra small package: 0.98 x 1.48 x 0.35 mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Battery switch
- High-speed line driver
- High-side loadswitch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-7.3	A
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -3\text{ A}; T_j = 25\text{ °C}$	-	22	30	mΩ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm²

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
A1	G	gate	<p>Transparent top view WLCSP6 (WLCSP6_3-2)</p>	<p>017aaa259</p>
A2	S	source		
B1	S	source		
B2	S	source		
C1	D	drain		
C2	D	drain		

6. Ordering information

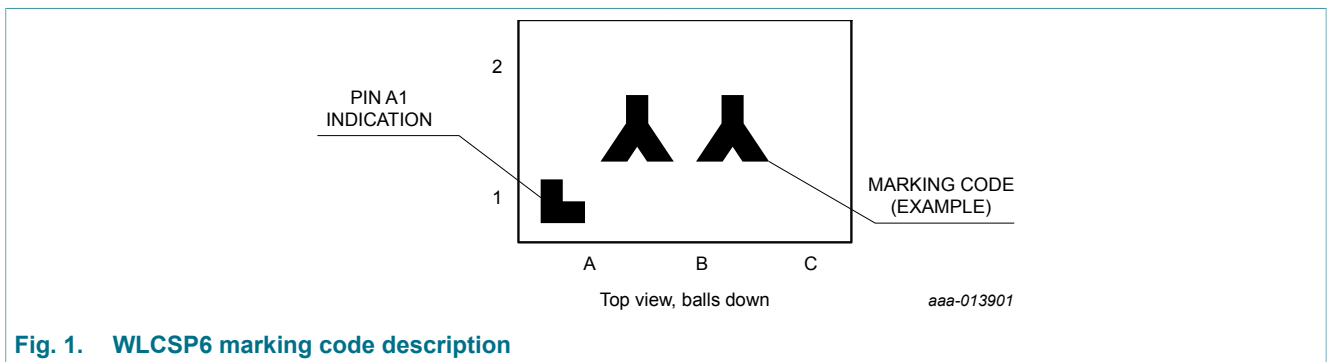
Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PMCM6501UPE	WLCSP6	wafer level chip-size package; 6 bumps (3 x 2)	WLCSP6_3-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PMCM6501UPE	AF



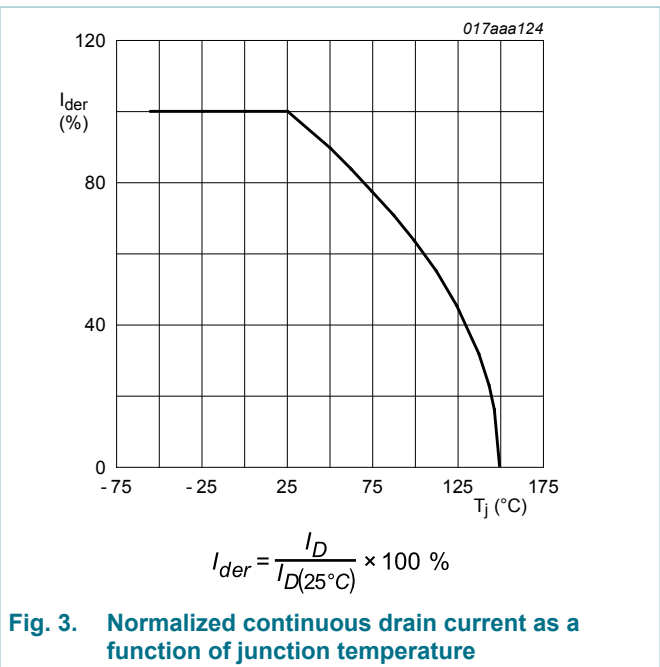
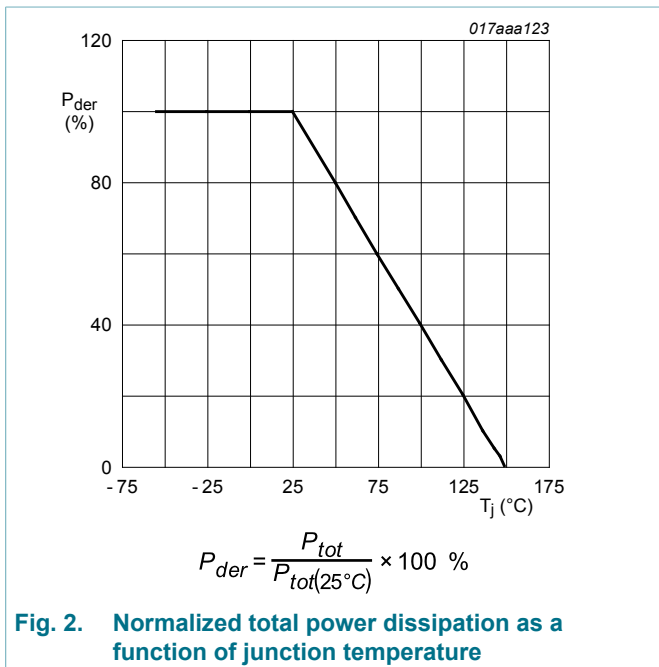
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-7.3	A
		V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-5.6	A
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-3.5	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-22	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	556	mW
			[1]	-	1.3	W
		T _{sp} = 25 °C		-	12.5	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.3	A

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm²
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



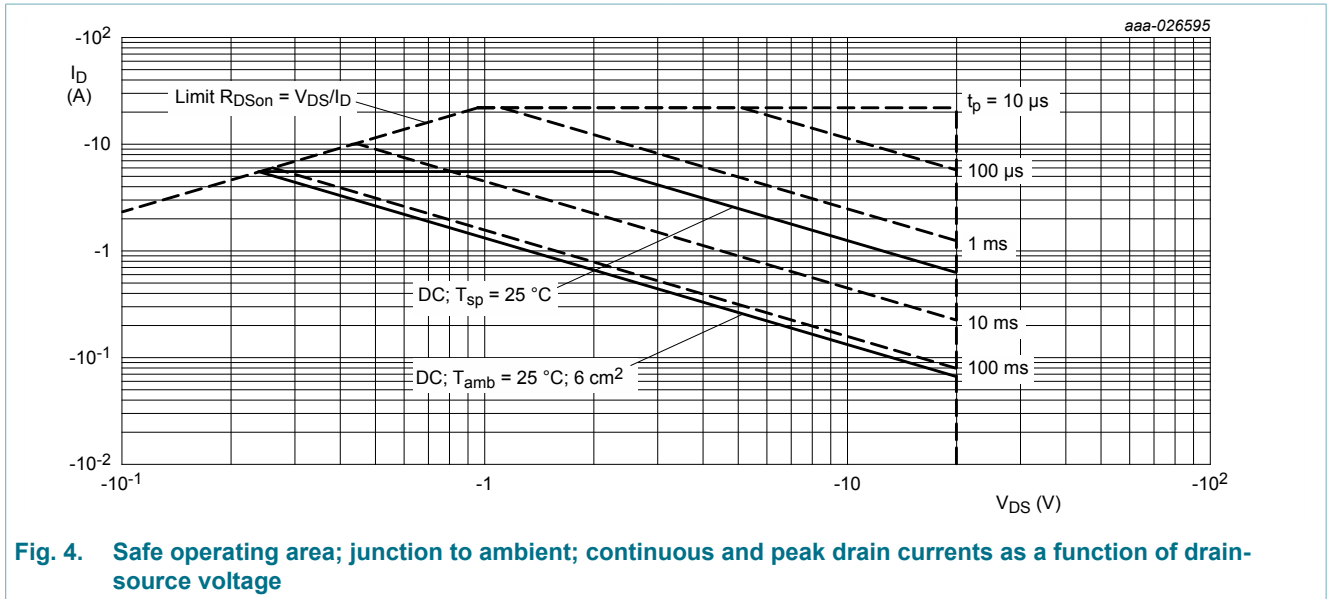


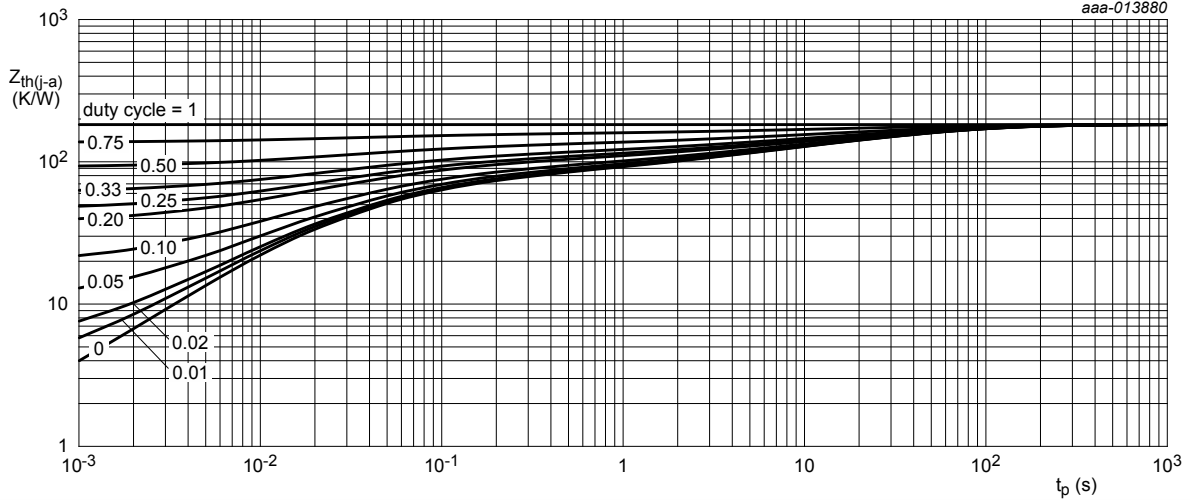
Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

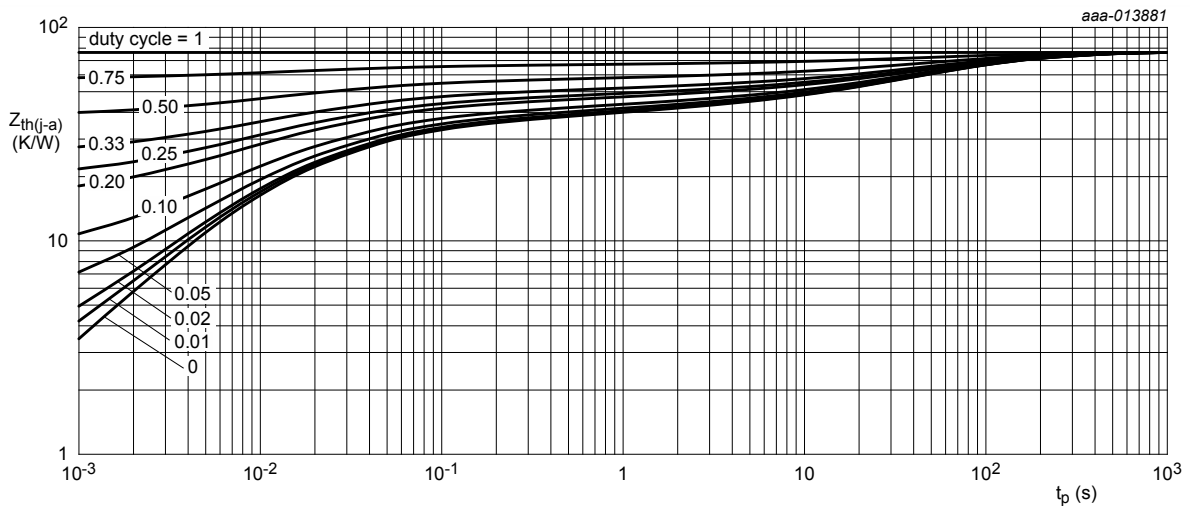
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	180	225	K/W
			[2]	-	65	85	K/W
			[3]	-	75	95	K/W
		$t \leq 5 \text{ s}$	[3]	-	45	55	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	5	10	K/W

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single sided-copper; tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain, 4 layer, 1 cm^2
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm^2 .



FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm^2

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu\text{A}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$	-0.4	-0.6	-0.9	V
I_{DSS}	drain leakage current	$V_{DS} = -20 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	10	μA
		$V_{GS} = -8 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-10	μA
		$V_{GS} = 4.5 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{GS} = -4.5 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	μA
		$V_{GS} = 2.5 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	200	nA
		$V_{GS} = -2.5 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-200	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}$; $I_D = -3 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	22	30	m Ω
		$V_{GS} = -4.5 \text{ V}$; $I_D = -3 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$	-	30	43	m Ω
		$V_{GS} = -2.5 \text{ V}$; $I_D = -3 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	28	44	m Ω
		$V_{GS} = -1.8 \text{ V}$; $I_D = -1 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	38	79	m Ω
g_{fs}	forward transconductance	$V_{DS} = -6 \text{ V}$; $I_D = -3 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	22	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$	-	15	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 \text{ V}$; $I_D = -3 \text{ A}$; $V_{GS} = -4.5 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	19.1	29	nC
Q_{GS}	gate-source charge		-	1.9	-	nC
Q_{GD}	gate-drain charge		-	5.4	-	nC
C_{iss}	input capacitance	$V_{DS} = -10 \text{ V}$; $f = 1 \text{ MHz}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	1420	-	pF
C_{oss}	output capacitance		-	210	-	pF
C_{rss}	reverse transfer capacitance		-	190	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = -10 \text{ V}$; $I_D = -5.6 \text{ A}$; $V_{GS} = -4.5 \text{ V}$; $R_{G(ext)} = 6 \text{ } \Omega$; $T_j = 25 \text{ }^\circ\text{C}$	-	6	-
t_r	rise time	-		35	-	ns
$t_{d(off)}$	turn-off delay time	-		105	-	ns
t_f	fall time	-		55	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -1.2 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-0.7	-1.2	V

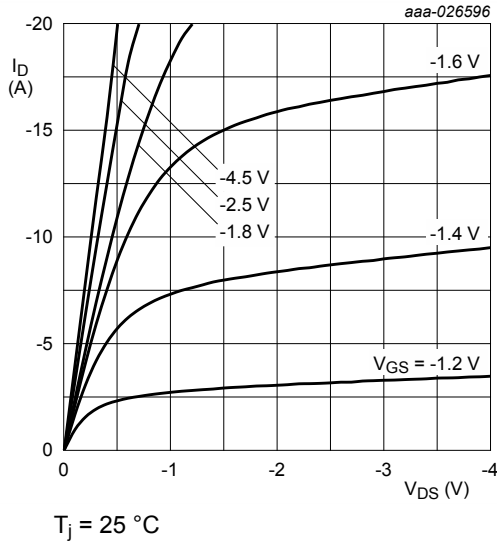


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

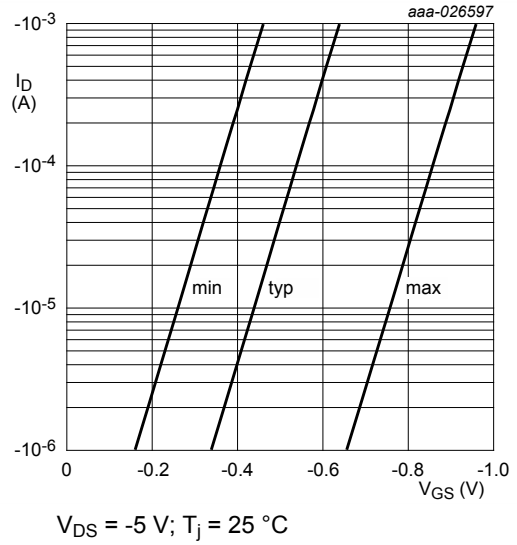


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

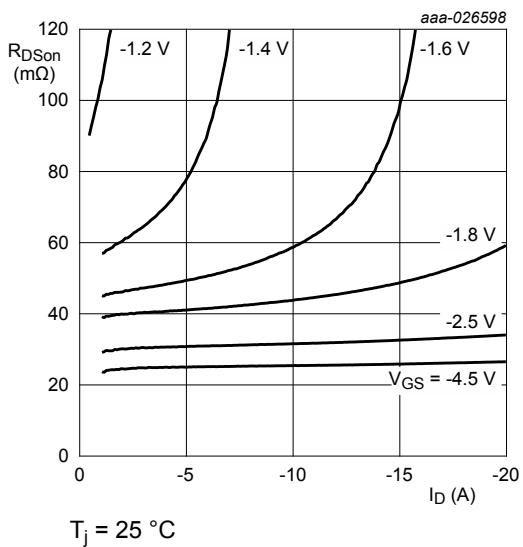


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

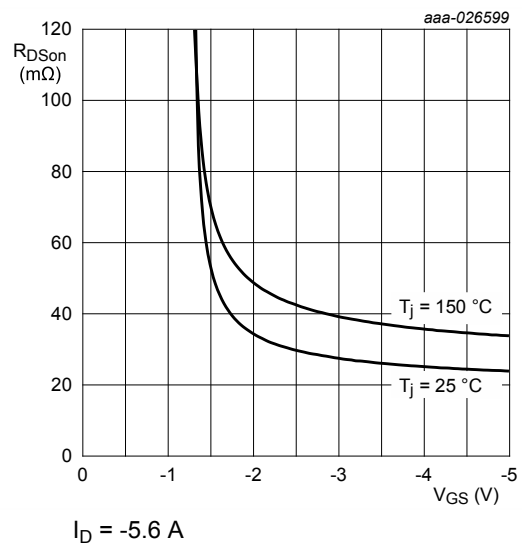


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

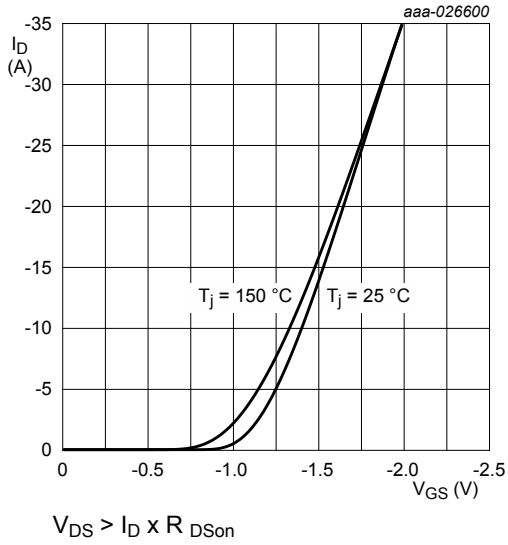


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

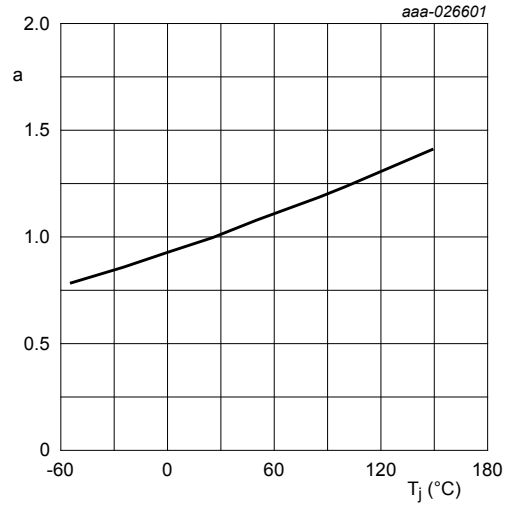


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

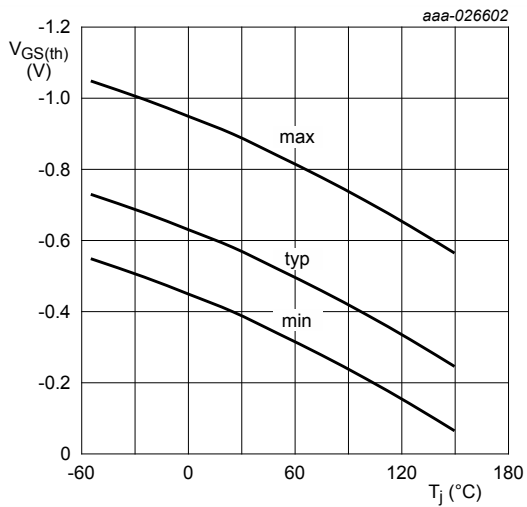


Fig. 13. Gate-source threshold voltage as a function of junction temperature

$I_D = -250 \mu A; V_{DS} = V_{GS}$

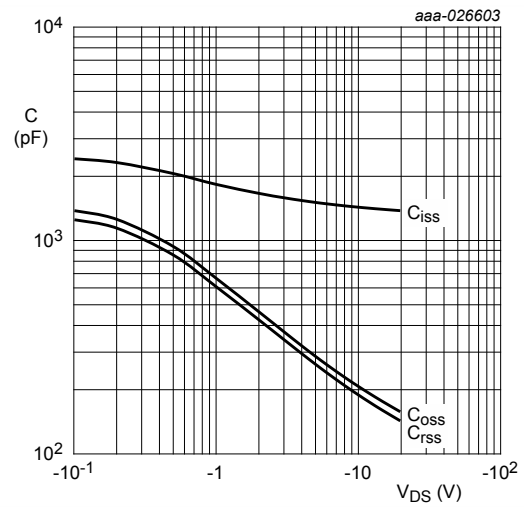
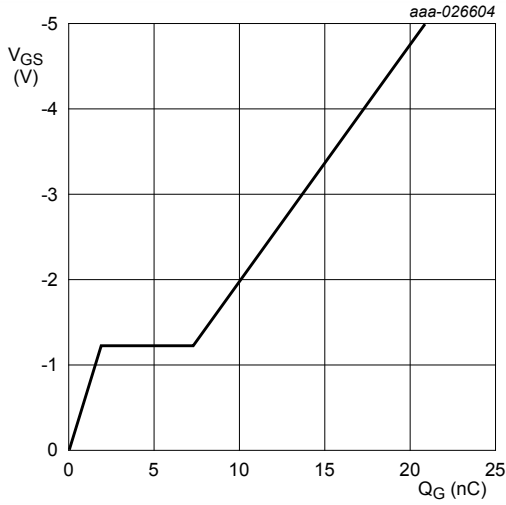


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$



$V_{DS} = -10\text{ V}; I_D = -3\text{ A}; T_{amb} = 25\text{ }^\circ\text{C}$

Fig. 15. Gate-source voltage as a function of gate charge; typical values

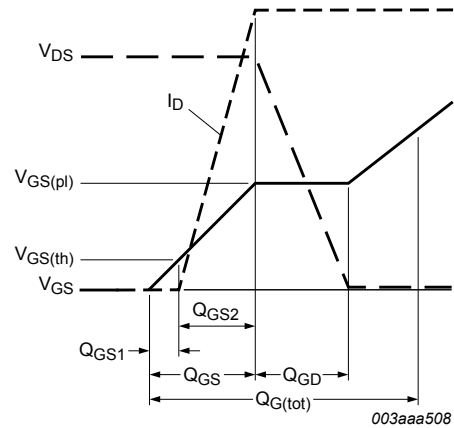
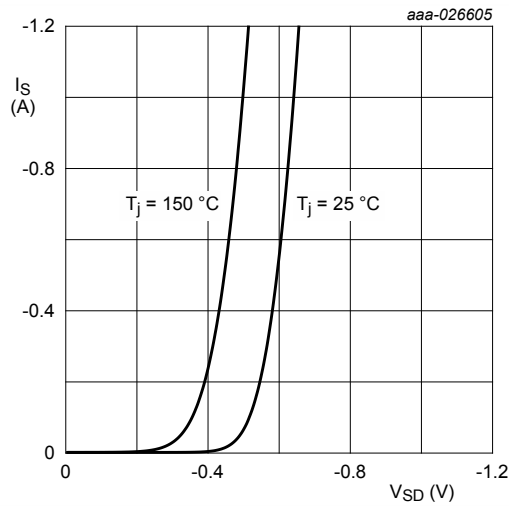


Fig. 16. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

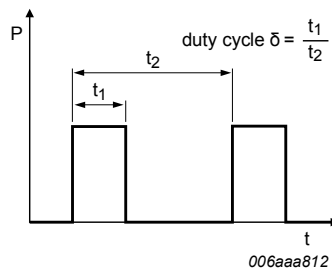
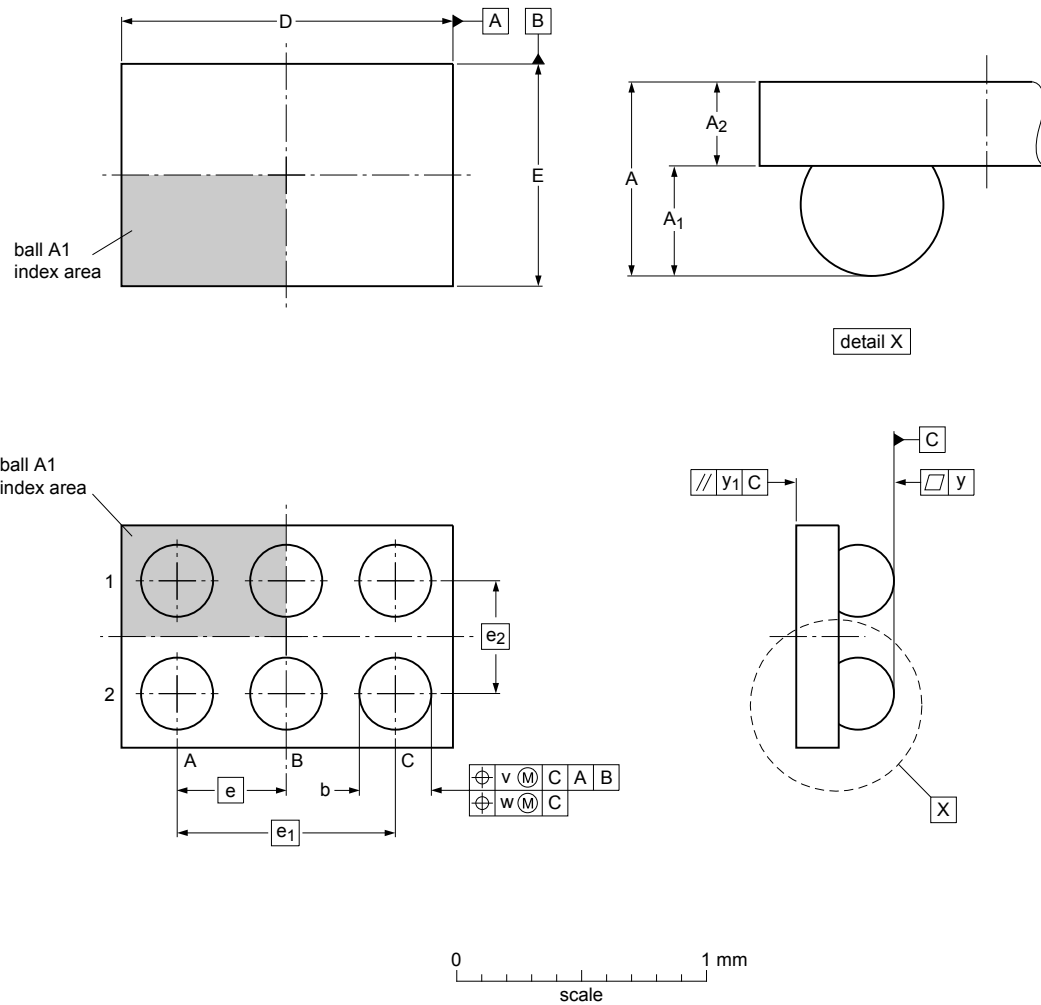


Fig. 18. Duty cycle definition

12. Package outline

WLCSP6: wafer level chip-size package; 6 bumps (3 x 2)

WLCSP6_3-2



Dimensions (mm are the original dimensions)

Unit	A	A ₁	A ₂	b	D	E	e	e ₁	e ₂	v	w	y
max	0.375	0.215	0.160	0.275	1.51	1.01						
nom	0.345	0.200	0.145	0.260	1.48	0.98	0.50	1.00	0.50	0.15	0.05	0.05
min	0.315	0.185	0.130	0.245	1.45	0.95						

Note

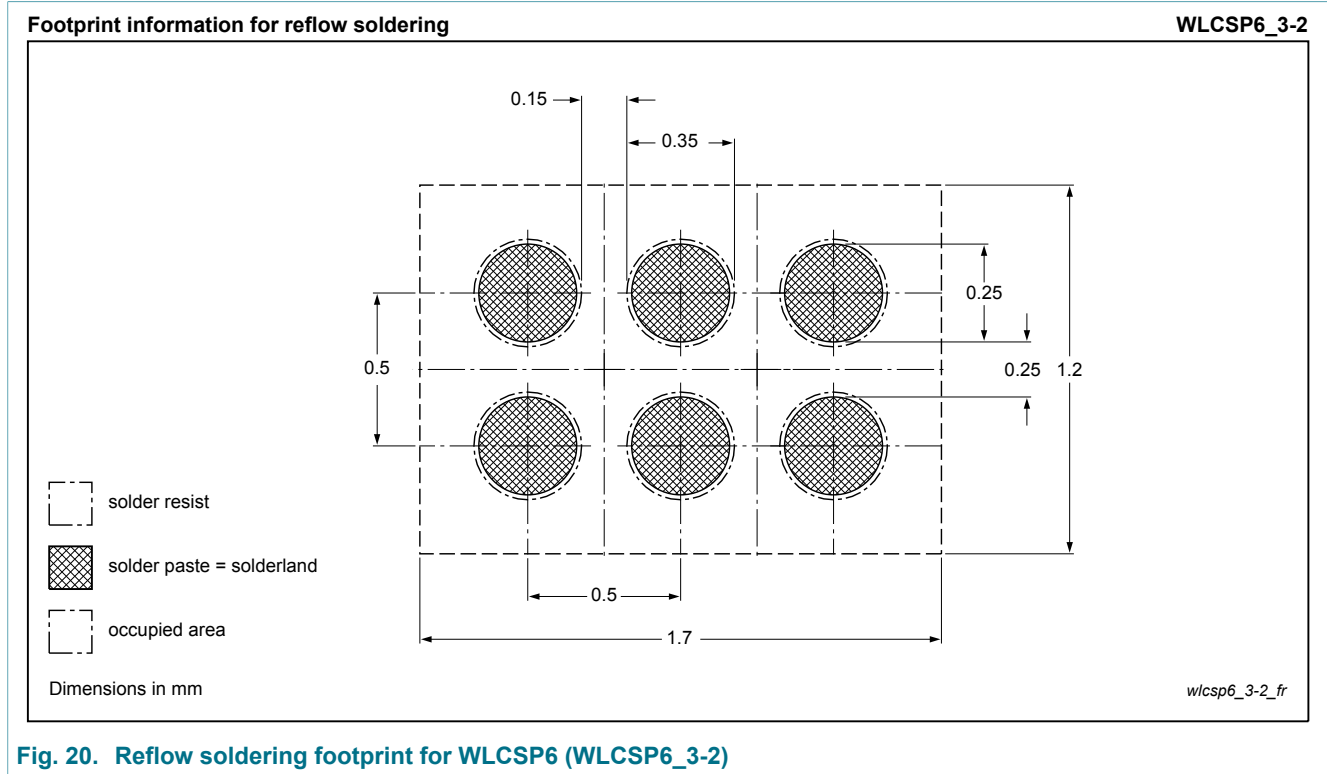
Device back is metal coated on Drain potential.

wlcsp6_3-2_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
WLCSP6_3-2					-17-04-26- 17-05-03

Fig. 19. Package outline WLCSP6 (WLCSP6_3-2)

13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMCM6501UPE v.1	20170703	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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