



PMCPB5530X

20 V, complementary Trench MOSFET

Rev. 1 — 26 June 2012

Product data sheet

1. Product profile

1.1 General description

Complementary N/P-channel enhancement mode Field-Effect Transistor (FET) in a small and leadless ultra thin DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Very fast switching
- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction

1.3 Applications

- Charging switch for portable devices
- DC-to-DC converters
- Small brushless DC motor drive
- Power management in battery-driven portables
- Hard disc and computing power management

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1 (N-channel), Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 3 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	26	34	m Ω
TR2 (P-channel), Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -3.4 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	55	70	m Ω
TR1 (N-channel)						
V_{DS}	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$	-	-	20	V
V_{GS}	gate-source voltage		-12	-	12	V
I_D	drain current	$V_{GS} = 4.5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}; t \leq 5 \text{ s}$	1	-	5.3	A

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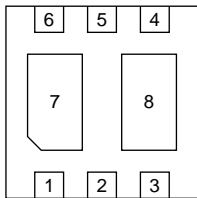
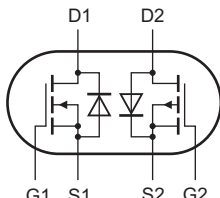
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR2 (P-channel)						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
V_{GS}	gate-source voltage		-12	-	12	V
I_D	drain current	$V_{GS} = -4.5\text{ V}$; $T_{amb} = 25\text{ °C}$; $t \leq 5\text{ s}$	[1]	-	-4.5	A

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view</p>	 <p>017aaa261</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

DFN2020-6 (SOT1118)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMCPB5530X	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1118

4. Marking

Table 4. Marking codes

Type number	Marking code
PMCPB5530X	1W

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
TR1 (N-channel)					
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	20	V
V_{GS}	gate-source voltage		-12	12	V

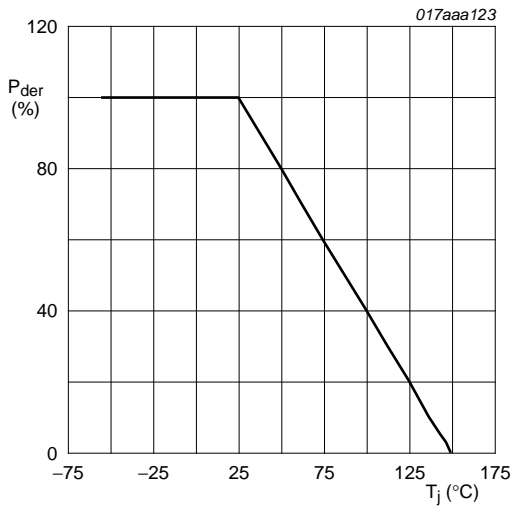
Table 5. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	5.3	A
		V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	4	A
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	-	2.6	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	12	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	490	mW
			[1]	-	1170	mW
		T _{sp} = 25 °C		-	8330	mW
TR1 (N-channel), Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	1.2	A
TR2 (P-channel)						
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-12	12	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-4.5	A
		V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-3.4	A
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-2.2	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-14	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	490	mW
			[1]	-	1170	mW
		T _{sp} = 25 °C		-	8330	mW
TR2 (P-channel), Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.2	A
Per device						
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

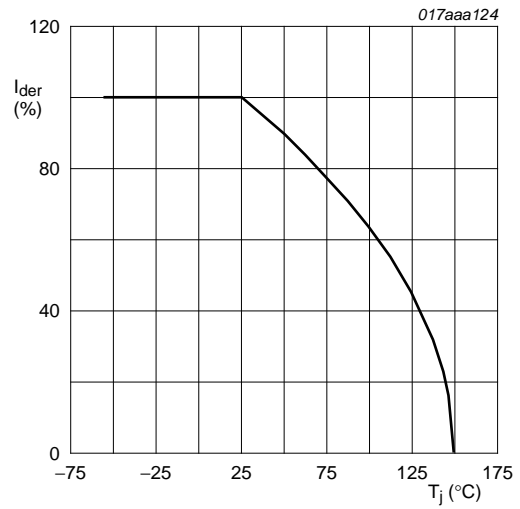
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.



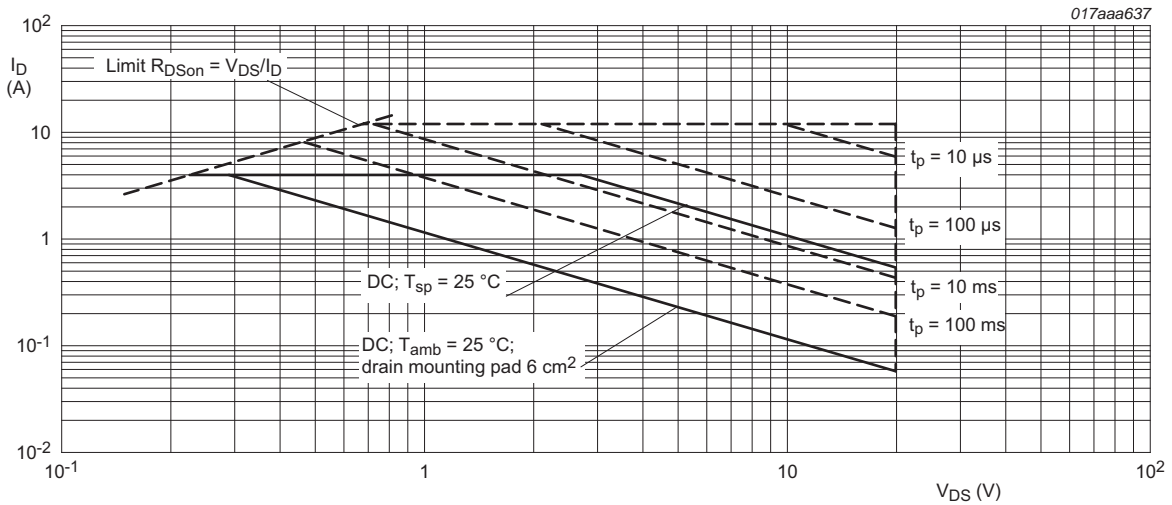
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



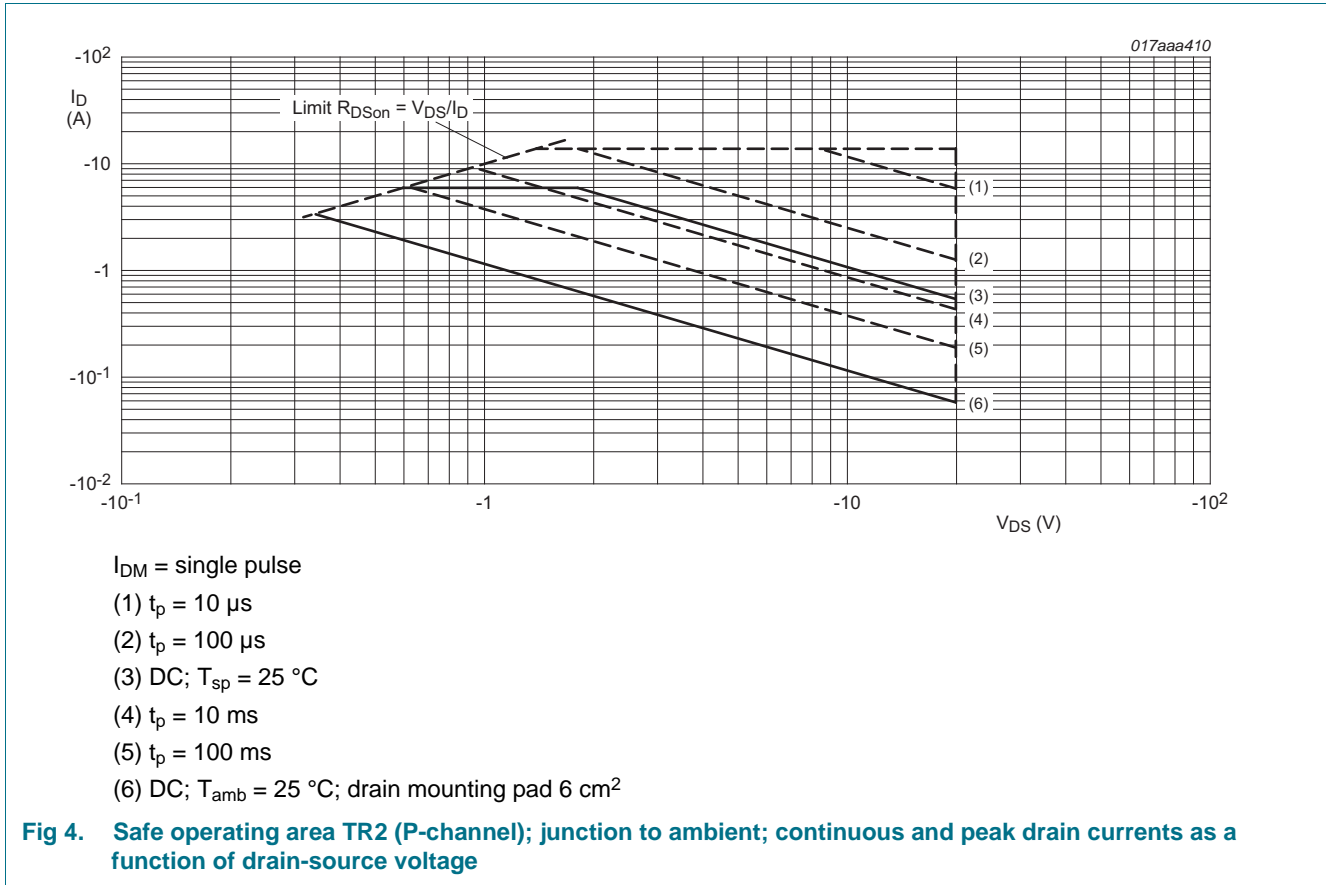
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} = single pulse

Fig 3. Safe operating area TR1 (N-channel); junction to ambient; continuous and peak drain currents as a function of drain-source voltage



6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1 (N-channel)							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	223	256	K/W
			[2]	-	93	107	K/W
			[3]	-	55	63	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			10	15	K/W	
TR2 (P-channel)							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	223	256	K/W
			[2]	-	93	107	K/W
			[3]	-	55	63	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			10	15	K/W	

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm^2 .

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm^2 , $t \leq 5 \text{ s}$.

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1 (N-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	0.4	0.65	0.9	V
I_{DSS}	drain leakage current	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	11	μA
I_{GSS}	gate leakage current	$V_{GS} = 12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 3 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	26	34	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 3 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	49	63	m Ω
		$V_{GS} = 2.5 \text{ V}; I_D = 1.4 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	33	46	m Ω
		$V_{GS} = 1.8 \text{ V}; I_D = 1.4 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	50	69	m Ω
g_{fs}	transfer conductance	$V_{DS} = 5 \text{ V}; I_D = 3 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	12	-	S
TR1 (N-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	14.4	21.7	nC
Q_{GS}	gate-source charge		-	1.1	-	nC
Q_{GD}	gate-drain charge		-	1.5	-	nC
C_{iss}	input capacitance	$V_{DS} = 10 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	660	-	pF
C_{oss}	output capacitance		-	87	-	pF
C_{riss}	reverse transfer capacitance		-	74	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 4.5 \text{ V}; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	4	-	ns
t_r	rise time		-	15	-	ns
$t_{d(off)}$	turn-off delay time		-	40	-	ns
t_f	fall time		-	16	-	ns
TR1 (N-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	$I_S = 1.2 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.8	1.2	V
TR2 (P-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	-0.47	-0.65	-0.9	V
I_{DSS}	drain leakage current	$V_{DS} = -20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	μA
		$V_{DS} = -20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	-10	μA
I_{GSS}	gate leakage current	$V_{GS} = 12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-100	nA
		$V_{GS} = -12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-100	nA

Table 7. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -3.4\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	55	70	m Ω
		$V_{GS} = -4.5\text{ V}; I_D = -3.4\text{ A}; T_j = 150\text{ }^\circ\text{C}$	-	78	99	m Ω
		$V_{GS} = -2.5\text{ V}; I_D = -3\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	75	90	m Ω
		$V_{GS} = -1.8\text{ V}; I_D = -1.5\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	110	135	m Ω
g_{fs}	transfer conductance	$V_{DS} = -10\text{ V}; I_D = -3.4\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	15	-	S
TR2 (P-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10\text{ V}; I_D = -3.4\text{ A}; V_{GS} = -5\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	8.1	12.2	nC
Q_{GS}	gate-source charge		-	1.2	-	nC
Q_{GD}	gate-drain charge		-	1.5	-	nC
C_{iss}	input capacitance	$V_{DS} = -10\text{ V}; f = 1\text{ MHz}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	785	-	pF
C_{oss}	output capacitance		-	63	-	pF
C_{rss}	reverse transfer capacitance		-	53	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10\text{ V}; I_D = -3.4\text{ A}; V_{GS} = -5\text{ V}; R_{G(ext)} = 6\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}$	-	4	-	ns
t_r	rise time		-	14	-	ns
$t_{d(off)}$	turn-off delay time		-	40	-	ns
t_f	fall time		-	16	-	ns
TR2 (P-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	$I_S = -1.2\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	-0.8	-1.2	V

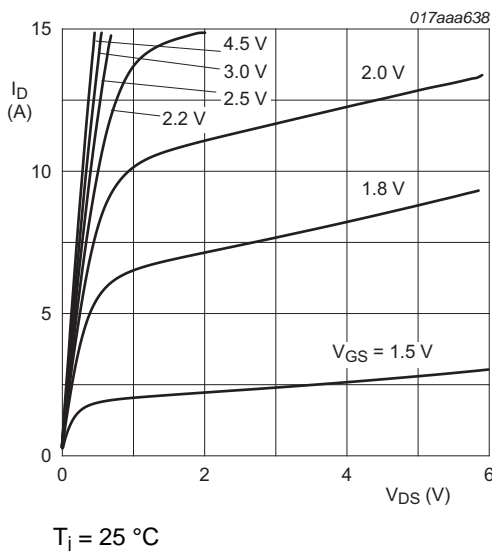


Fig 5. TR1: Output characteristics: drain current as a function of drain-source voltage; typical values

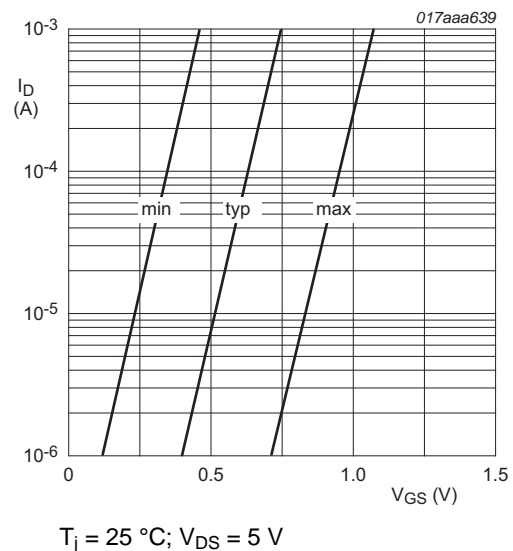


Fig 6. TR1: Sub-threshold drain current as a function of gate-source voltage

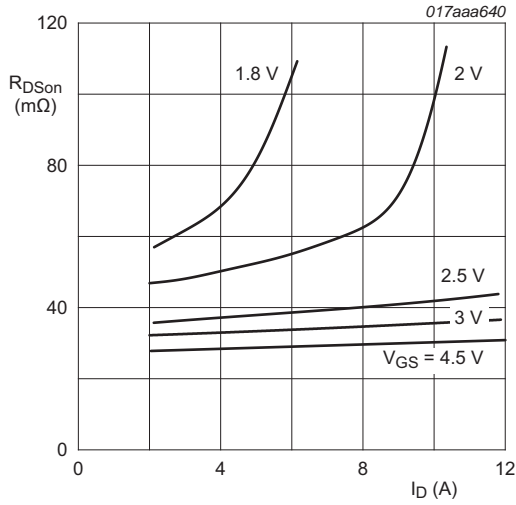


Fig 7. TR1: Drain-source on-state resistance as a function of drain current; typical values

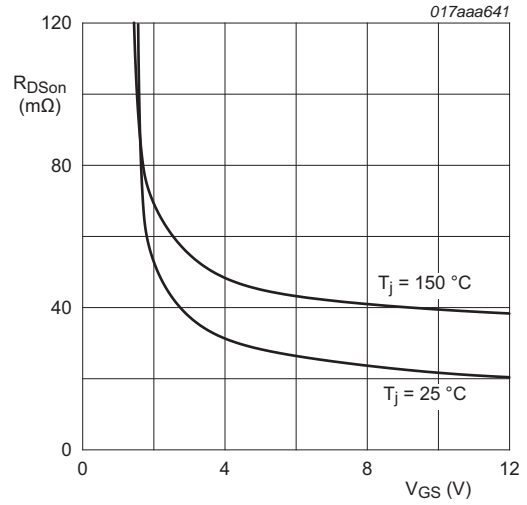


Fig 8. TR1: Drain-source on-state resistance as a function of gate-source voltage; typical values

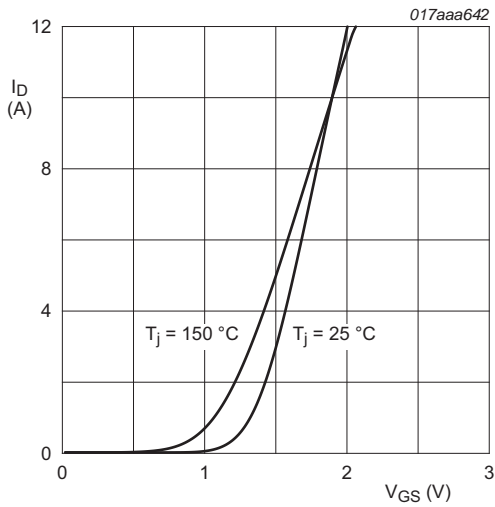


Fig 9. TR1: Transfer characteristics: drain current as a function of gate-source voltage; typical values

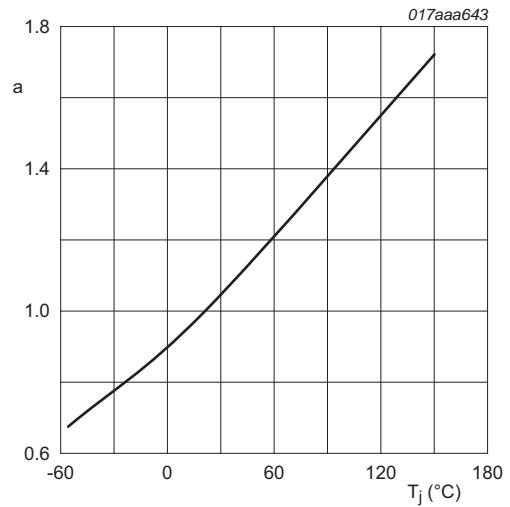
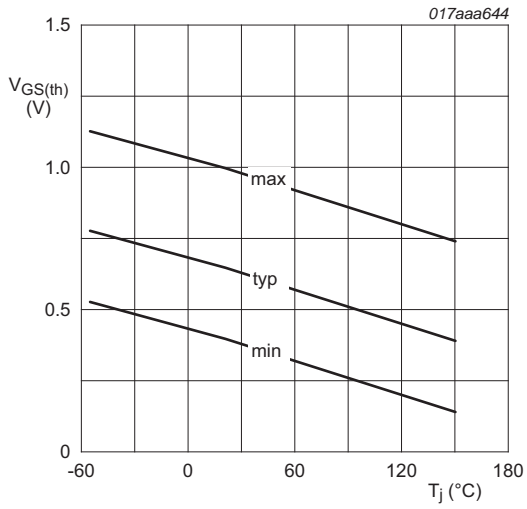
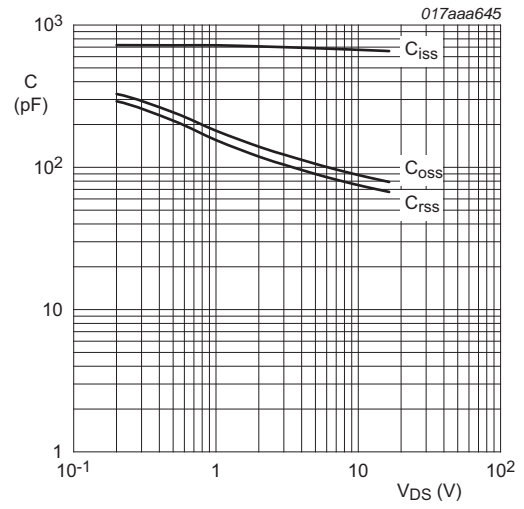


Fig 10. TR1: Normalized drain-source on-state resistance as a function of junction temperature; typical values



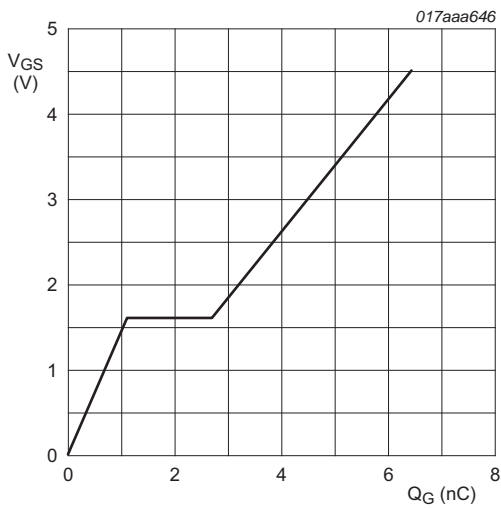
$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$

Fig 11. TR1: Gate-source threshold voltage as a function of junction temperature



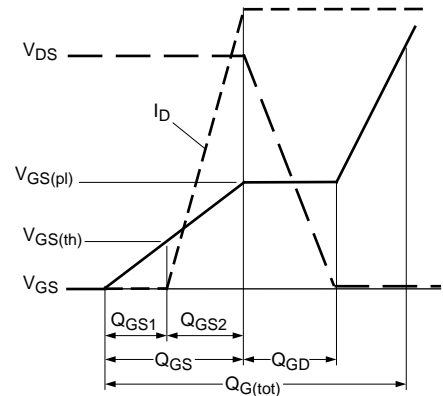
$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

Fig 12. TR1: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 3 \text{ A}; V_{DS} = 10 \text{ V}; T_{amb} = 25 \text{ °C}$

Fig 13. TR1: Gate-source voltage as a function of gate charge; typical values



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Fig 14. Gate charge waveform definitions

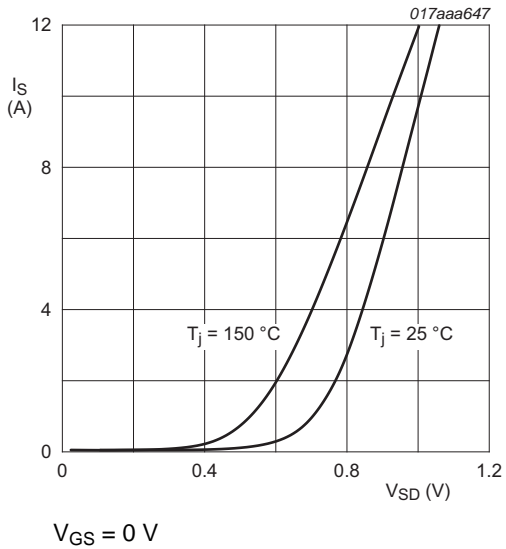


Fig 15. TR1: Source current as a function of source-drain voltage; typical values

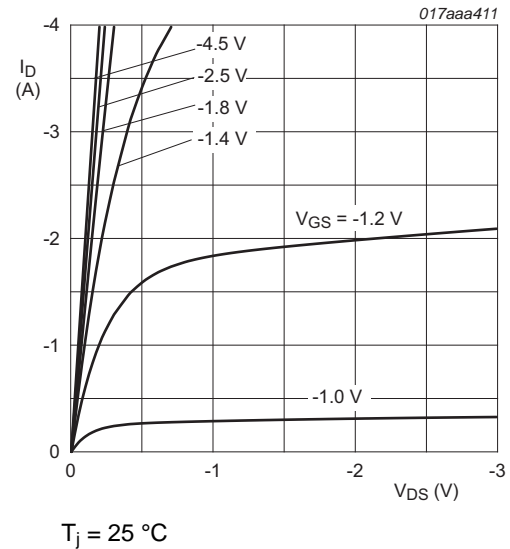
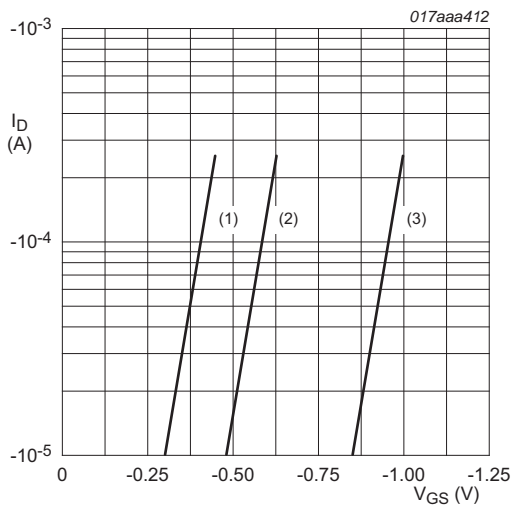


Fig 16. TR2: Output characteristics: drain current as a function of drain-source voltage; typical values



$T_j = 25\text{ °C}; V_{DS} = -5\text{ V}$
 (1) minimum values
 (2) typical values
 (3) maximum values

Fig 17. TR2: Sub-threshold drain current as a function of gate-source voltage

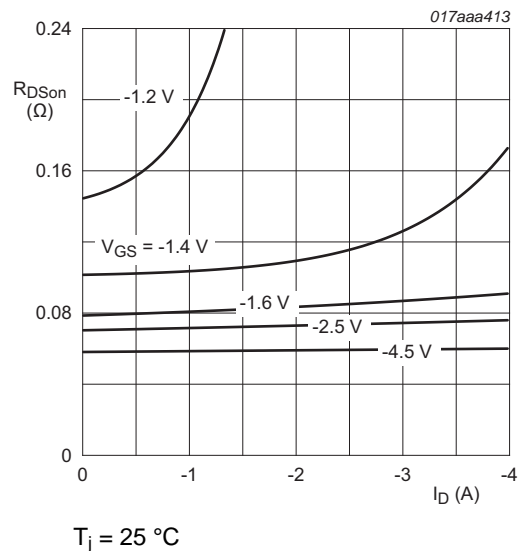
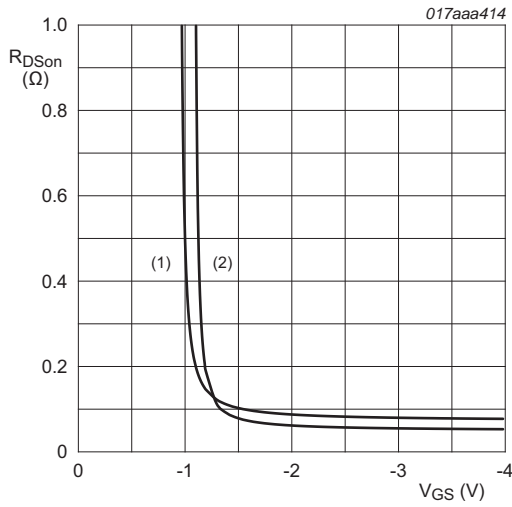
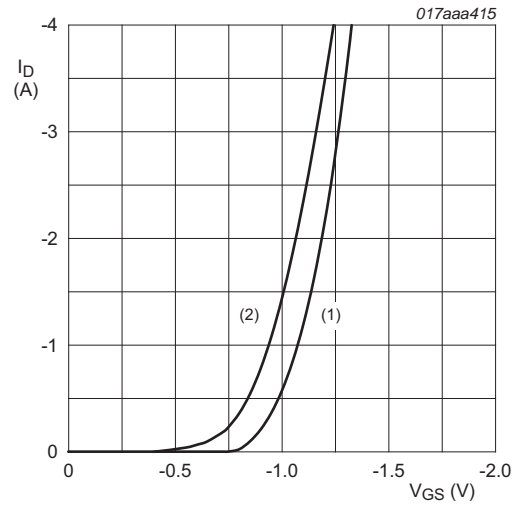


Fig 18. TR2: Drain-source on-state resistance as a function of drain current; typical values



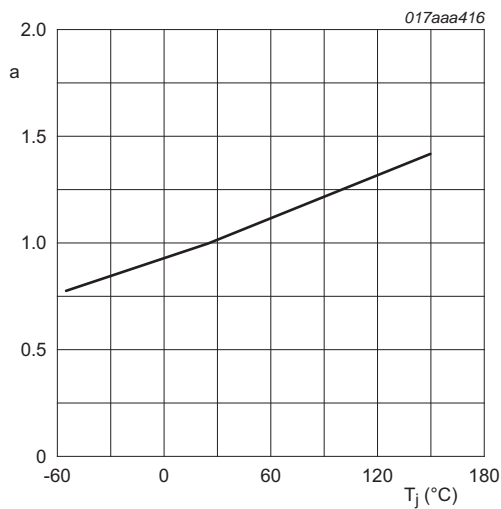
$I_D = -1\text{ A}$
 (1) $T_j = 150\text{ °C}$
 (2) $T_j = 25\text{ °C}$

Fig 19. TR2: Drain-source on-state resistance as a function of gate-source voltage; typical values



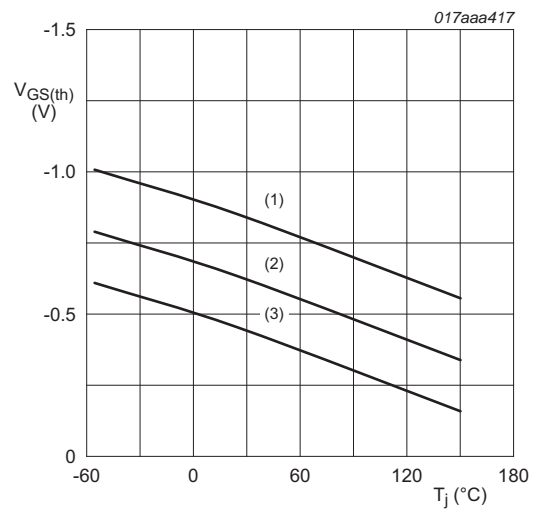
$V_{DS} > I_D \times R_{DS(on)}$
 (1) $T_j = 25\text{ °C}$
 (2) $T_j = 150\text{ °C}$

Fig 20. TR2: Transfer characteristics: drain current as a function of gate-source voltage; typical values



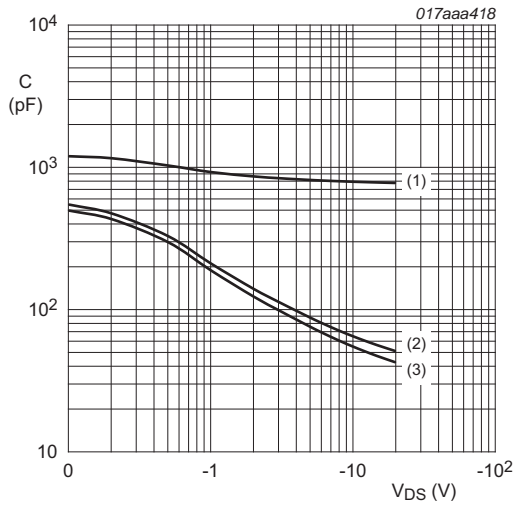
$$\alpha = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 21. TR2: Normalized drain-source on-state resistance as a function of junction temperature; typical values



$I_D = -0.25\text{ mA}; V_{DS} = V_{GS}$
 (1) maximum values
 (2) typical values
 (3) minimum values

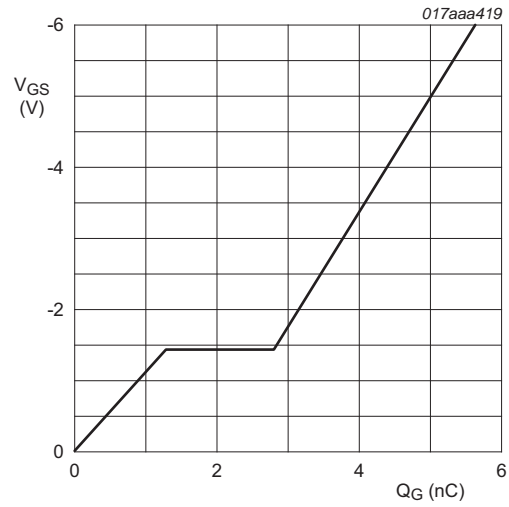
Fig 22. TR2: Gate-source threshold voltage as a function of junction temperature



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

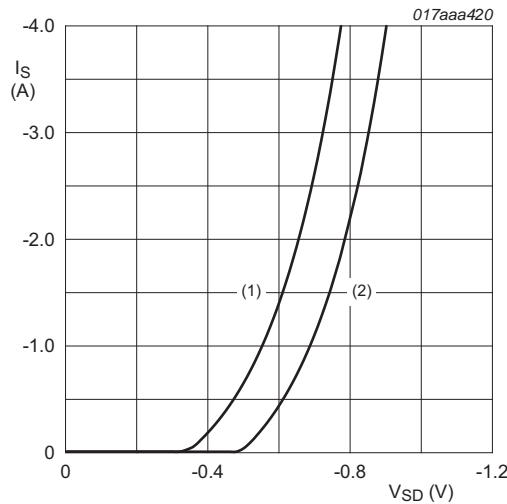
- (1) C_{iss}
- (2) C_{oss}
- (3) C_{rss}

Fig 23. TR2: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = -3.3 \text{ A}; V_{DS} = -10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig 24. TR2: Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0 \text{ V}$

- (1) $T_{amb} = 150 \text{ }^\circ\text{C}$
- (2) $T_{amb} = 25 \text{ }^\circ\text{C}$

Fig 25. TR2: Source current as a function of source-drain voltage; typical values

8. Test information

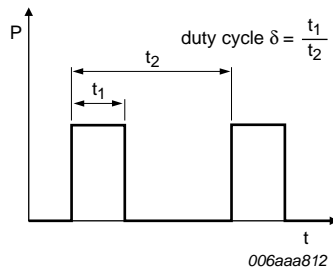


Fig 26. Duty cycle definition

9. Package outline

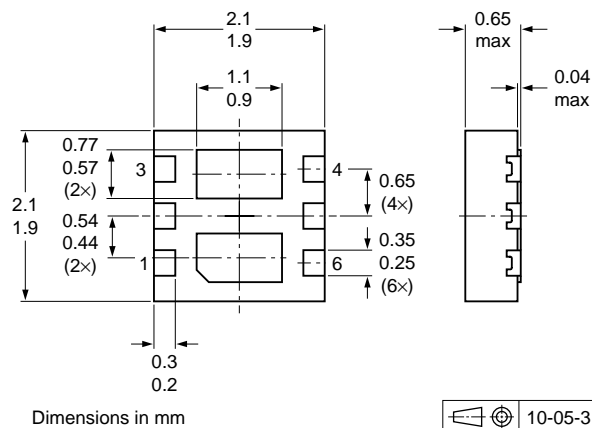


Fig 27. DFN2020-6 (SOT1118)

10. Soldering

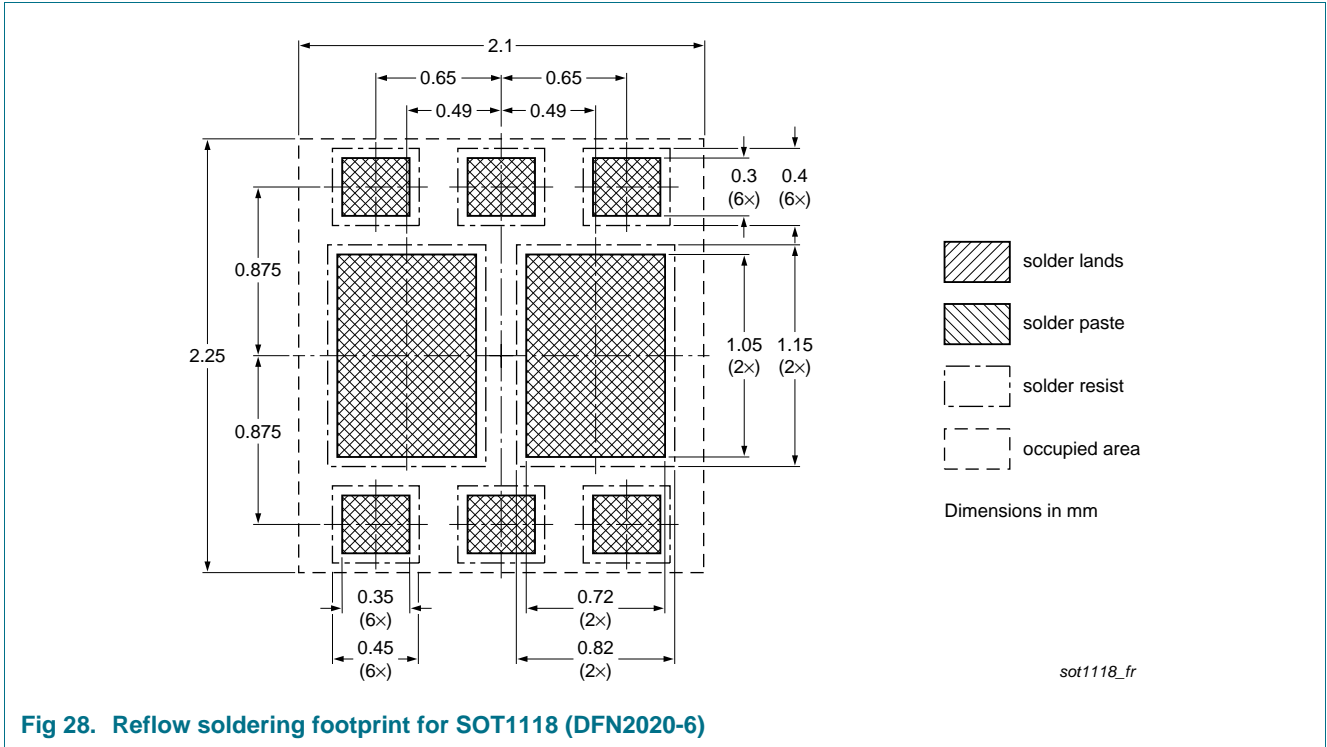


Fig 28. Reflow soldering footprint for SOT1118 (DFN2020-6)

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMCPB5530X v.1	20120626	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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