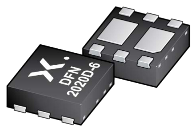

PMDPB56XNEA

30 V, dual N-channel Trench MOSFET

19 April 2016 Product data sheet

1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a small and leadless DFN2020D-6 (SOT1118D) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Low threshold voltage
- Leadless medium power SMD plastic package: 2 × 2 × 0.65 mm
- Tin-plated 100 % solderable side pads for optical solder inspection
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- AEC-Q101 qualified

3. Applications

- LED driver
- Power management
- Low-side loadswitch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	30	V
V_{GS}	gate-source voltage			-12	-	12	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C	[1]	-	-	3.1	A
Static characteristics (per transistor)							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 3.1 A; T_j = 25 °C		-	55	72	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

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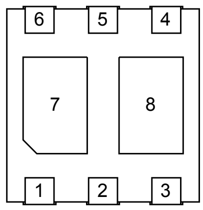
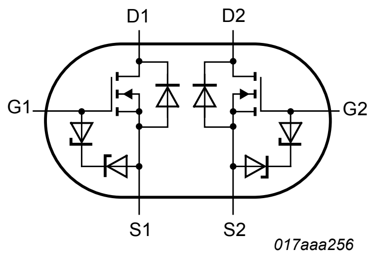
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 Transparent top view **DFN2020D-6 (SOT1118D)**	
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDPB56XNEA	DFN2020D-6	DFN2020D-6: plastic, thermally enhanced ultra thin and small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118D

7. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB56XNEA	3A

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	T_j = 25 °C		-	30	V
V_{GS}	gate-source voltage			-12	12	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C	[1]	-	3.1	A
		V_{GS} = 4.5 V; T_{amb} = 100 °C	[1]	-	2	A
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	12	A
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 0.3 A; $T_{j(init)}$ = 25 °C; DUT in avalanche (unclamped)		-	6.2	mJ
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	485	mW
			[1]	-	1.15	W
		T_{sp} = 25 °C		-	8.33	W
Per device						
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	1.1	A
ESD Maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[3] Measured between all pins.

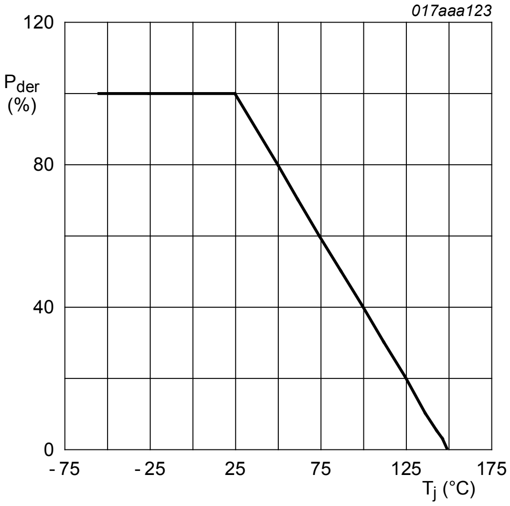


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

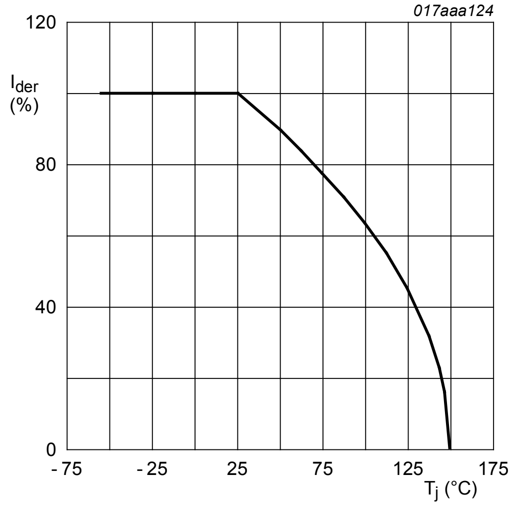


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

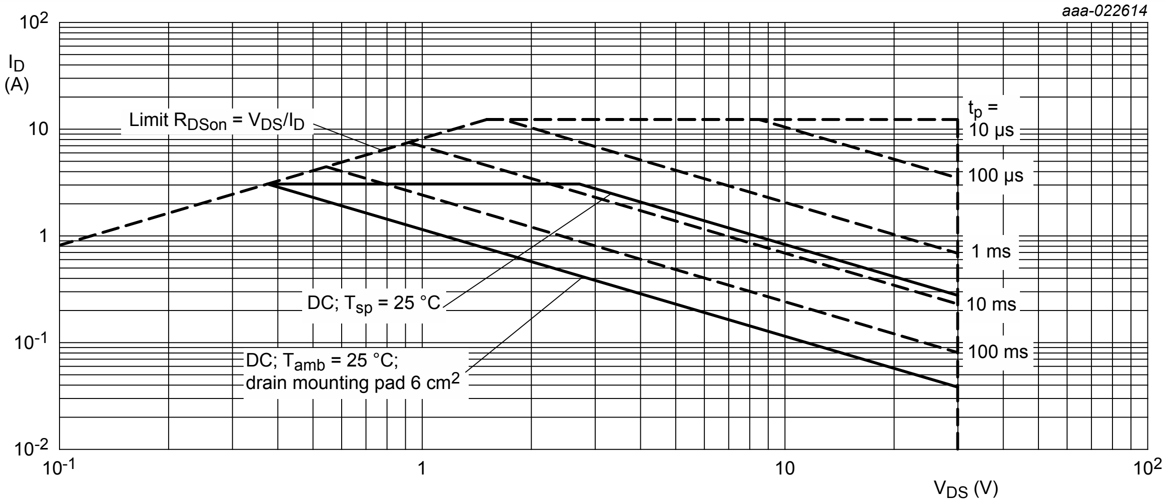


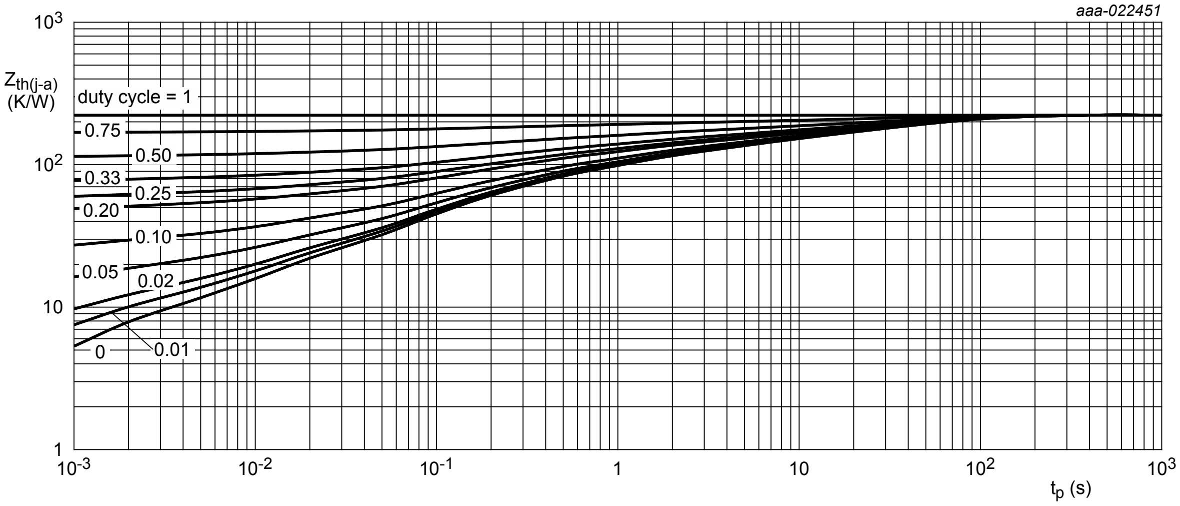
Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

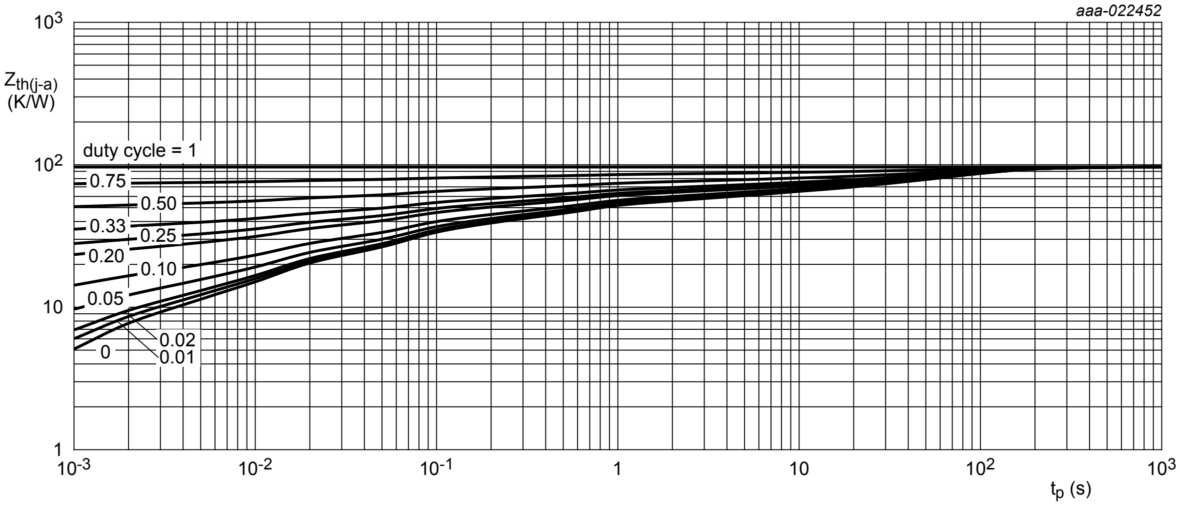
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	224	257	K/W
			[2]	-	96	109	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	12	15	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2.



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



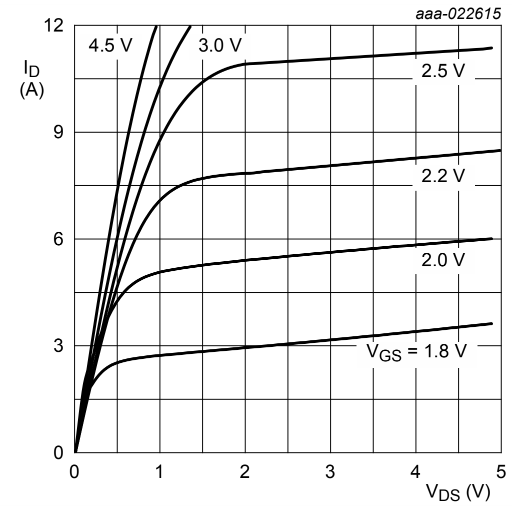
FR4 PCB, mounting pad for drain 6 cm^2

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

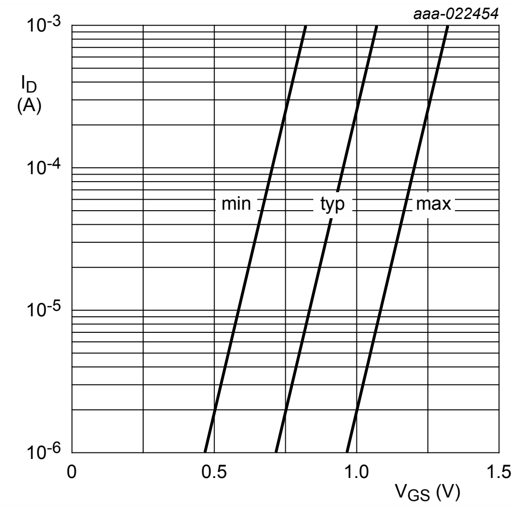
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics (per transistor)							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 μA; V_{GS} = 0 V; T_j = 25 °C		30	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 250 μA; V_{DS}=V_{GS}; T_j = 25 °C		0.75	1	1.25	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	μA
I_{GSS}	gate leakage current	V_{GS} = 12 V; V_{DS} = 0 V; T_j = 25 °C		-	-	10	μA
		V_{GS} = -12 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-10	μA
		V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	2	μA
		V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-2	μA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 3.1 A; T_j = 25 °C		-	55	72	mΩ
		V_{GS} = 4.5 V; I_D = 3.1 A; T_j = 150 °C		-	92	121	mΩ
		V_{GS} = 2.5 V; I_D = 2.6 A; T_j = 25 °C		-	72	102	mΩ
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 3.1 A; T_j = 25 °C		-	12	-	S
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		-	9.2	-	Ω
Dynamic characteristics (per transistor)							
$Q_{G(tot)}$	total gate charge	V_{DS} = 15 V; I_D = 3.1 A; V_{GS} = 4.5 V; T_j = 25 °C		-	2.9	5	nC
Q_{GS}	gate-source charge			-	0.4	-	nC
Q_{GD}	gate-drain charge			-	0.8	-	nC
C_{iss}	input capacitance	V_{DS} = 15 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	256	-	pF
C_{oss}	output capacitance			-	31	-	pF
C_{rss}	reverse transfer capacitance			-	23	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; I_D = 8 A; V_{GS} = 4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	9	-	ns
t_r	rise time			-	20	-	ns
$t_{d(off)}$	turn-off delay time			-	19	-	ns
t_f	fall time			-	7	-	ns
Source-drain diode (per transistor)							
V_{SD}	source-drain voltage	I_S = 1.1 A; V_{GS} = 0 V; T_j = 25 °C		-	0.7	1.2	V



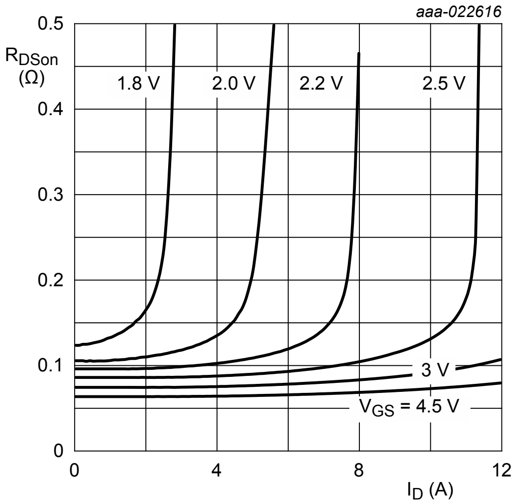
$T_j = 25\ °C$

Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values



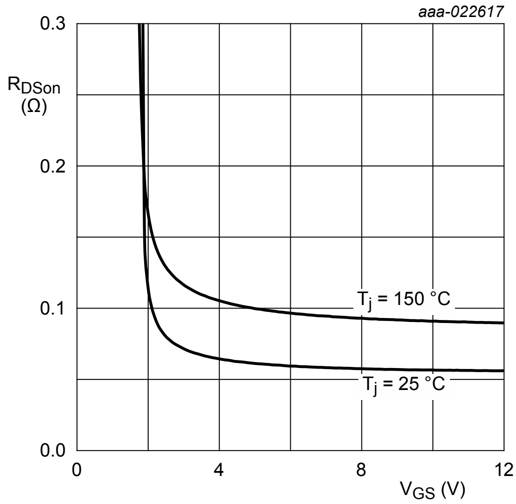
$T_j = 25\ °C$; $V_{DS} = 5\ V$

Fig. 7. Subthreshold drain current as a function of gate-source voltage



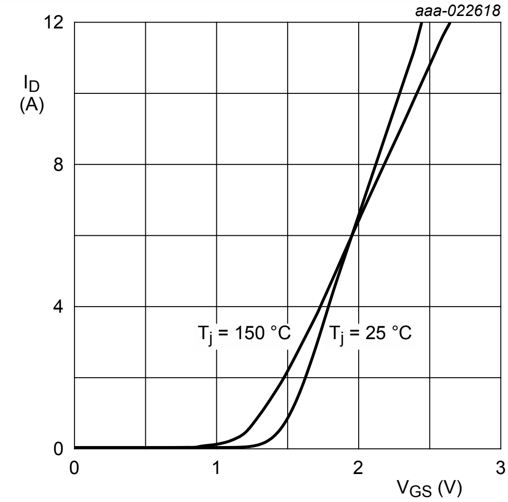
$T_j = 25\ °C$

Fig. 8. Drain-source on-state resistance as a function of drain current; typical values



$I_D = 3.1\ A$

Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



$V_{DS} > I_D \times R_{DSon}$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

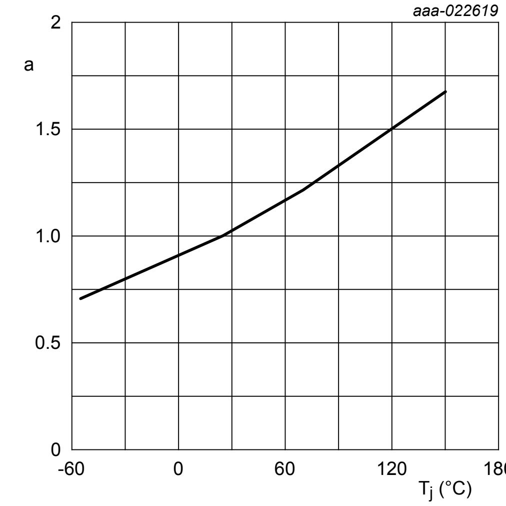
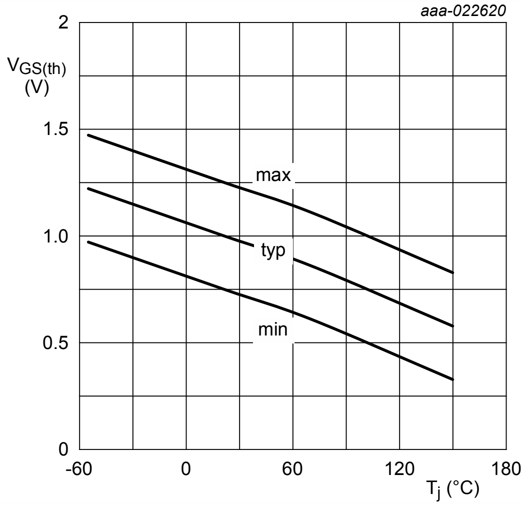


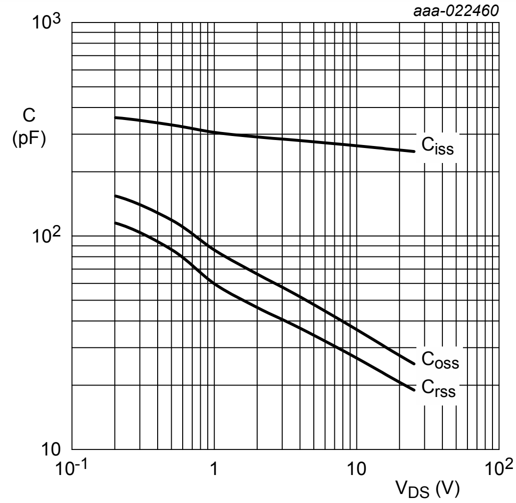
Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$



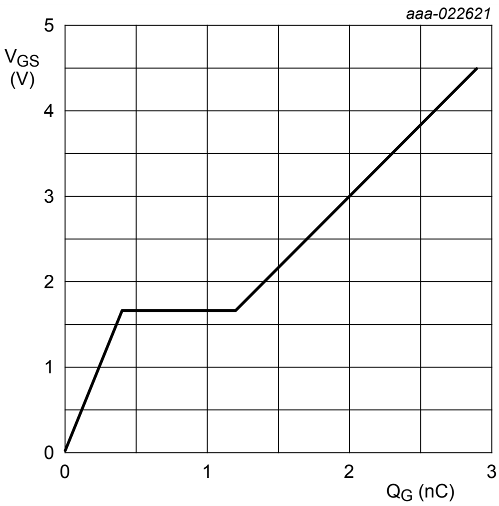
I_D = 0.25 mA; $V_{DS} = V_{GS}$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = 3.1 A; V_{DS} = 15 V; T_{amb} = 25 °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

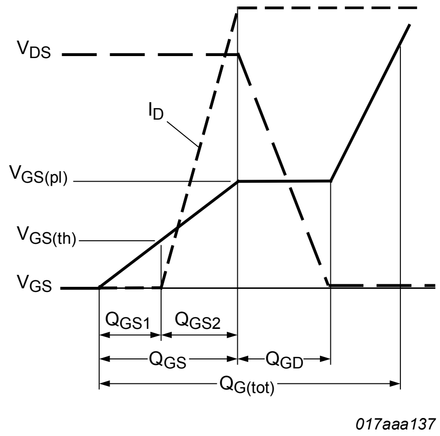
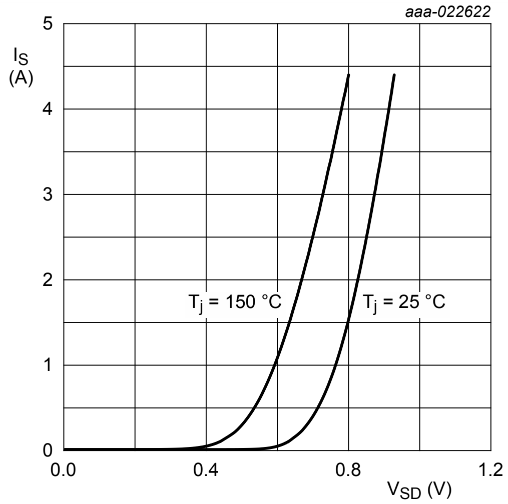


Fig. 15. Gate charge waveform definitions



V_{GS} = 0 V

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

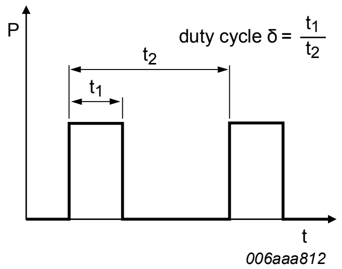


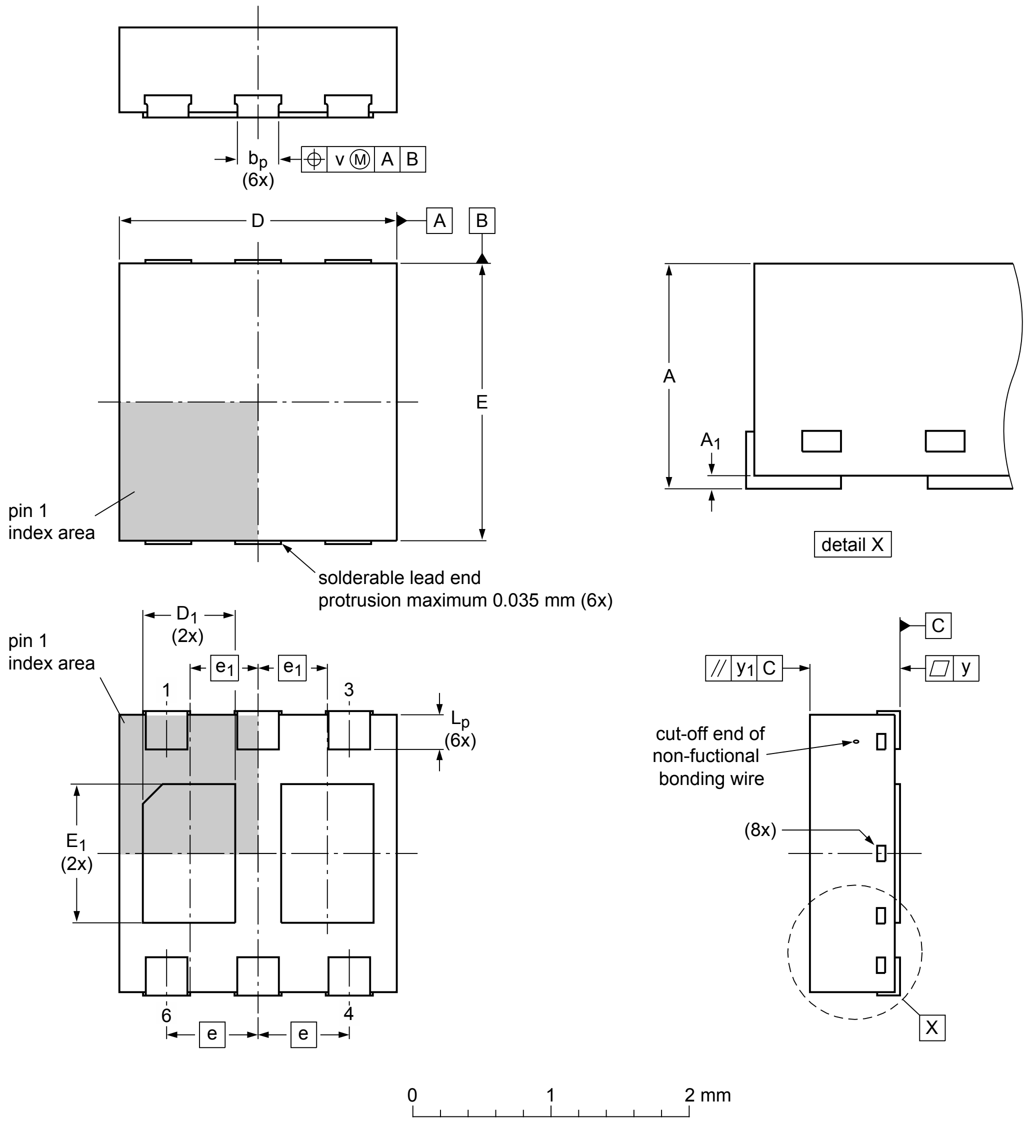
Fig. 17. Duty cycle definition

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

DFN2020D-6: plastic, thermally enhanced ultra thin and small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm **SOT1118D**



Dimensions (mm are the original dimensions)

Unit		A	A1	bp	D	D1	E	E1	e	e1	Lp	v	y	y1
mm	max	0.65	0.04	0.35	2.1	0.77	2.1	1.0		0.54	0.30			
	nom	0.62		0.30	2.0	0.67	2.0	0.9	0.65	0.49	0.25	0.1	0.05	0.05
	min	0.59		0.25	1.9	0.57	1.9	0.8		0.44	0.20			

Note

1. Dimension A is including plating thickness.

sot1118d_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1118D		- - -				~~14-07-16~~ 14-10-16

Fig. 18. Package outline DFN2020D-6 (SOT1118D)

13. Soldering

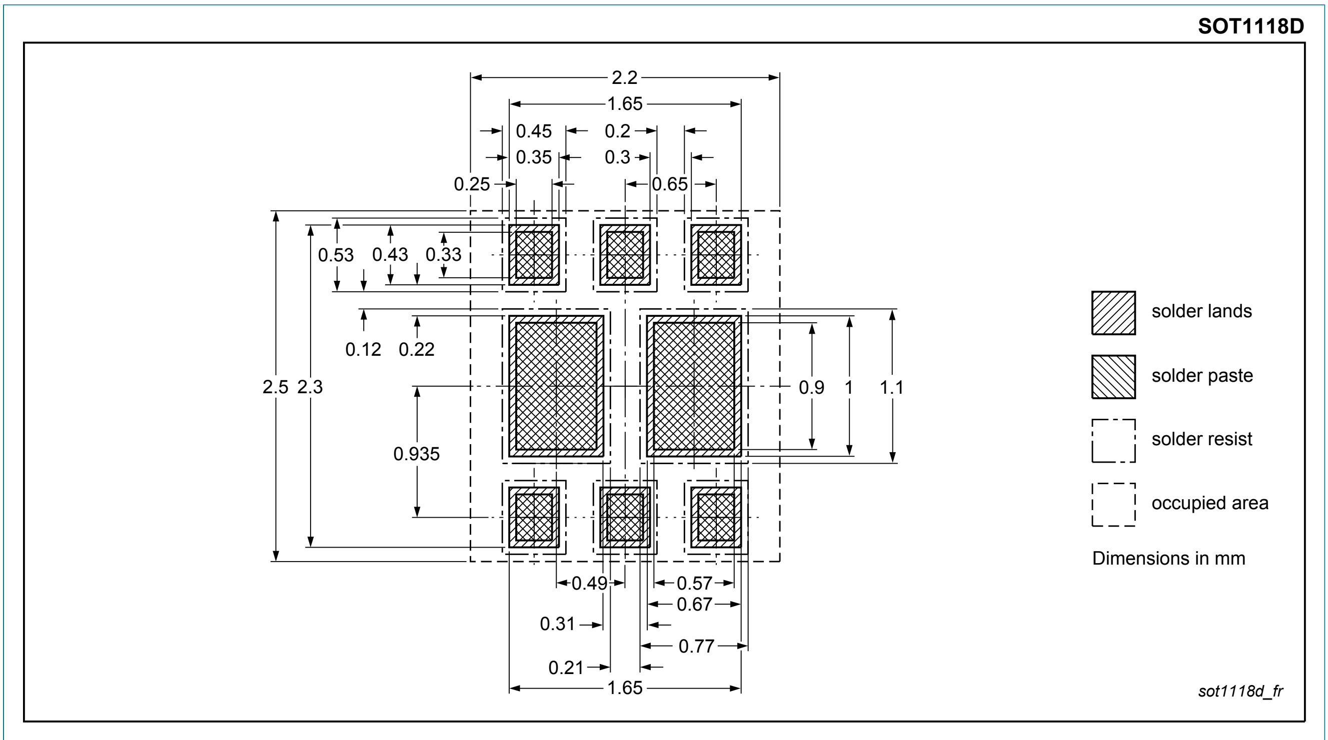


Fig. 19. Reflow soldering footprint for DFN2020D-6 (SOT1118D)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB56XNEA v.1	20160419	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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16. Contents

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Date of release: 19 April 2016

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