PMDPB70XP



30 V, dual P-channel Trench MOSFET

Rev. 1 — 9 March 2012

Product data sheet

1. Product profile

1.1 General description

Dual P-channel enhancement mode Field-Effect Transistor (FET) in a small and leadless ultra thin SOT1118 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Very fast switching
- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction

1.3 Applications

- Charging switch for portable devices
- DC/DC converters
- Small brushless DC motor drive
- Power management in battery-driven portables
- Hard disc and computing power management

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transisto	or						
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	-30	V
V_{GS}	gate-source voltage			-12	-	12	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C; t ≤ 5 s	[1]	-	-	-3.8	Α
Static chara	cteristics (per transistor)						
R _{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -2.9 A; T_j = 25 °C		-	70	87	mΩ

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1		D4
2	G1	gate TR1	6 5 4	D1 D2
3	D2	drain TR2		
4	S2	source TR2	7 8	
5	G2	gate TR2		
6	D1	drain TR1	1 2 3	G1 S1 S2 G2
7	D1	drain TR1	Transparent top view	017aaa258
8	D2	drain TR2	SOT1118 (HUSON6)	

3. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PMDPB70XP	HUSON6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1118			

4. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB70XP	1H

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transiste	or					
V_{DS}	drain-source voltage	T _j = 25 °C		-	-30	V
V_{GS}	gate-source voltage			-12	12	V
I_D	drain current	$V_{GS} = -4.5 \text{ V}; T_{amb} = 25 \text{ °C}; t \le 5 \text{ s}$	<u>[1]</u>	-	-3.8	Α
		V _{GS} = -4.5 V; T _{amb} = 25 °C	<u>[1]</u>	-	-2.9	Α
		V _{GS} = -4.5 V; T _{amb} = 100 °C	<u>[1]</u>	-	-1.9	Α
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	-11.6	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	490	mW
			<u>[1]</u>	-	1170	mW
		T _{sp} = 25 °C		-	8300	mW
Source-drain	n diode					
I _S	source current	T _{amb} = 25 °C	<u>[1]</u>	-	-1.2	Α
Per device						
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

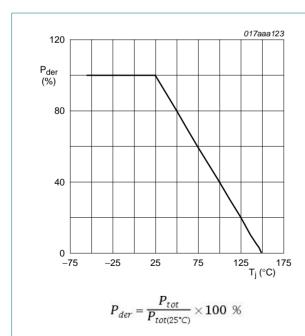


Fig 1. Normalized total power dissipation as a function of junction temperature

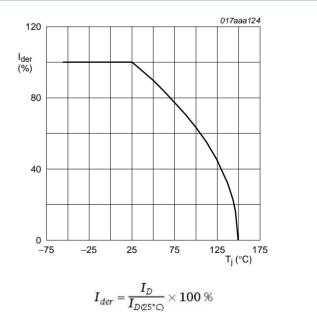
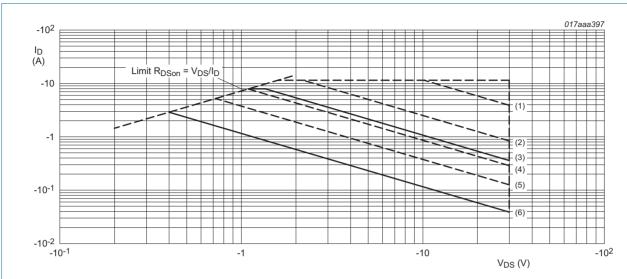


Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} = single pulse

- (1) $t_0 = 10 \mu s$
- (2) $t_p = 100 \mu s$
- (3) DC; $T_{sp} = 25 \, ^{\circ}C$
- $(4) t_p = 10 \text{ ms}$
- $(5) t_p = 100 \text{ ms}$
- (6) DC; T_{amb} = 25 °C; drain mounting pad 6 cm²

Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

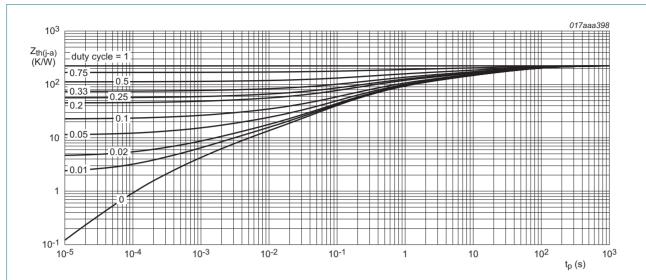
6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	<u>[1]</u>	-	223	256	K/W
			[2]	-	93	107	K/W
		in free air; t ≤ 5 s	[2]	-	55	63	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point	in free air		-	10	15	K/W

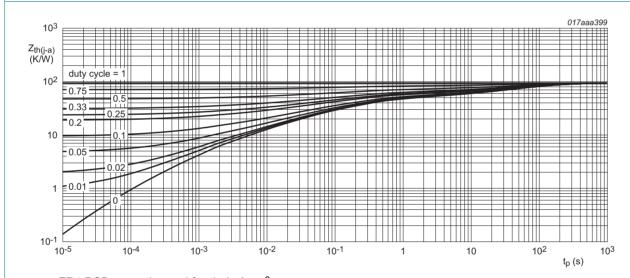
^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

^[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².



FR4 PCB, standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm²

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics (per transistor)					
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 μ A; V_{GS} = 0 V; T_j = 25 °C	-30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 °C$	-0.45	-0.7	-1	V
I _{DSS}	drain leakage current	V_{DS} = -30 V; V_{GS} = 0 V; T_j = 25 °C	-	-	-1	μΑ
		V_{DS} = -30 V; V_{GS} = 0 V; T_j = 150 °C	-	-	-10	μΑ
I _{GSS}	gate leakage current	V_{GS} = 12 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -12 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -2.9 A; T_j = 25 °C	-	70	87	mΩ
		V_{GS} = -4.5 V; I_{D} = -2.9 A; T_{j} = 150 °C	-	110	137	mΩ
		V_{GS} = -2.5 V; I_D = -1.6 A; T_j = 25 °C	-	89	110	mΩ
9fs	forward transconductance	V_{DS} = -10 V; I_{D} = -2.9 A; T_{j} = 25 °C	-	10	-	S
Dynamic ch	naracteristics (per transist	or)				
Q _{G(tot)}	total gate charge	$V_{DS} = -15 \text{ V}; I_D = -2.9 \text{ A}; V_{GS} = -5 \text{ V};$	-	5.2	7.8	nC
Q_{GS}	gate-source charge	T _j = 25 °C	-	1.1	-	nC
Q_{GD}	gate-drain charge		-	0.95	-	nC
C _{iss}	input capacitance	$V_{DS} = -15 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V};$	-	680	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	54	-	pF
C _{rss}	reverse transfer capacitance		-	40	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = -15 V; I_{D} = -2.9 A; V_{GS} = -5 V;	-	3	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	15	-	ns
$t_{d(off)}$	turn-off delay time		-	112	-	ns
t _f	fall time		-	48	-	ns
Source-dra	in diode (per transistor)					
V_{SD}	source-drain voltage	$I_S = -1.2 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_i = 25 ^{\circ}\text{C}$	-	-0.8	-1.2	V

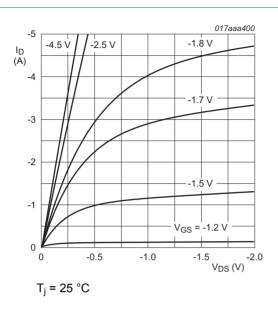


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

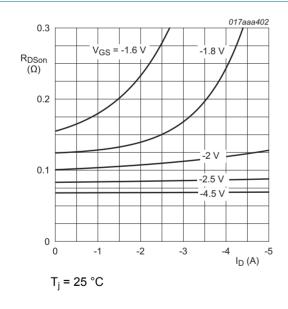
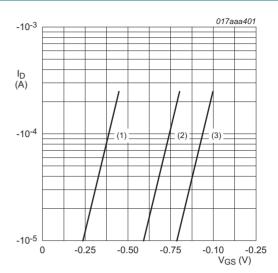


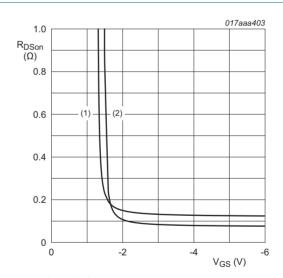
Fig 8. Drain-source on-state resistance as a function of drain current; typical values



 $T_i = 25 \,^{\circ}\text{C}; \, V_{DS} = -5 \,^{\circ}\text{V}$

- (1) minimum values
- (2) typical values
- (3) maximum values

Fig 7. Sub-threshold drain current as a function of gate-source voltage

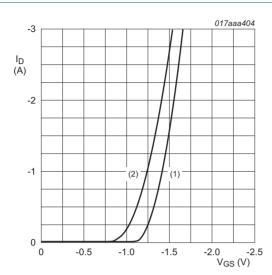


 $I_{D} = -1 A$

(1) $T_j = 150 \, ^{\circ}C$

(2) $T_i = 25 \,^{\circ}C$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

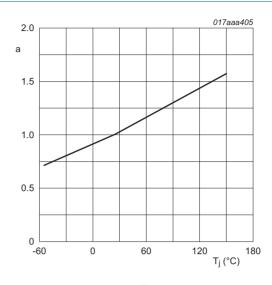


 $V_{DS} > I_D \times R_{DSon}$

(1) $T_i = 25$ °C

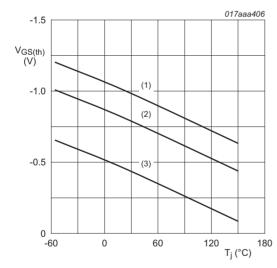
(2) $T_j = 150 \, ^{\circ}\text{C}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



 $a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$

Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



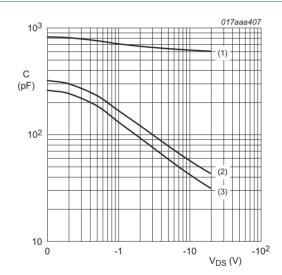
 $I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$

(1) maximum values

(2) typical values

(3) minimum values

Fig 12. Gate-source threshold voltage as a function of junction temperature



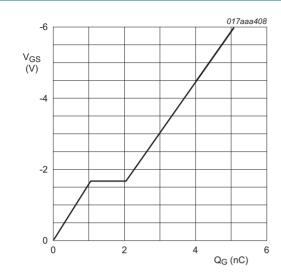
 $f = 1 MHz; V_{GS} = 0 V$

(1) C_{iss}

(2) Coss

(3) C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



 $I_D = -3.3 \text{ A}; V_{DS} = -10 \text{ V}; T_{amb} = 25 ^{\circ}\text{C}$

Fig 14. Gate-source voltage as a function of gate charge; typical values

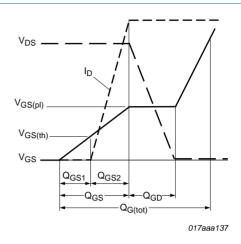
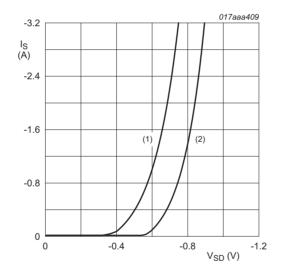


Fig 15. Gate charge waveform definitions



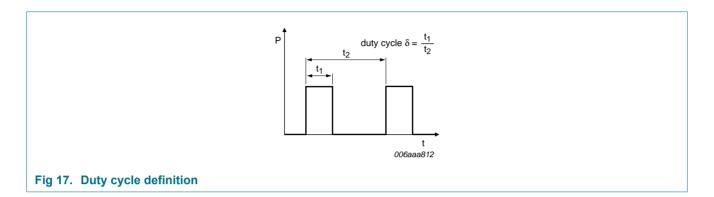
 $V_{GS} = 0 V$

(1) $T_{amb} = 150 \, ^{\circ}C$

(2) $T_{amb} = 25 \, ^{\circ}C$

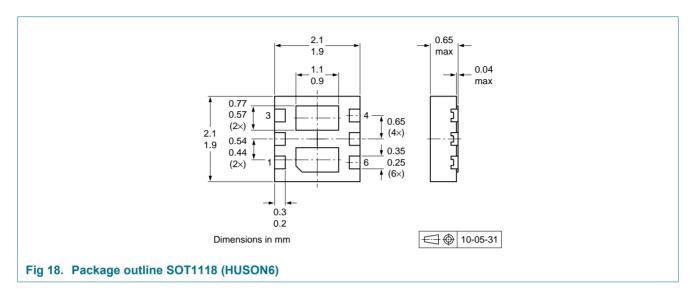
Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information

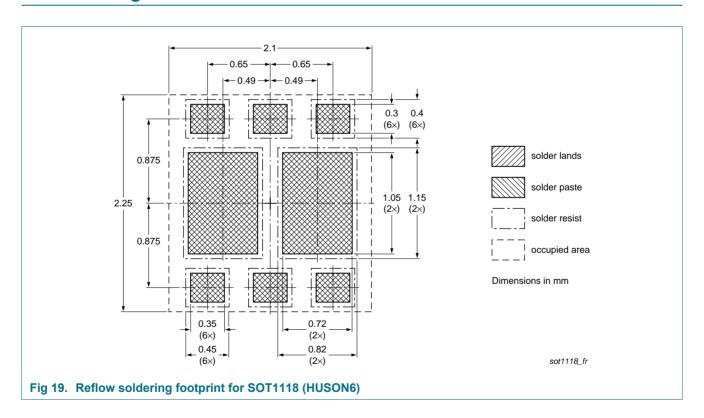


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9. Package outline



10. Soldering





11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB70XP v.1	20120309	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1] [2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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