



# PMDPB70XPE

20 V dual P-channel Trench MOSFET

Rev. 1 — 20 June 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Dual small-signal P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Very fast switching
- Trench MOSFET technology
- 2 kV ElectroStatic Discharge (ESD) protection

### 1.3 Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

### 1.4 Quick reference data

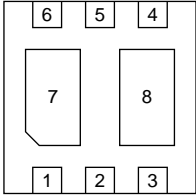
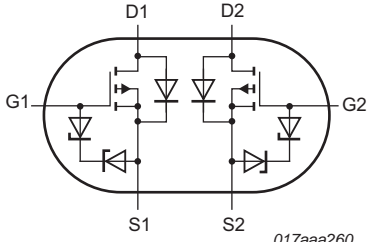
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
$V_{GS}$	gate-source voltage		-12	-	12	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-4.2	A
<b>Static characteristics (per transistor)</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -2\text{ A}; T_j = 25\text{ °C}$	-	66	79	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view</p> <p><b>DFN2020-6 (SOT1118)</b></p>	 <p>017aaa260</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		Description	Version
	Name			
PMDPB70XPE	DFN2020-6		plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1118

## 4. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB70XPE	2B

## 5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

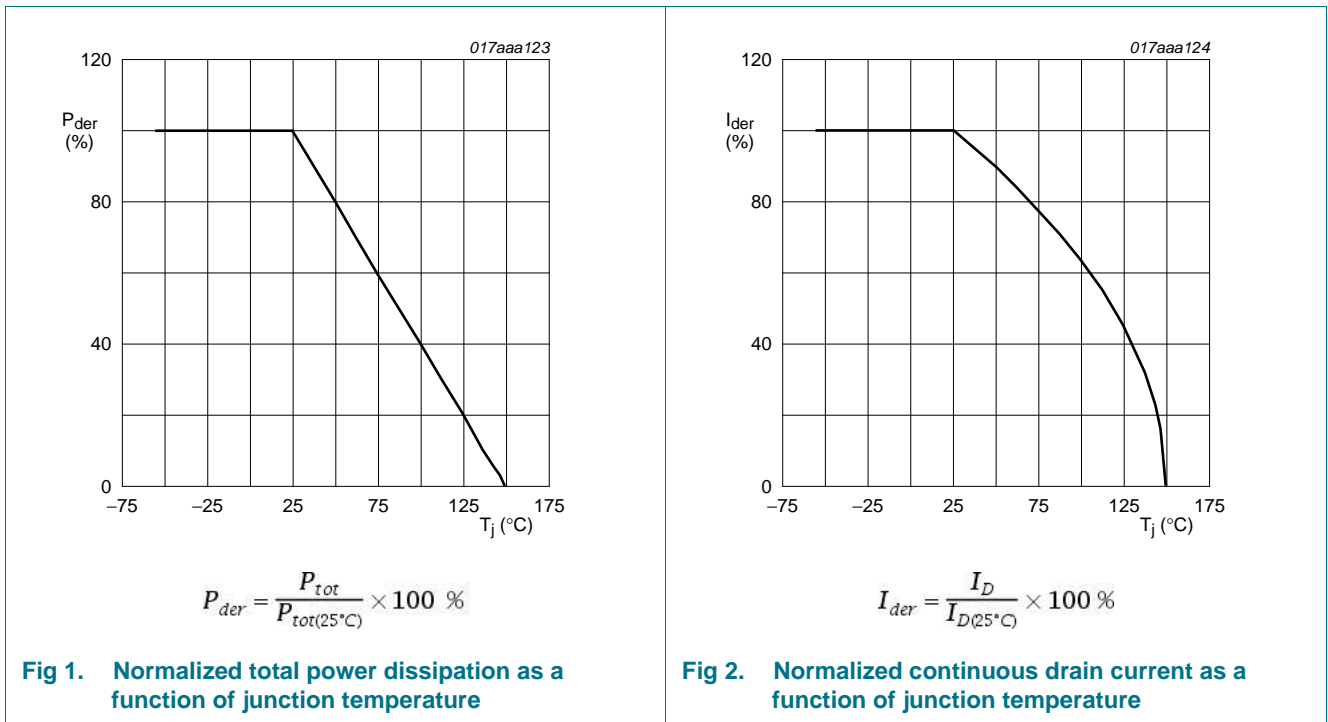
Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-20	V	
$V_{GS}$	gate-source voltage		-12	12	V	
$I_D$	drain current	$V_{GS} = -4.5\text{ V}$ ; $T_{amb} = 25\text{ °C}$ ; $t \leq 5\text{ s}$	[1]	-	-4.2	A
		$V_{GS} = -4.5\text{ V}$ ; $T_{amb} = 25\text{ °C}$	[1]	-	-3	A
		$V_{GS} = -4.5\text{ V}$ ; $T_{amb} = 100\text{ °C}$	[1]	-	-2.1	A
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C}$ ; single pulse; $t_p \leq 10\text{ }\mu\text{s}$	-	-12	A	
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	515	mW
			[1]	-	1210	mW
		$T_{sp} = 25\text{ °C}$		-	8330	mW
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-1.3	A

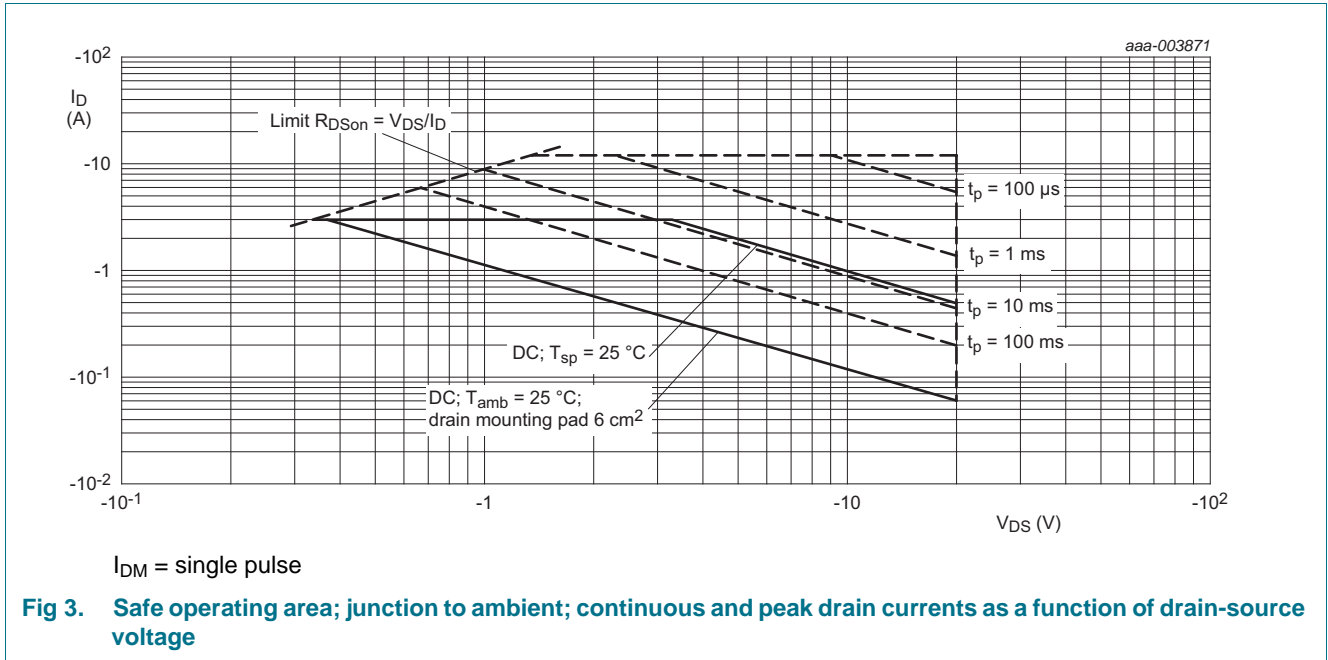
**Table 5. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>ESD maximum rating</b>					
V <sub>ESD</sub>	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ	[3]	-	2000 V
<b>Per device</b>					
T <sub>j</sub>	junction temperature		-55	150	°C
T <sub>amb</sub>	ambient temperature		-55	150	°C
T <sub>stg</sub>	storage temperature		-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.





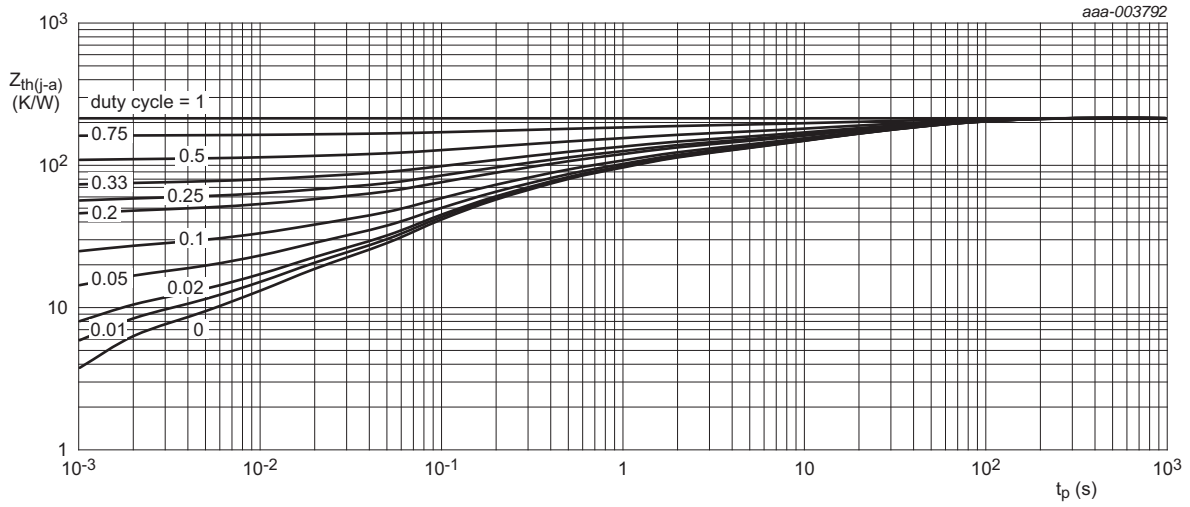
## 6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	212	244	K/W
			[2]	-	90	104	K/W
		in free air; $t \leq 5 \text{ s}$	[2]	-	55	64	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	11	15	K/W	

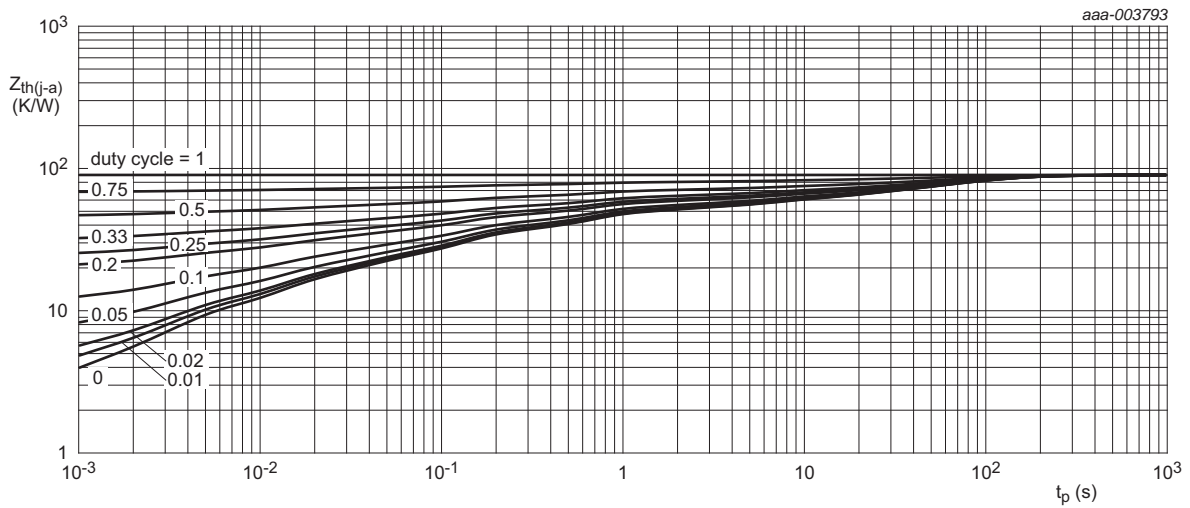
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6 \text{ cm}^2$ .



FR4 PCB, standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



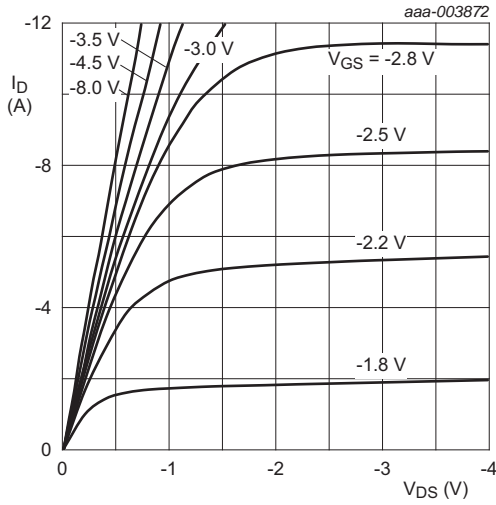
FR4 PCB, mounting pad for drain  $6\text{ cm}^2$

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 7. Characteristics

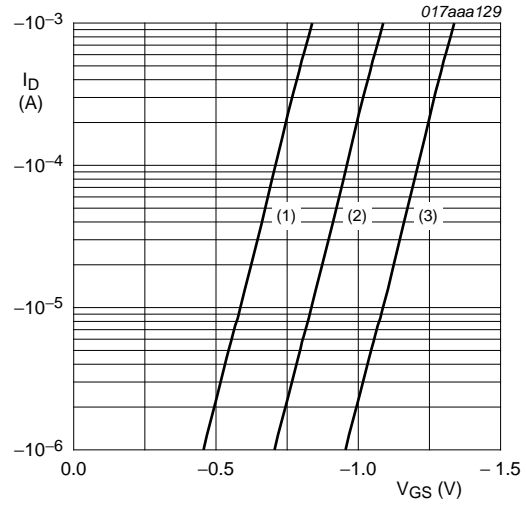
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics (per transistor)</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-0.75	-1	-1.25	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = -20 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	-	-10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 12 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	10	$\mu\text{A}$
		$V_{GS} = -12 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-10	$\mu\text{A}$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}$ ; $I_D = -2 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	66	79	m $\Omega$
		$V_{GS} = -4.5 \text{ V}$ ; $I_D = -2 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	94	112	m $\Omega$
		$V_{GS} = -2.5 \text{ V}$ ; $I_D = -1.5 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	98	123	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 \text{ V}$ ; $I_D = -2 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	7.3	-	S
<b>Dynamic characteristics (per transistor)</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 \text{ V}$ ; $I_D = -2 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	5	7.5	nC
$Q_{GS}$	gate-source charge		-	1.1	-	nC
$Q_{GD}$	gate-drain charge		-	1.1	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -10 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	600	-	pF
$C_{oss}$	output capacitance		-	103	-	pF
$C_{rss}$	reverse transfer capacitance		-	77	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 \text{ V}$ ; $I_D = -2 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $R_{G(ext)} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	7	-	ns
$t_r$	rise time		-	16	-	ns
$t_{d(off)}$	turn-off delay time		-	33	-	ns
$t_f$	fall time		-	15	-	ns
<b>Source-drain diode (per transistor)</b>						
$V_{SD}$	source-drain voltage	$I_S = -0.5 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-0.7	-1.2	V



$T_j = 25\text{ }^\circ\text{C}$

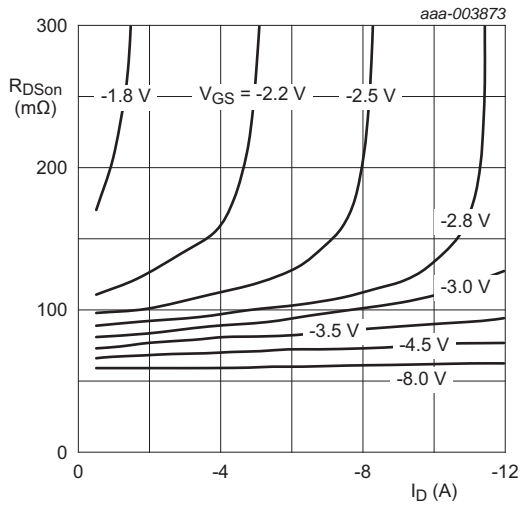
**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



$T_j = 25\text{ }^\circ\text{C}; V_{DS} = -3\text{ V}$

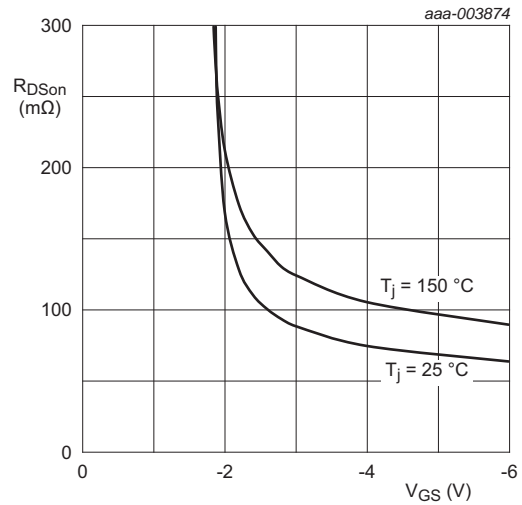
- (1) minimum values
- (2) typical values
- (3) maximum values

**Fig 7. Sub-threshold drain current as a function of gate-source voltage**



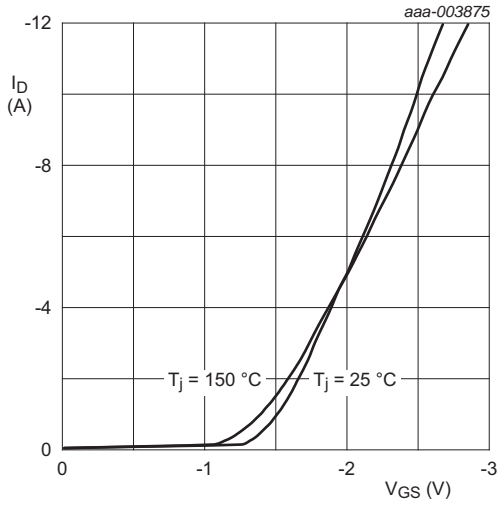
$T_j = 25\text{ }^\circ\text{C}$

**Fig 8. Drain-source on-state resistance as a function of drain current; typical values**



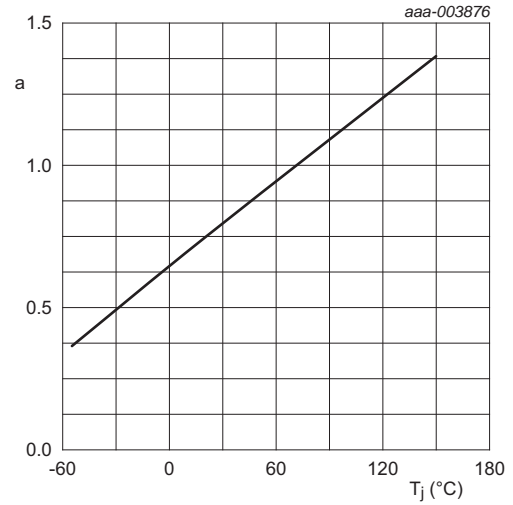
$I_D = -2\text{ A}$

**Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



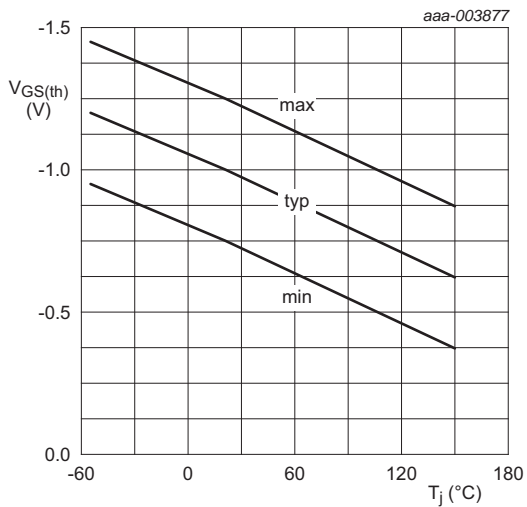
$$V_{DS} > I_D \times R_{DS(on)}$$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



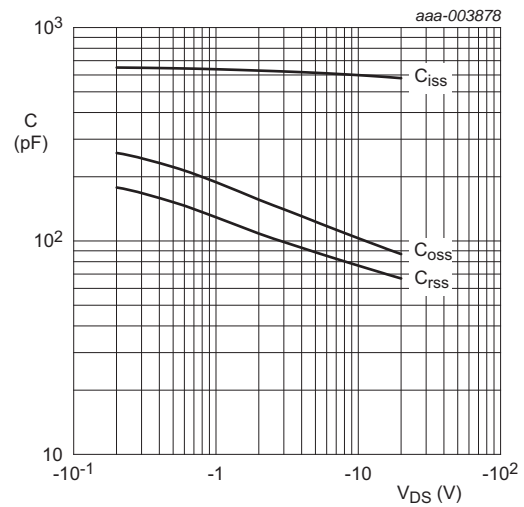
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ C)}}$$

Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



$$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$$

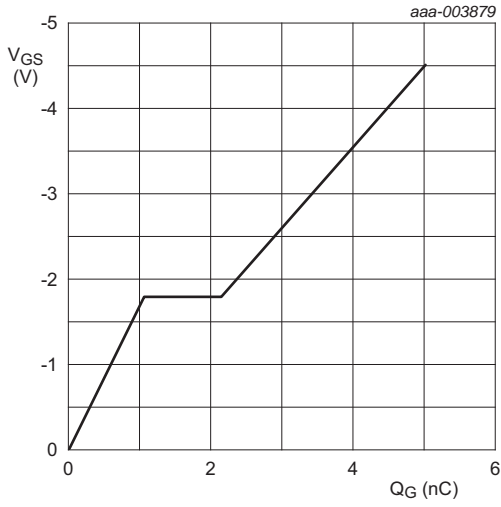
Fig 12. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

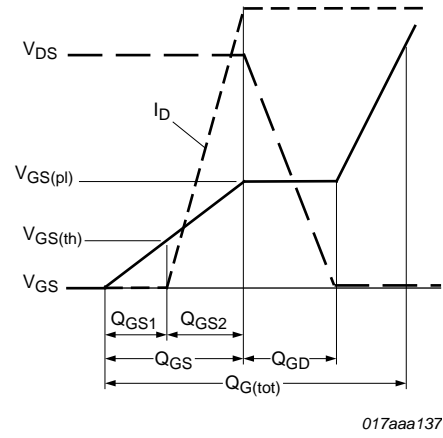
Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



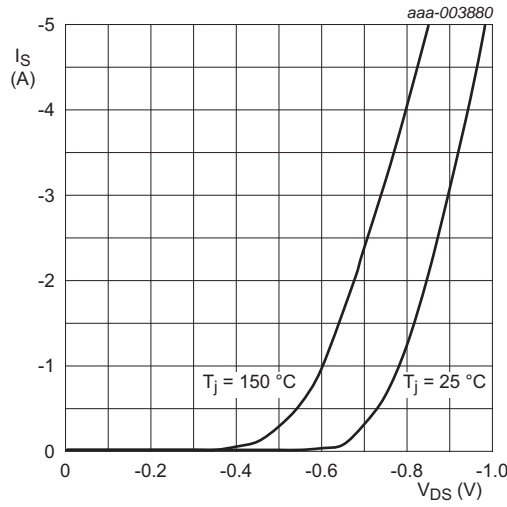


$I_D = -2$  A;  $V_{DS} = -10$  V;  $T_{amb} = 25$  °C

**Fig 14. Gate-source voltage as a function of gate charge; typical values**



**Fig 15. Gate charge waveform definitions**



$V_{GS} = 0$  V

**Fig 16. Source current as a function of source-drain voltage; typical values**

## 8. Test information

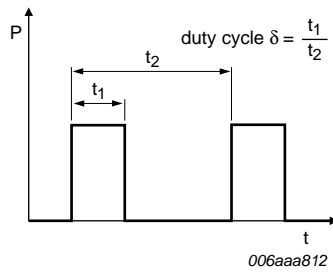


Fig 17. Duty cycle definition

## 9. Package outline

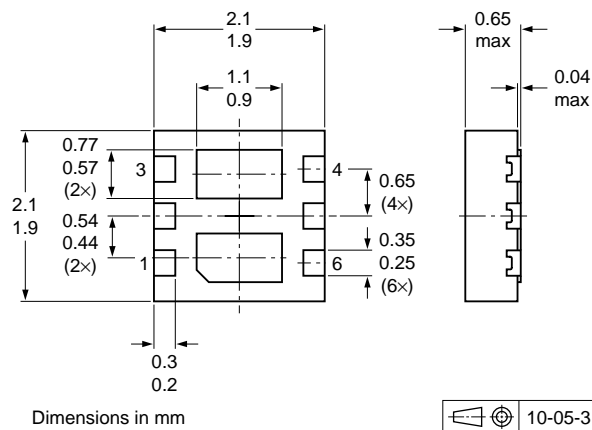
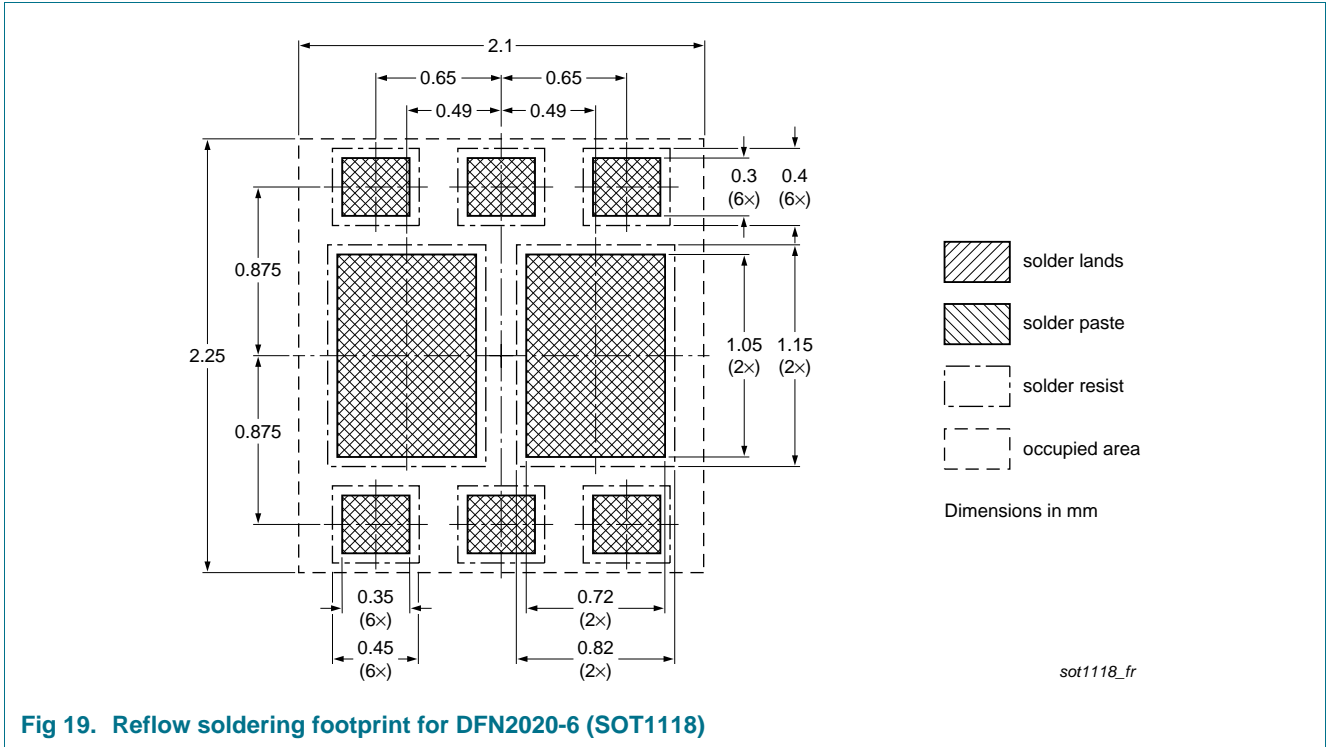


Fig 18. Package outline DFN2020-6 (SOT1118)

**10. Soldering**



**Fig 19. Reflow soldering footprint for DFN2020-6 (SOT1118)**

## 11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB70XPE v.1	20120620	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1]</sup> [2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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