



PMN40ENA

60 V, N-channel Trench MOSFET

11 April 2019

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Extended temperature range $T_j = 175\text{ °C}$
- Trench MOSFET technology
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

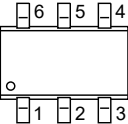
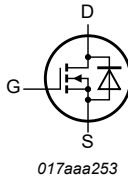
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------|--|-----|-----|-----|------------|
| V_{DS} | drain-source voltage | $T_j = 25\text{ °C}$ | - | - | 60 | V |
| V_{GS} | gate-source voltage | | -20 | - | 20 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$ | [1] | - | 4.2 | A |
| Static characteristics | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 4.2\text{ A}; T_j = 25\text{ °C}$ | - | 32 | 43 | m Ω |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|--|--|
| 1 | D | drain |  <p>SC-74; TSOP6 (SOT457)</p> |  <p>017aaa253</p> |
| 2 | D | drain | | |
| 3 | G | gate | | |
| 4 | S | source | | |
| 5 | D | drain | | |
| 6 | D | drain | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|--------------|--|---------|
| | Name | Description | Version |
| PMN40ENA | SC-74; TSOP6 | plastic, surface-mounted package (SC-74; TSOP6); 6 leads | SOT457 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PMN40ENA | 3N |

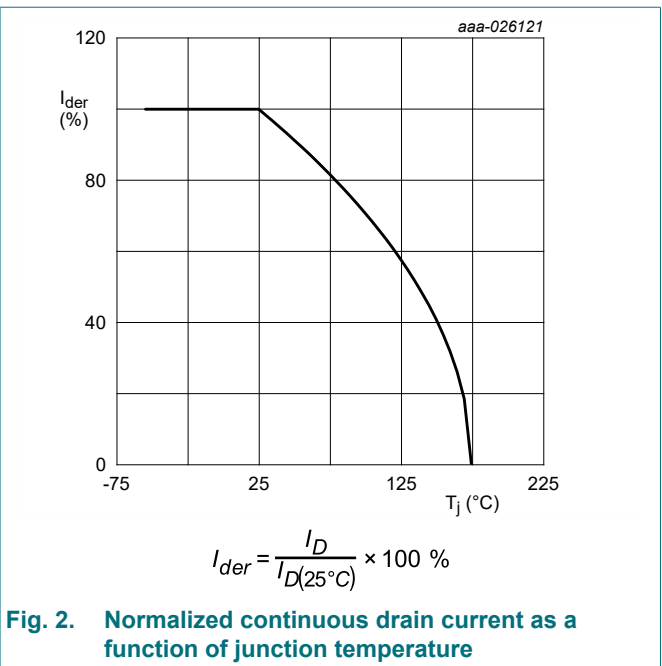
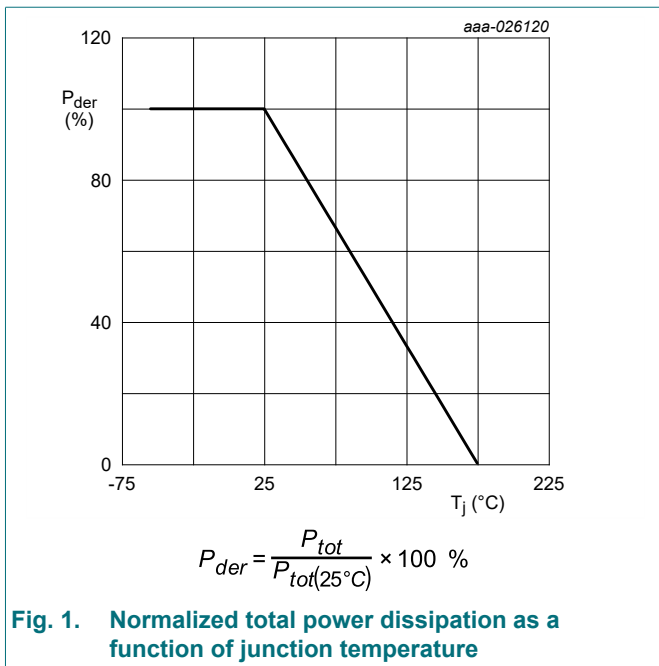
8. Limiting values

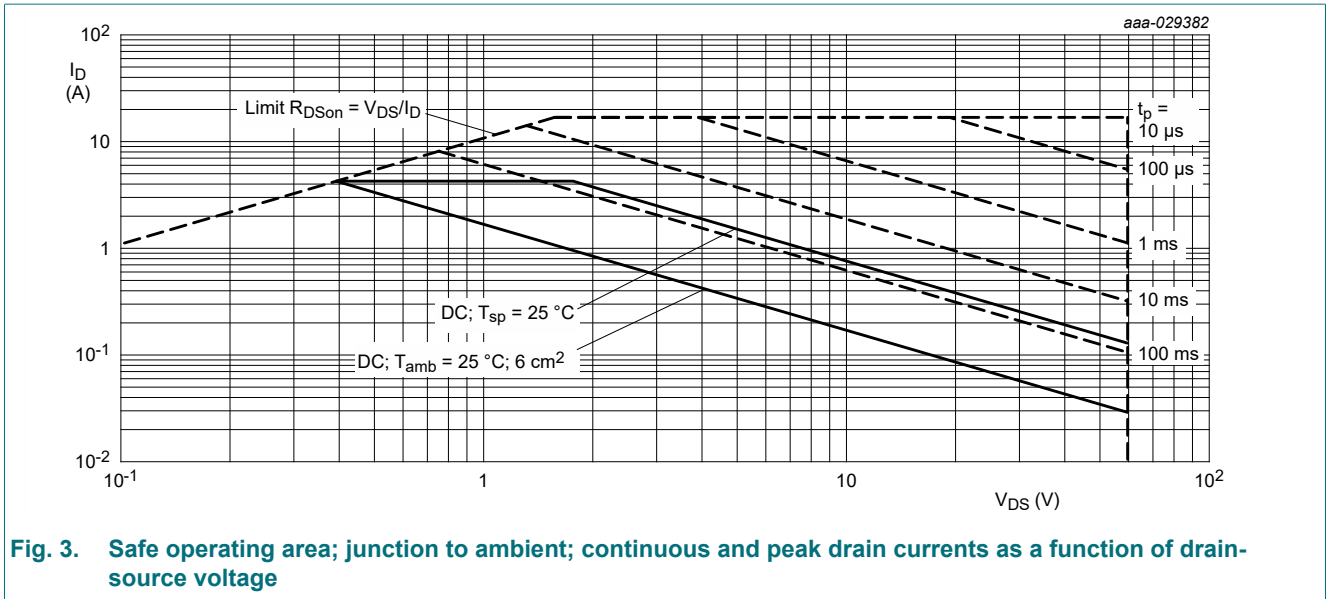
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-----------------------------|--|--|-----|-----|-----|------|
| V _{DS} | drain-source voltage | T _j = 25 °C | | - | 60 | V |
| V _{GS} | gate-source voltage | | | -20 | 20 | V |
| I _D | drain current | V _{GS} = 10 V; T _{amb} = 25 °C | [1] | - | 4.2 | A |
| | | V _{GS} = 10 V; T _{amb} = 100 °C | [1] | - | 3 | A |
| I _{DM} | peak drain current | T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs | | - | 17 | A |
| P _{tot} | total power dissipation | T _{amb} = 25 °C | [2] | - | 652 | mW |
| | | | [1] | - | 1.7 | W |
| | | T _{sp} = 25 °C | | - | 7.5 | W |
| T _j | junction temperature | | | -55 | 175 | °C |
| T _{amb} | ambient temperature | | | -55 | 175 | °C |
| T _{stg} | storage temperature | | | -65 | 175 | °C |
| Source Drain Diode | | | | | | |
| I _S | source current | T _{amb} = 25 °C | [1] | - | 1.7 | A |
| ESD maximum rating | | | | | | |
| V _{ESD} | electrostatic discharge voltage | HBM | [3] | - | 500 | V |
| Avalanche ruggedness | | | | | | |
| E _{DS(AL)S} | non-repetitive drain-source avalanche energy | T _{j(initial)} = 25 °C; I _D = 0.75 A; DUT in avalanche (unclamped) | | - | 24 | mJ |

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.





9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|----------------|--|-------------|-----|-----|-----|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | 200 | 230 | K/W |
| | | | [2] | - | 78 | 90 | K/W |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | | | - | 15 | 20 | K/W |

[1] Device mounted on an FR4 (PCB), single-sided copper; tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

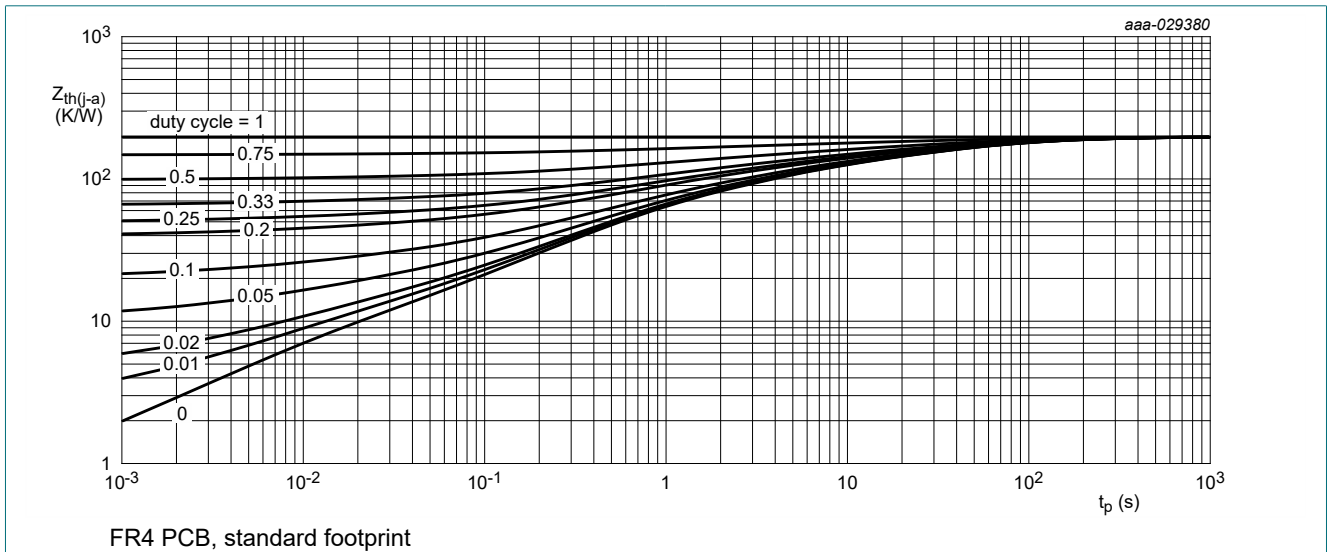


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

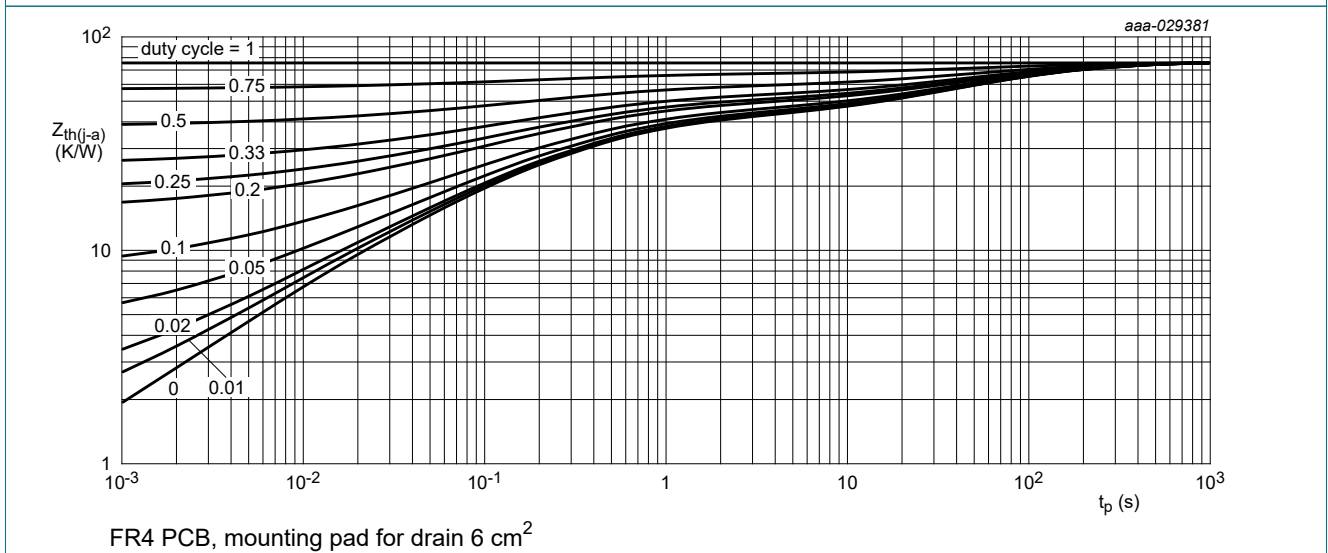


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---|--|------|------|---------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | 60 | - | - | V |
| V_{GSth} | gate-source threshold voltage | $I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$ | 1.3 | 1.7 | 2.7 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | - | 1 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | - | 100 | nA |
| | | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | - | -100 | nA |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 4.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ | - | 32 | 43 | m Ω |
| | | $V_{GS} = 10 \text{ V}; I_D = 4.2 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$ | - | 69 | 93 | m Ω |
| | | $V_{GS} = 4.5 \text{ V}; I_D = 3.8 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ | - | 38 | 53 | m Ω |
| g_{fs} | forward transconductance | $V_{DS} = 5 \text{ V}; I_D = 4.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ | - | 5 | - | S |
| R_G | gate resistance | $f = 1 \text{ MHz}$ | - | 3.5 | - | Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $V_{DS} = 30 \text{ V}; I_D = 4.2 \text{ A}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 10 | 15 | nC |
| Q_{GS} | gate-source charge | | - | 1.7 | - | nC |
| Q_{GD} | gate-drain charge | | - | 2.1 | - | nC |
| C_{iss} | input capacitance | $V_{DS} = 30 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 590 | - | pF |
| C_{oss} | output capacitance | | - | 60 | - | pF |
| C_{rss} | reverse transfer capacitance | | - | 34 | - | pF |
| $t_{d(on)}$ | turn-on delay time | | $V_{DS} = 30 \text{ V}; I_D = 4.2 \text{ A}; V_{GS} = 10 \text{ V}; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$ | - | 3 | - |
| t_r | rise time | - | | 5 | - | ns |
| $t_{d(off)}$ | turn-off delay time | - | | 11 | - | ns |
| t_f | fall time | - | | 4 | - | ns |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 1.7 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 0.8 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 2.3 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 15.5 | - | ns |
| Q_r | recovered charge | | - | 8.3 | - | nC |

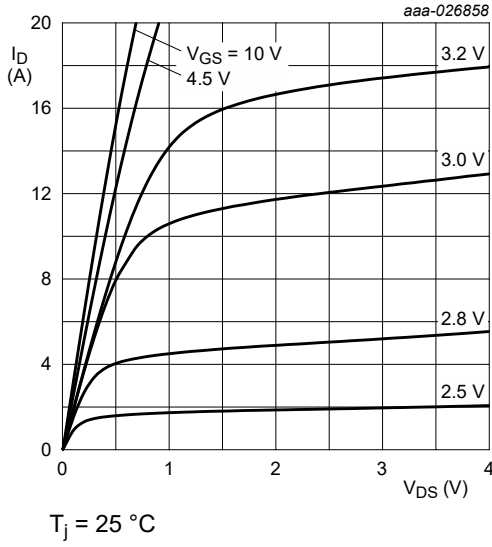


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

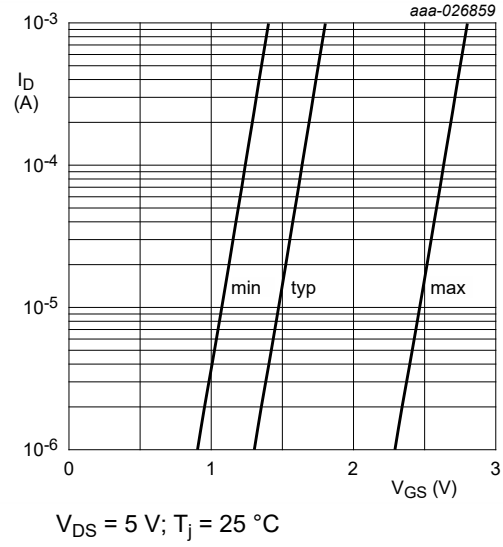


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

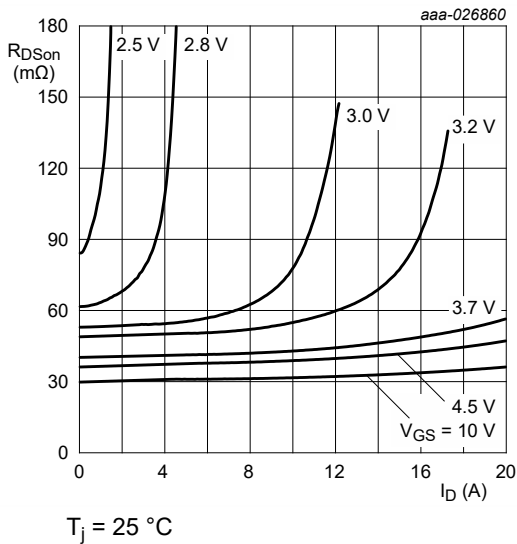


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

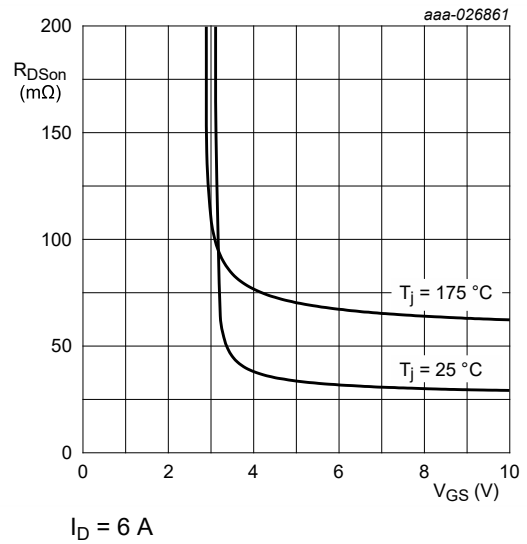
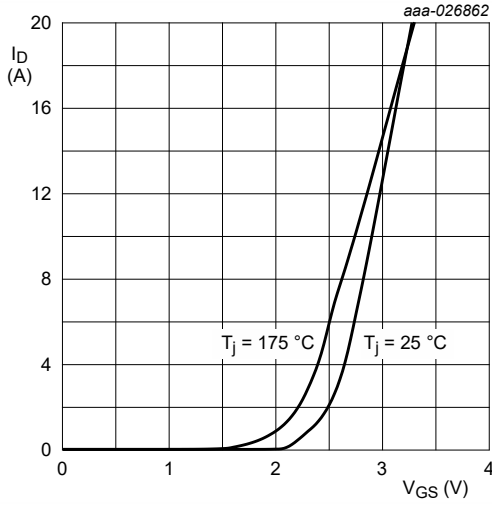
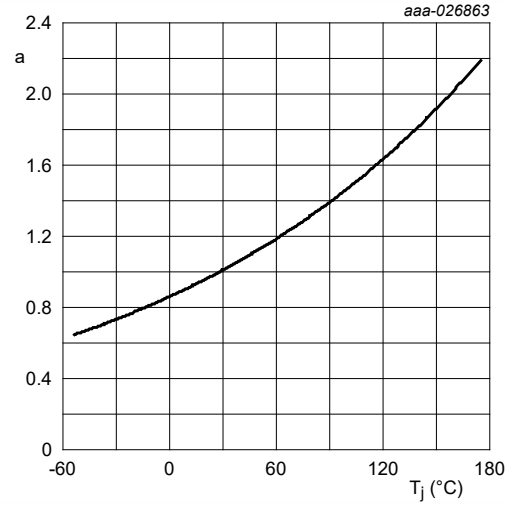


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



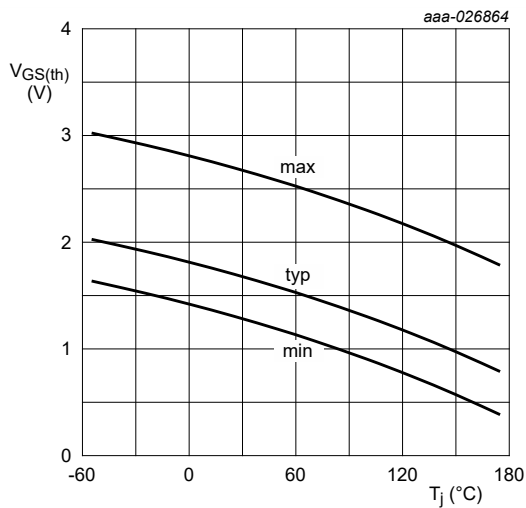
$$V_{DS} > I_D \times R_{DSon}$$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



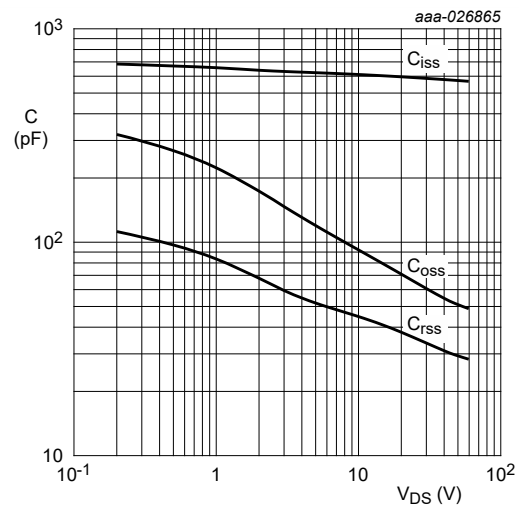
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



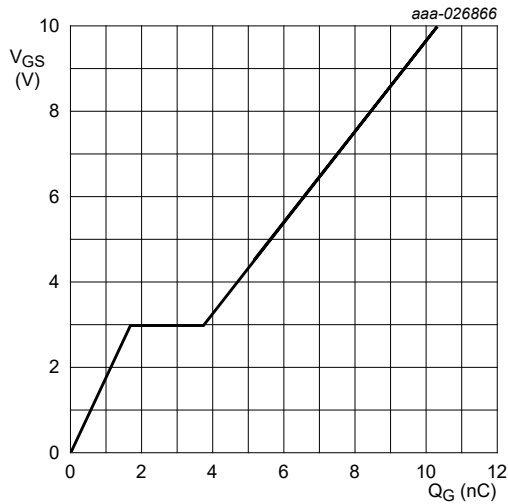
$$I_D = 250 \mu A; V_{DS} = V_{GS}$$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 30\text{ V}$; $I_D = 6\text{ A}$; $T_{amb} = 25\text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

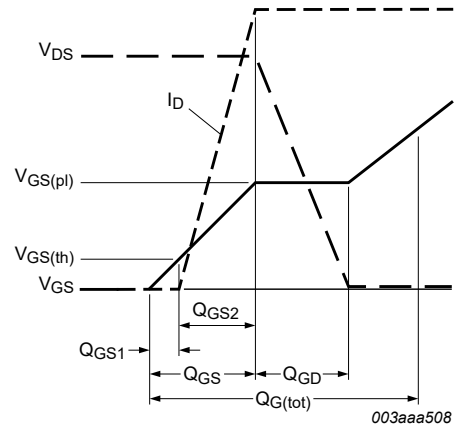
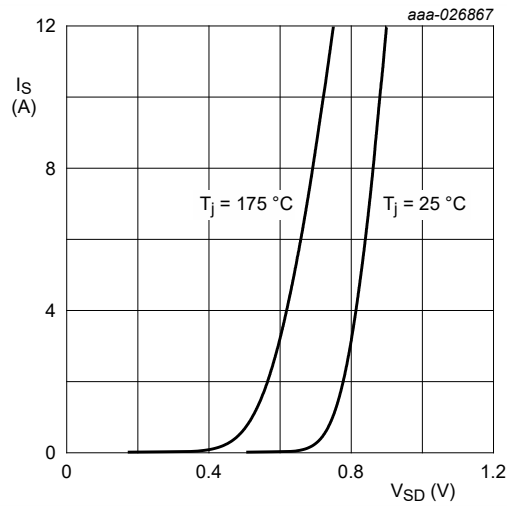


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information



Fig. 17. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

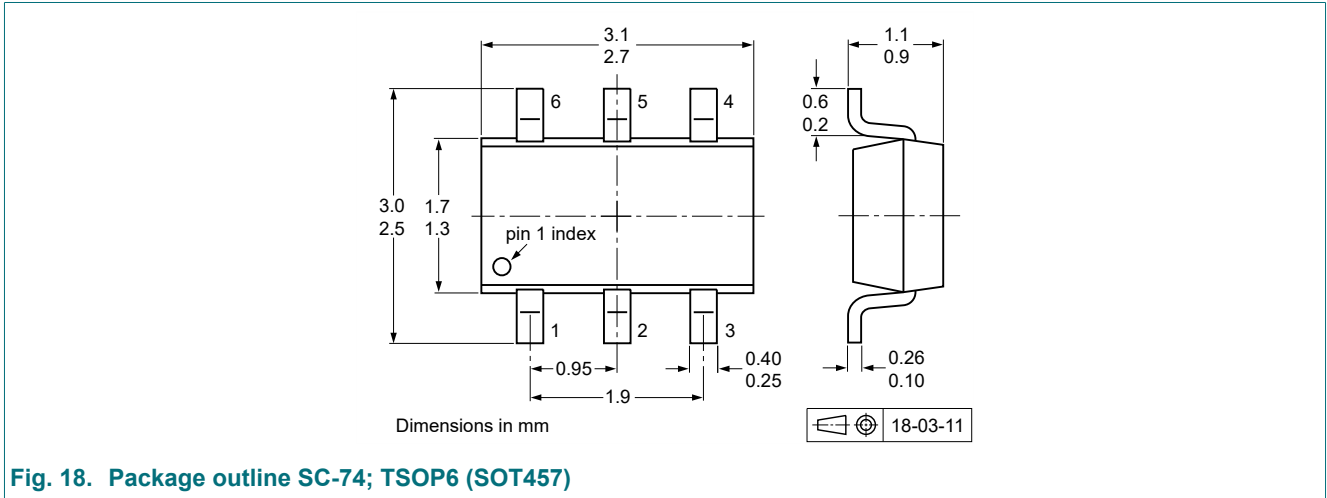


Fig. 18. Package outline SC-74; TSOP6 (SOT457)

13. Soldering

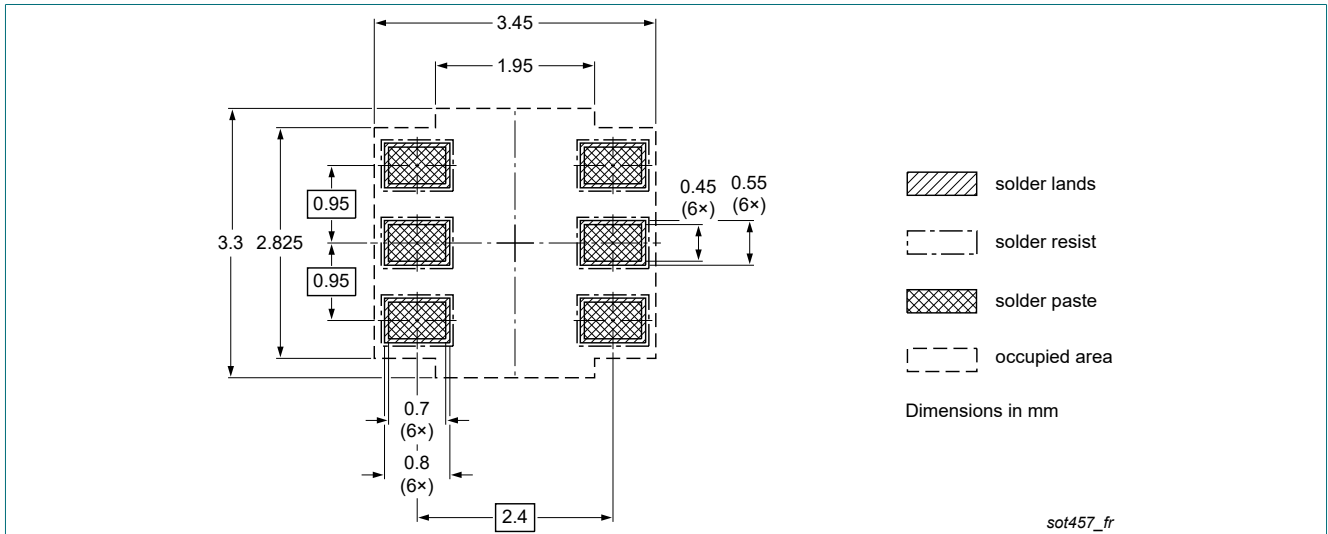


Fig. 19. Reflow soldering footprint for SC-74; TSOP6 (SOT457)

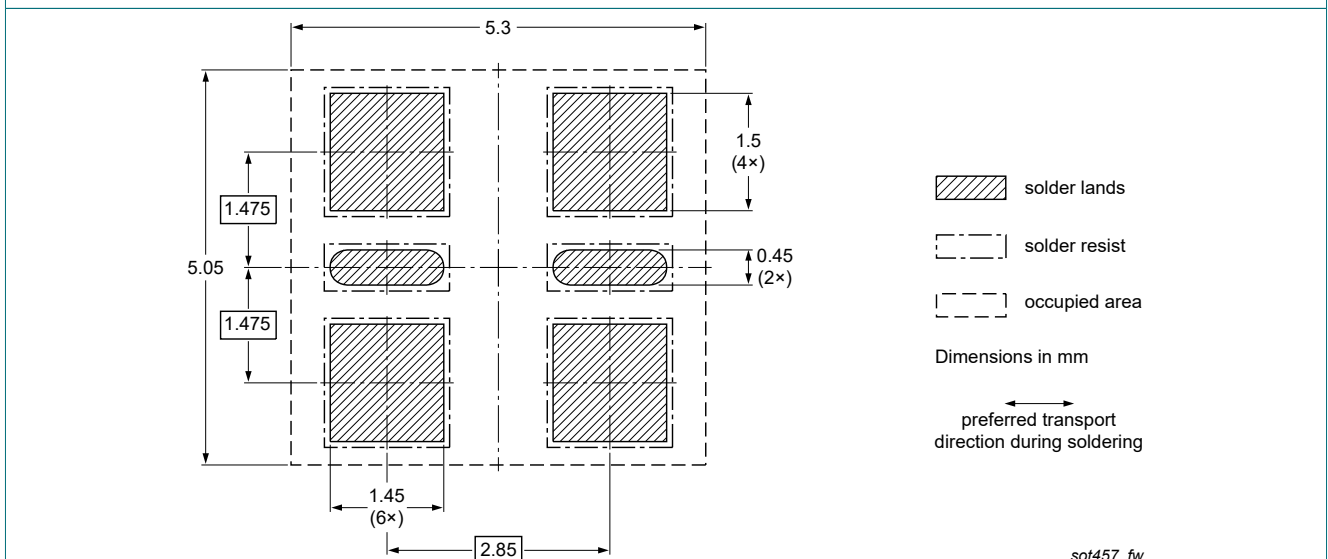


Fig. 20. Wave soldering footprint for SC-74; TSOP6 (SOT457)

14. Revision history

Table 8. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------|--------------|--------------------|---------------|------------|
| PMN40ENA v.1 | 20190411 | Product data sheet | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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| Product [short] data sheet | Production | This document contains the product specification. |

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