

#### Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <a href="http://www.nxp.com">http://www.nxp.com</a>, <a href="http://www.semiconductors.philips.com/">http://www.nxp.com</a>, <a href="http://www.nexperia.com">http://www.nexperia.com</a>, <a href="http://www.nexperia.com">http://www.nexperia.com</a>)

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use salesaddresses@nexperia.com (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © Nexperia B.V. (year). All rights reserved.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

# PMP4201V; PMP4201G; PMP4201Y

## **NPN/NPN** matched double transistors

Rev. 04 — 28 August 2009

**Product data sheet** 

## 1. Product profile

## 1.1 General description

NPN/NPN matched double transistors in small Surface-Mounted Device (SMD) plastic packages. The transistors in the SOT666 and SOT363 (SC-88) packages are fully isolated internally.

Table 1. Product overview

Type number	Package		NPN/NPN h <sub>FE1</sub> /h <sub>FE2</sub>	PNP/PNP	
	NXP	JEITA	0.95 complement	complement	
PMP4201V	SOT666	-	PMP4501V	PMP5201V	
PMP4201G	SOT353	SC-88A	PMP4501G	PMP5201G	
PMP4201Y	SOT363	SC-88	PMP4501Y	PMP5201Y	

#### 1.2 Features

- Current gain matching
- Base-emitter voltage matching
- Common emitter configuration for SOT353 types
- Application-optimized pinout

## 1.3 Applications

- Current mirror
- Differential amplifier

#### 1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per transis	stor					
$V_{CEO}$	collector-emitter voltage	open base	-	-	45	V
I <sub>C</sub>	collector current		-	-	100	mA
h <sub>FE</sub>	DC current gain	$V_{CE} = 5 \text{ V};$ $I_{C} = 2 \text{ mA}$	200	290	450	



# PMP4201V; PMP4201G; PMP4201Y

**NPN/NPN** matched double transistors

Table 2. Quick reference data ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per device						
h <sub>FE1</sub> /h <sub>FE2</sub>	h <sub>FE</sub> matching	$V_{CE} = 5 \text{ V};$ $I_{C} = 2 \text{ mA}$	[1] 0.98	1	-	
$V_{BE1}-V_{BE2}$	V <sub>BE</sub> matching	$V_{CE} = 5 \text{ V};$ $I_{C} = 2 \text{ mA}$	[2] -	-	2	mV

- [1] The smaller of the two values is taken as the numerator.
- [2] The smaller of the two values is subtracted from the larger value.

## **Pinning information**

Table 3 Pinning

SOT666; SOT363  1	Table 3.	Pinning		
1 base TR1 2 base TR2 3 collector TR2 4 emitter TR1 6 collector TR1  2 emitter TR1, TR2 3 base TR1 2 emitter TR1, TR2 4 collector TR2 5 collector TR1	Pin	Description	Simplified outline	Symbol
2 base TR2 3 collector TR2 4 emitter TR1 6 collector TR1   SOT353  1 base TR1 2 emitter TR1, TR2 3 base TR2 4 collector TR2 5 collector TR1	SOT666;	SOT363		
2 base TR2 3 collector TR2 4 emitter TR1 5 emitter TR1 6 collector TR1   SOT353  1 base TR1 2 emitter TR1, TR2 3 base TR2 4 collector TR2 5 collector TR1	1	base TR1		
3	2	base TR2	6   5   4	<del>-                                    </del>
5 emitter TR1 6 collector TR1  1 2 3 006aaa548  SOT353  1 base TR1 2 emitter TR1, TR2 3 base TR2 4 collector TR2 5 collector TR1	3	collector TR2		\
5 emitter TR1 6 collector TR1  1 2 3 006aaa548  SOT353  1 base TR1 2 emitter TR1, TR2 3 base TR2 4 collector TR2 5 collector TR1	4	emitter TR2		
6 collector TR1 001aab555  SOT353  1 base TR1 2 emitter TR1, TR2 3 base TR2 4 collector TR2 5 collector TR1	5	emitter TR1	البــــــــــــــــــــــــــــــــــــ	
1 base TR1 2 emitter TR1, TR2 3 base TR2 4 collector TR2 5 collector TR1	6	collector TR1		000aaa340
2 emitter TR1, TR2 3 base TR2 4 collector TR2 5 collector TR1	SOT353			
2 emitter TR1, TR2 3 base TR2 4 collector TR2 5 collector TR1	1	base TR1		
4 collector TR2 5 collector TR1	2	emitter TR1, TR2	<u> </u>	5 4
4 collector TR2 5 collector TR1	3	base TR2		TR1 TR2
5 collector IR1 1 2 3	4	collector TR2		
	5	collector TR1	<u> </u>	

## **Ordering information**

**Product data sheet** 

Table 4. **Ordering information** 

Type number	Package	Package						
	Name	Description	Version					
PMP4201V	-	plastic surface-mounted package; 6 leads	SOT666					
PMP4201G	SC-88A	plastic surface-mounted package; 5 leads	SOT353					
PMP4201Y	SC-88	plastic surface-mounted package; 6 leads	SOT363					

2 of 14

PMP4201V\_G\_Y\_4 © NXP B.V. 2009. All rights reserved. Rev. 04 — 28 August 2009

Downloaded From Oneyac.com

## 4. Marking

Table 5. Marking codes

Type number	Marking code <sup>[1]</sup>
PMP4201V	EA
PMP4201G	R7*
PMP4201Y	S7*

<sup>[1] \* = -:</sup> made in Hong Kong

## 5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transis	stor				
$V_{CBO}$	collector-base voltage	open emitter	-	50	V
$V_{CEO}$	collector-emitter voltage	open base	-	45	V
$V_{EBO}$	emitter-base voltage	open collector	-	6	V
I <sub>C</sub>	collector current		-	100	mA
I <sub>CM</sub>	peak collector current	single pulse; $t_p \le 1 \text{ ms}$	-	200	mA
P <sub>tot</sub>	total power dissipation	$T_{amb} \le 25  ^{\circ}C$			
	SOT666		[1][2]	200	mW
	SOT353		<u>[1]</u> _	200	mW
	SOT363		<u>[1]</u> _	200	mW
Per device	)				
P <sub>tot</sub>	total power dissipation	$T_{amb} \le 25  ^{\circ}C$			
	SOT666		[1][2]	300	mW
	SOT353		<u>[1]</u> _	300	mW
	SOT363		<u>[1]</u> -	300	mW
Tj	junction temperature		-	150	°C
T <sub>amb</sub>	ambient temperature		-65	+150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

<sup>[1]</sup> Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

<sup>\* =</sup> p: made in Hong Kong

<sup>\* =</sup> t: made in Malaysia

<sup>\* =</sup> W: made in China

<sup>[2]</sup> Reflow soldering is the only recommended soldering method.

## 6. Thermal characteristics

Table 7. Thermal characteristics

Idolo I.	Thormal onaraotoriotio	•					
Symbol	Parameter	Conditions	N	<b>V</b> lin	Тур	Max	Unit
Per trans	istor						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air					
	SOT666		[1][2]		-	625	K/W
	SOT353		<u>[1]</u> _		-	625	K/W
	SOT363		[1] _		-	625	K/W
Per devic	e						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air					
	SOT666		[1][2]		-	416	K/W
	SOT353		<u>[1]</u> _		-	416	K/W
	SOT363		<u>[1]</u> _		-	416	K/W

<sup>[1]</sup> Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

## 7. Characteristics

Table 8. Characteristics

T<sub>amb</sub> = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Тур	Max	Unit			
Per transis	Per transistor								
I <sub>CBO</sub>	collector-base cut-off current	$V_{CB} = 30 \text{ V};$ $I_E = 0 \text{ A}$	-	-	15	nA			
		$V_{CB} = 30 \text{ V};$ $I_{E} = 0 \text{ A};$ $T_{j} = 150 ^{\circ}\text{C}$	-	-	5	μΑ			
I <sub>EBO</sub>	emitter-base cut-off current	$V_{EB} = 5 \text{ V};$ $I_{C} = 0 \text{ A}$	-	-	100	nA			
h <sub>FE</sub>	DC current gain	$V_{CE} = 5 \text{ V};$ $I_{C} = 10 \mu\text{A}$	-	250	-				
		$V_{CE} = 5 \text{ V};$ $I_C = 2 \text{ mA}$	200	290	450				
V <sub>CEsat</sub>	collector-emitter saturation voltage	$I_C = 10 \text{ mA};$ $I_B = 0.5 \text{ mA}$	-	50	200	mV			
		$I_C = 100 \text{ mA};$ $I_B = 5 \text{ mA}$	-	200	400	mV			
V <sub>BEsat</sub>	base-emitter saturation voltage	$I_C = 10 \text{ mA};$ $I_B = 0.5 \text{ mA}$	[1] -	760	-	mV			
		$I_{C} = 100 \text{ mA};$ $I_{B} = 5 \text{ mA}$	[1] -	910	-	mV			

PMP4201V\_G\_Y\_4 © NXP B.V. 2009. All rights reserved.

<sup>[2]</sup> Reflow soldering is the only recommended soldering method.

**Product data sheet** 

#### **NPN/NPN** matched double transistors

5 of 14

Characteristics ...continued Table 8. T<sub>amb</sub> = 25 °C unless otherwise specified

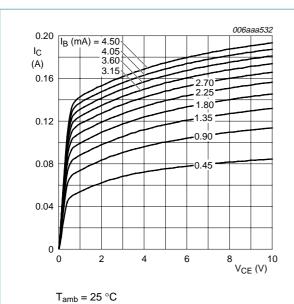
Symbol	Parameter	Conditions	N	lin Typ	Max	Unit
$V_{BE}$	base-emitter voltage	$V_{CE} = 5 \text{ V};$ $I_{C} = 2 \text{ mA}$	[2] 6	10 660	710	mV
		$V_{CE} = 5 \text{ V};$ $I_C = 10 \text{ mA}$	[2] -	-	770	mV
C <sub>c</sub>	collector capacitance	$V_{CB} = 10 \text{ V};$ $I_E = i_e = 0 \text{ A};$ $f = 1 \text{ MHz}$	-	-	1.5	pF
C <sub>e</sub>	emitter capacitance	$V_{EB} = 0.5 \text{ V};$ $I_{C} = i_{c} = 0 \text{ A};$ $f = 1 \text{ MHz}$	-	11	-	pF
f <sub>T</sub>	transition frequency	$V_{CE} = 5 \text{ V};$ $I_{C} = 10 \text{ mA};$ $f = 100 \text{ MHz}$	1	00 250	-	MHz
NF	noise figure	$V_{CE} = 5 \text{ V};$ $I_{C} = 0.2 \text{ mA};$ $R_{S} = 2 \text{ k}\Omega;$ $f = 10 \text{ Hz to}$ $15.7 \text{ kHz}$	-	2.8	-	dB
		$V_{CE} = 5 \text{ V};$ $I_{C} = 0.2 \text{ mA};$ $R_{S} = 2 \text{ k}\Omega;$ $f = 1 \text{ kHz};$ $B = 200 \text{ Hz}$	-	3.3	-	dB
Per device						
h <sub>FE1</sub> /h <sub>FE2</sub>	h <sub>FE</sub> matching	$V_{CE} = 5 \text{ V};$ $I_{C} = 2 \text{ mA}$	[3] 0	.98 1	-	
$V_{BE1}-V_{BE2}$	V <sub>BE</sub> matching	$V_{CE} = 5 \text{ V};$ $I_{C} = 2 \text{ mA}$	<u>[4]</u> -	-	2	mV

<sup>[1]</sup>  $V_{BEsat}$  decreases by about 1.7 mV/K with increasing temperature.

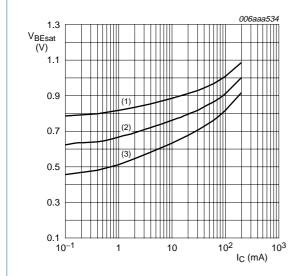
<sup>[2]</sup> V<sub>BE</sub> decreases by about 2 mV/K with increasing temperature.

<sup>[3]</sup> The smaller of the two values is taken as the numerator.

<sup>[4]</sup> The smaller of the two values is subtracted from the larger value.



Collector current as a function of Fig 1. collector-emitter voltage; typical values



 $I_{\rm C}/I_{\rm B} = 20$ 

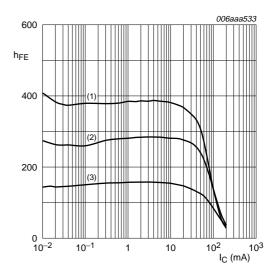
(1)  $T_{amb} = -55 \,^{\circ}C$ 

(2)  $T_{amb} = 25 \, ^{\circ}C$ 

**Product data sheet** 

(3)  $T_{amb} = 100 \, ^{\circ}C$ 

Fig 3. Base-emitter saturation voltage as a function of collector current; typical values



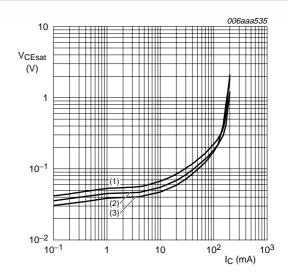
 $V_{CE} = 5 V$ 

(1)  $T_{amb} = 100 \, ^{\circ}C$ 

(2)  $T_{amb} = 25 \, ^{\circ}C$ 

(3)  $T_{amb} = -55 \, ^{\circ}C$ 

DC current gain as a function of collector Fig 2. current; typical values



 $I_{\rm C}/I_{\rm B} = 20$ 

(1)  $T_{amb} = 100 \, ^{\circ}C$ 

(2)  $T_{amb} = 25 \, ^{\circ}C$ 

(3)  $T_{amb} = -55 \, ^{\circ}C$ 

Collector-emitter saturation voltage as a Fig 4. function of collector current; typical values

6 of 14

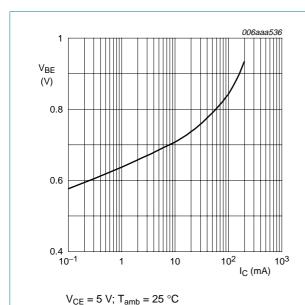
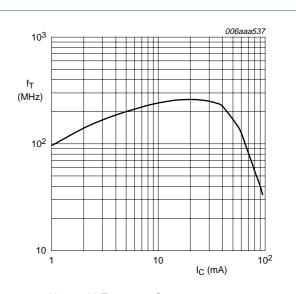
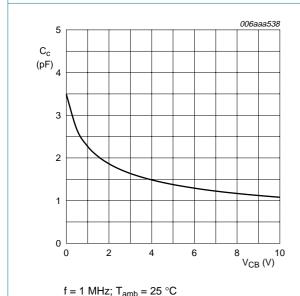


Fig 5. Base-emitter voltage as a function of collector current; typical values



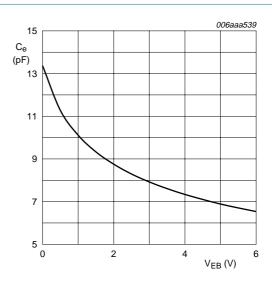
 $V_{CE} = 5 \text{ V}; T_{amb} = 25 \,^{\circ}\text{C}$ 





Collector capacitance as a function of Fig 7. collector-base voltage; typical values

**Product data sheet** 



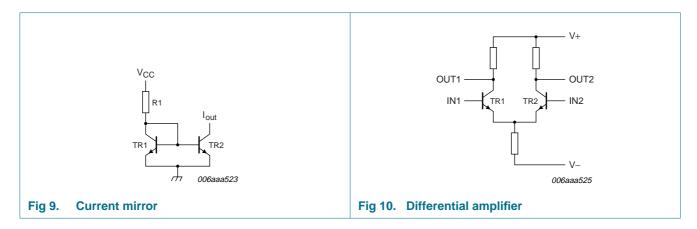
f = 1 MHz;  $T_{amb} = 25 \, ^{\circ}\text{C}$ 

Emitter capacitance as a function of Fig 8. emitter-base voltage; typical values

7 of 14

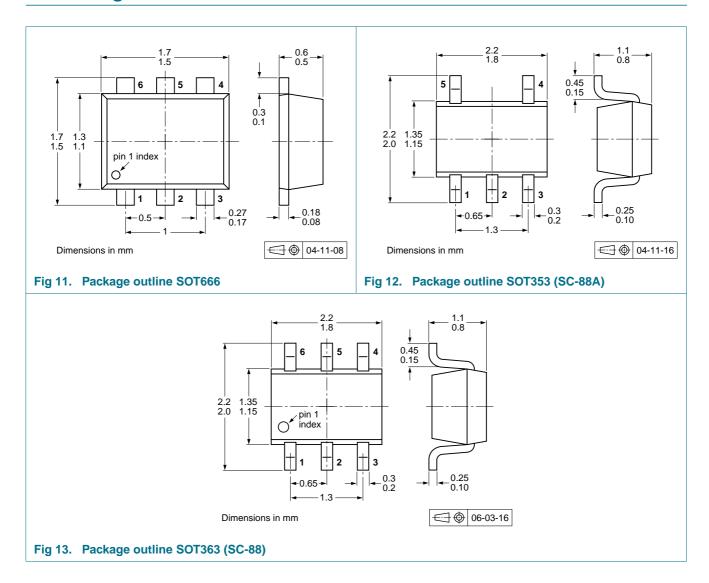
8 of 14

# **Application information**



## Package outline

**Product data sheet** 



PMP4201V\_G\_Y\_4 © NXP B.V. 2009. All rights reserved. Rev. 04 — 28 August 2009

## 10. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

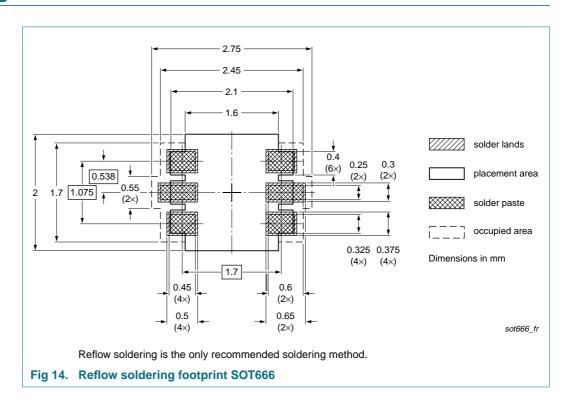
Туре	Package	Description		Packing quantity			
number			3000	4000	8000	10000	
PMP4201V SOT666		2 mm pitch, 8 mm tape and reel		-	-	-315	-
		4 mm pitch, 8 mm tape and reel		-	-115	-	-
PMP4201G	SOT353	4 mm pitch, 8 mm tape and reel		-115	-	-	-135
PMP4201Y SOT36		4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-	-	-165

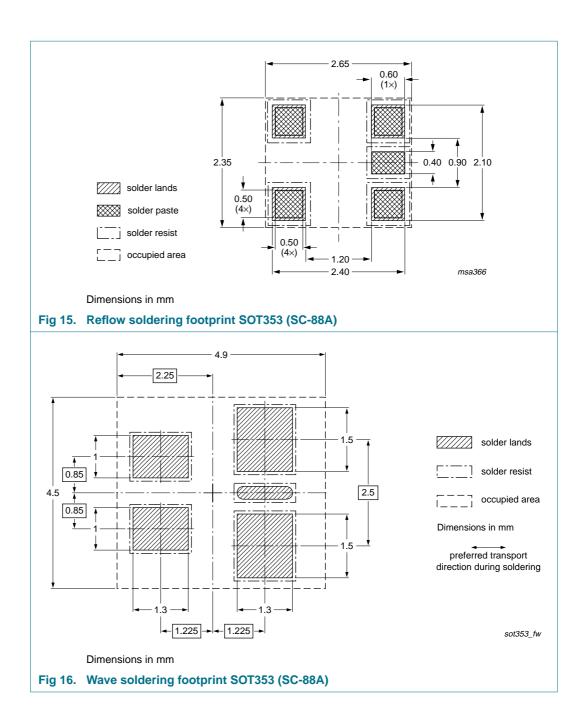
[1] For further information and the availability of packing methods, see Section 14.

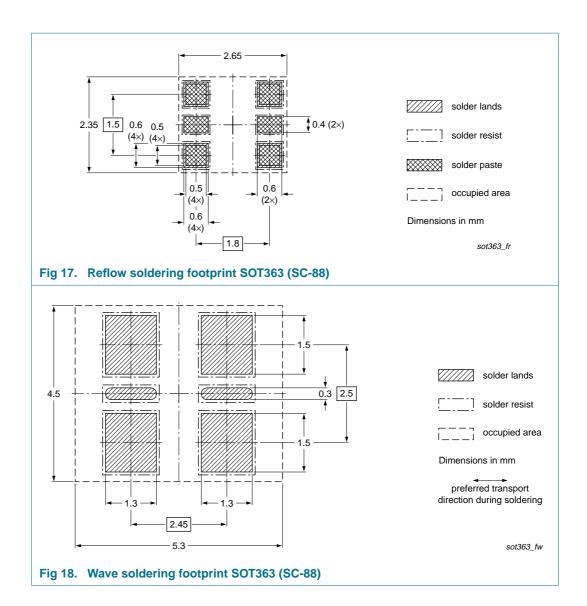
[2] T1: normal taping

[3] T2: reverse taping

## 11. Soldering







## 12. Revision history

#### Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes			
PMP4201V_G_Y_4	20090828	Product data sheet	-	PMP4201V_G_Y_3			
Modifications:	<ul> <li>This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.</li> </ul>						
	• Figure 14 "l	<ul> <li>Figure 14 "Reflow soldering footprint SOT666": updated</li> </ul>					
	• Figure 16 "	Nave soldering footprint SC	OT353 (SC-88A)": update	ed			
	<ul><li>Figure 17 "l</li></ul>	Reflow soldering footprint S	SOT363 (SC-88)": update	ed			
	• Figure 18 "	Wave soldering footprint SC	OT363 (SC-88)": updated	t			
PMP4201V_G_Y_3	20060915	Product data sheet	-	PMP4201G_Y_2			
PMP4201G_Y_2	20060214	Product data sheet	-	PMP4201G_Y_1			
PMP4201G_Y_1	20060131	Product data sheet	-	-			

## 13. Legal information

#### 13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

#### 13.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

#### 13.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <a href="http://www.nxp.com/profile/terms">http://www.nxp.com/profile/terms</a>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

#### 13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

#### 14. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: <a href="mailto:salesaddresses@nxp.com">salesaddresses@nxp.com</a>

PMP4201V\_G\_Y\_4 © NXP B.V. 2009. All rights reserved.

## **NXP Semiconductors**

# PMP4201V; PMP4201G; PMP4201Y

**NPN/NPN** matched double transistors

## 15. Contents

1	Product profile
1.1	General description
1.2	Features
1.3	Applications
1.4	Quick reference data
2	Pinning information 2
3	Ordering information
4	Marking 3
5	Limiting values 3
6	Thermal characteristics4
7	Characteristics4
8	Application information 8
9	Package outline
10	Packing information9
11	Soldering9
12	Revision history
13	Legal information
13.1	Data sheet status
13.2	Definitions
13.3	Disclaimers
13.4	Trademarks13
14	Contact information
15	Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2009.

All rights reserved.

DHILIDS

For more information, please visit: http://www.nxp.com For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 28 August 2009
Document identifier: PMP4201V\_G\_Y\_4



## 单击下面可查看定价,库存,交付和生命周期等信息

>>Nexperia(安世)