



PMPB100ENE

30 V, N-channel MOSFET

26 April 2018

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Extended temperature range $T_j = 175\text{ °C}$
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Tin-plated 100 % solderable side pads for optical solder inspection
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- Trench MOSFET technology

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

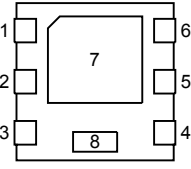
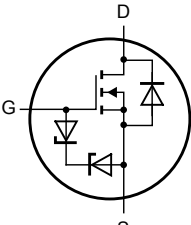
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------|---|-----|-----|-----|------------|
| V_{DS} | drain-source voltage | $T_j = 25\text{ °C}$ | - | - | 30 | V |
| V_{GS} | gate-source voltage | | -20 | - | 20 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$ | [1] | - | 5.1 | A |
| Static characteristics | | | | | | |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 3.9\text{ A}; T_j = 25\text{ °C}$ | - | 54 | 72 | m Ω |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6cm².

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|--|--|
| 1 | D | drain |  <p>Transparent top view DFN2020MD-6 (SOT1220)</p> |  <p>017aaa255</p> |
| 2 | D | drain | | |
| 3 | G | gate | | |
| 4 | S | source | | |
| 5 | D | drain | | |
| 6 | D | drain | | |
| 7 | D | drain | | |
| 8 | S | source | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|-------------|---|---------|
| | Name | Description | Version |
| PMPB100ENE | DFN2020MD-6 | DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals | SOT1220 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PMPB100ENE | 3T |

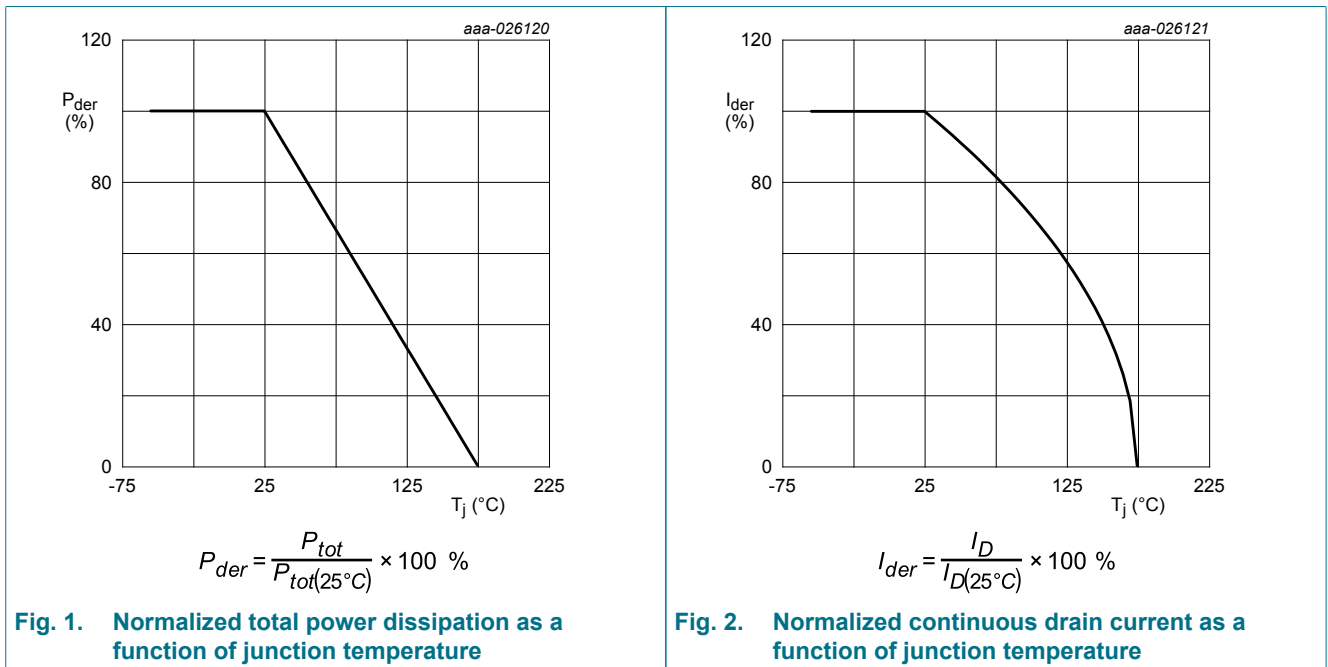
8. Limiting values

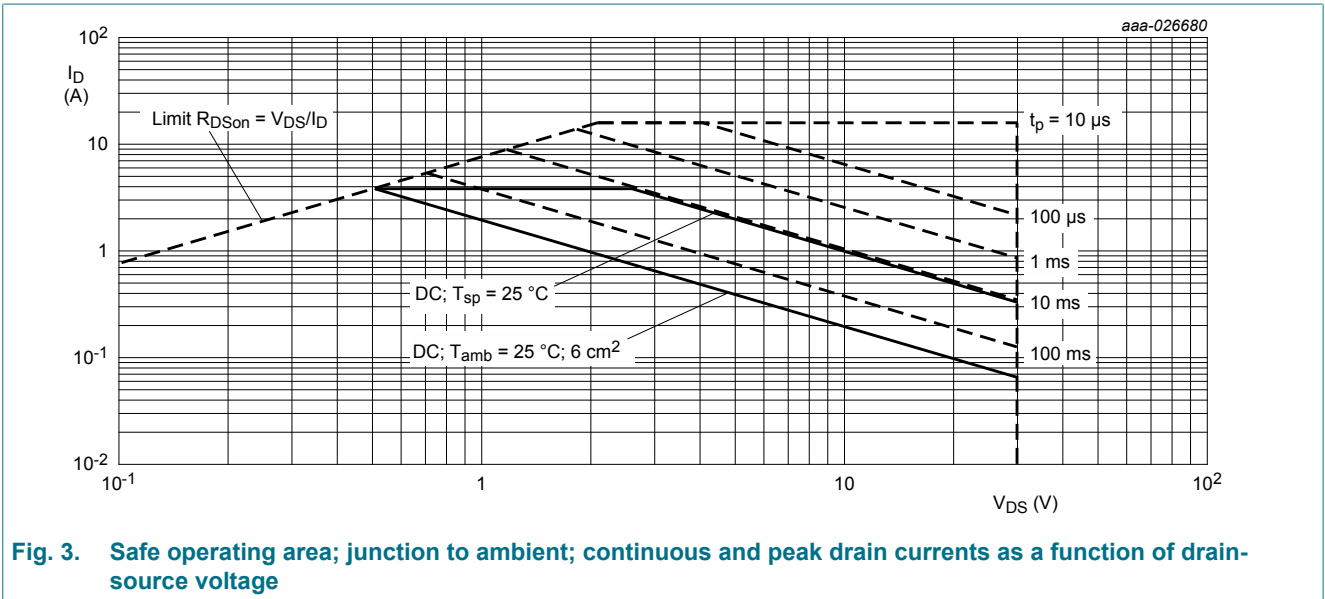
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---------------------------|-------------------------|--|-----|-----|-----|------|
| V _{DS} | drain-source voltage | T _j = 25 °C | | - | 30 | V |
| V _{GS} | gate-source voltage | | | -20 | 20 | V |
| I _D | drain current | V _{GS} = 10 V; T _{amb} = 25 °C; t ≤ 5 s | [1] | - | 5.1 | A |
| | | V _{GS} = 10 V; T _{amb} = 25 °C | [1] | - | 3.9 | A |
| | | V _{GS} = 10 V; T _{amb} = 100 °C | [1] | - | 2.4 | A |
| I _{DM} | peak drain current | T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs | | - | 16 | A |
| P _{tot} | total power dissipation | T _{amb} = 25 °C | [1] | - | 2 | W |
| | | T _{amb} = 25 °C; t ≤ 5 s | [1] | - | 3.3 | W |
| | | T _{sp} = 25 °C | | - | 10 | W |
| T _j | junction temperature | | | -55 | 175 | °C |
| T _{amb} | ambient temperature | | | -55 | 175 | °C |
| T _{stg} | storage temperature | | | -65 | 175 | °C |
| Source Drain Diode | | | | | | |
| I _S | source current | T _{amb} = 25 °C | [1] | - | 1.9 | A |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6cm².





9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|----------------|--|---------------------------|-----|-----|-----|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | 236 | 272 | K/W |
| | | | [2] | - | 67 | 77 | K/W |
| | | in free air; $t \leq 5$ s | [2] | - | 36 | 45 | K/W |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | | | - | 12 | 15 | K/W |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

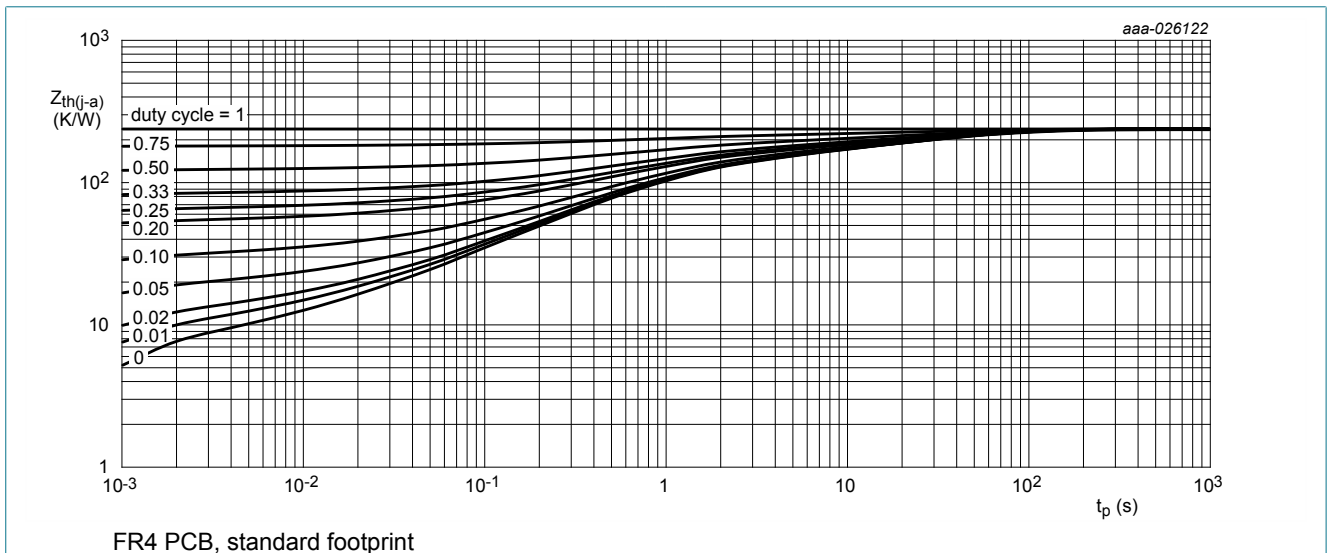


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

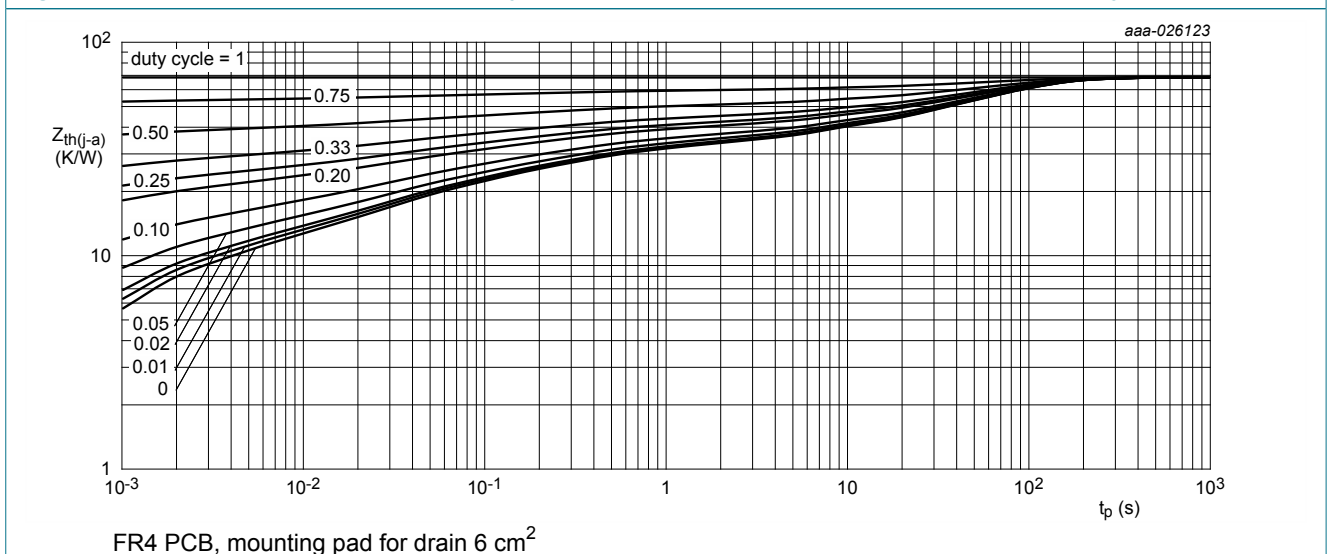


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|--|-----|------|-----|------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | 30 | - | - | V |
| V_{GSth} | gate-source threshold voltage | $I_D = 250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ C$ | 1 | 1.5 | 2.5 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 30 V$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | - | 1 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | - | 10 | μA |
| | | $V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | - | -10 | μA |
| | | $V_{GS} = 10 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | - | 2 | μA |
| | | $V_{GS} = -10 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | - | -2 | μA |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10 V$; $I_D = 3.9 A$; $T_j = 25 \text{ }^\circ C$ | - | 54 | 72 | m Ω |
| | | $V_{GS} = 10 V$; $I_D = 3.9 A$; $T_j = 175 \text{ }^\circ C$ | - | 98 | 130 | m Ω |
| | | $V_{GS} = 4.5 V$; $I_D = 3.3 A$; $T_j = 25 \text{ }^\circ C$ | - | 70 | 100 | m Ω |
| g_{fs} | forward transconductance | $V_{DS} = 10 V$; $I_D = 3.9 A$; $T_j = 25 \text{ }^\circ C$ | - | 6.2 | - | S |
| R_G | gate resistance | $f = 1 \text{ MHz}$ | - | 11.8 | - | Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $V_{DS} = 15 V$; $I_D = 3.9 A$; $V_{GS} = 10 V$; $T_j = 25 \text{ }^\circ C$ | - | 3.5 | 5 | nC |
| Q_{GS} | gate-source charge | | - | 0.4 | - | nC |
| Q_{GD} | gate-drain charge | | - | 0.8 | - | nC |
| C_{iss} | input capacitance | $V_{DS} = 15 V$; $f = 1 \text{ MHz}$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | 157 | - | pF |
| C_{oss} | output capacitance | | - | 34 | - | pF |
| C_{rss} | reverse transfer capacitance | | - | 27 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 15 V$; $I_D = 3.9 A$; $V_{GS} = 10 V$; $R_{G(ext)} = 6 \Omega$; $T_j = 25 \text{ }^\circ C$ | - | 3 | - | ns |
| t_r | rise time | | - | 19 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 15 | - | ns |
| t_f | fall time | | - | 8 | - | ns |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 1.9 A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | 0.8 | 1.2 | V |

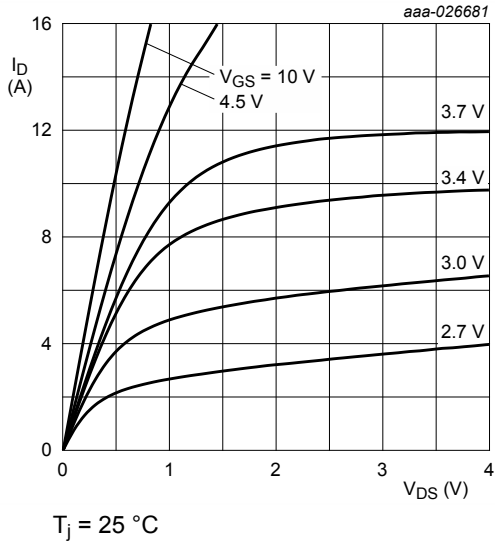


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

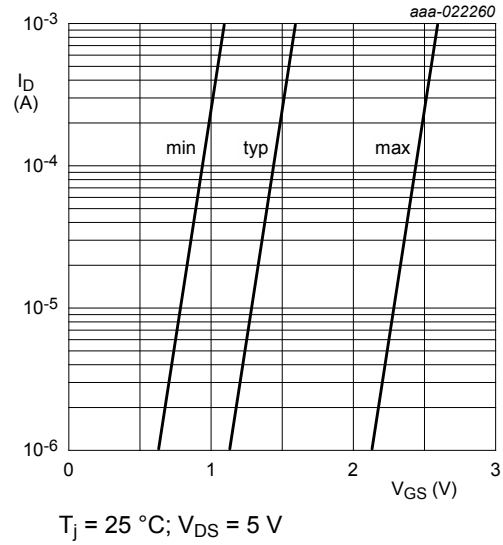


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

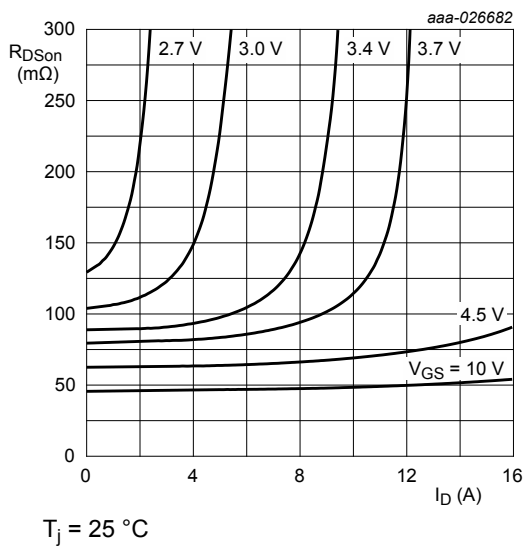


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

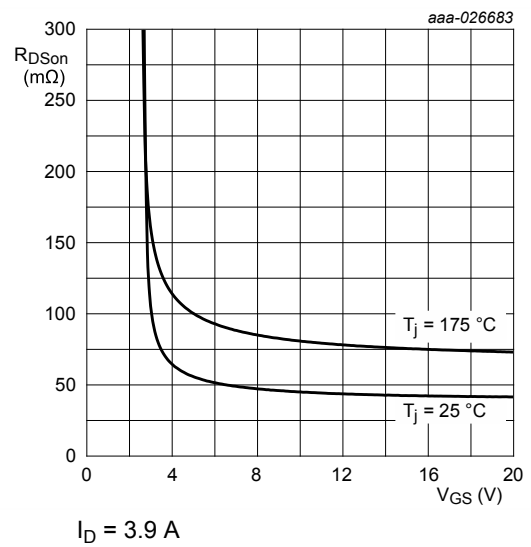
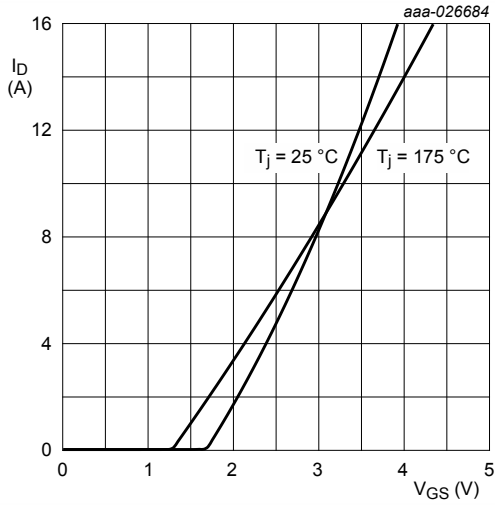
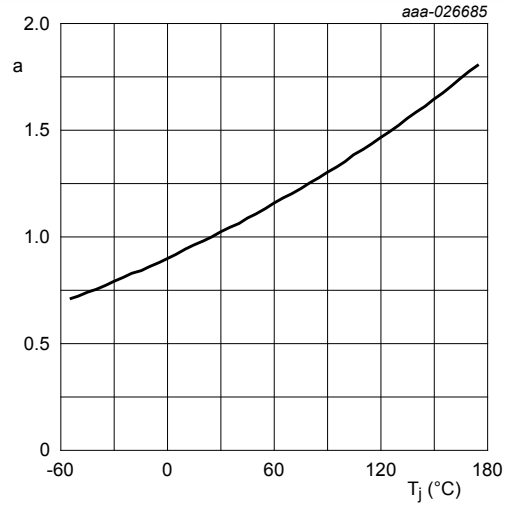


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



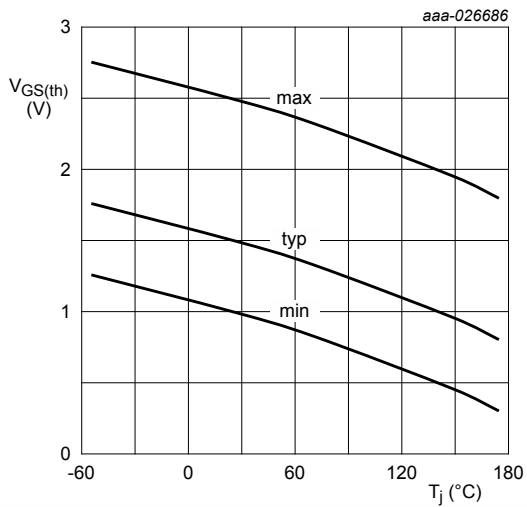
$$V_{DS} > I_D \times R_{DSon}$$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



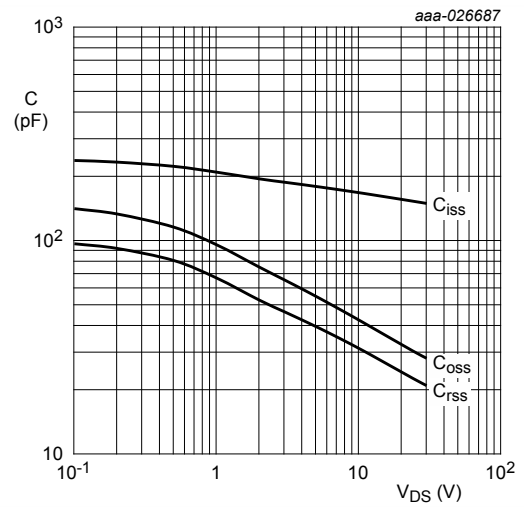
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



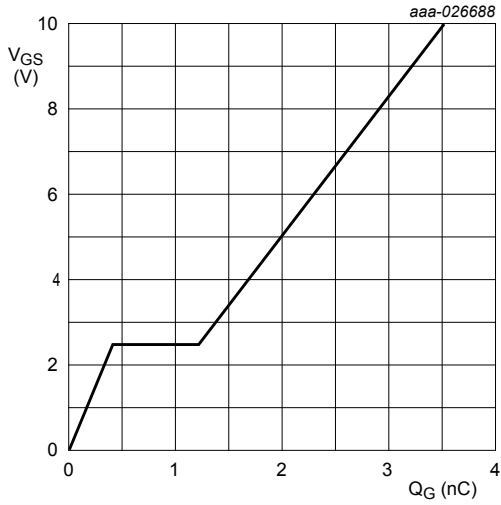
$$I_D = 250 \mu A; V_{DS} = V_{GS}$$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 15\text{ V}; I_D = 3.9\text{ A}; T_{amb} = 25\text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

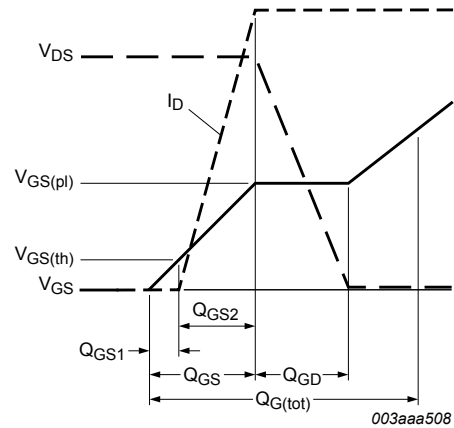
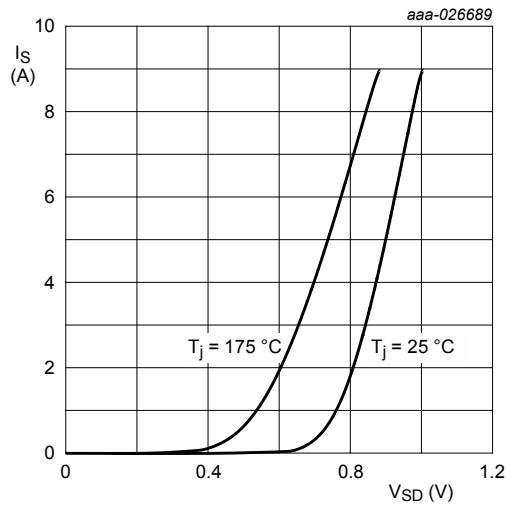


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

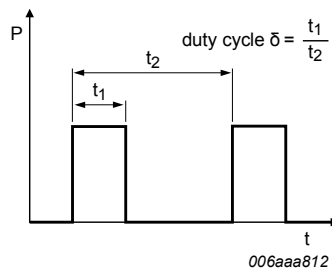


Fig. 17. Duty cycle definition

12. Package outline

DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads;
6 terminals; body 2 x 2 x 0.65 mm

SOT1220

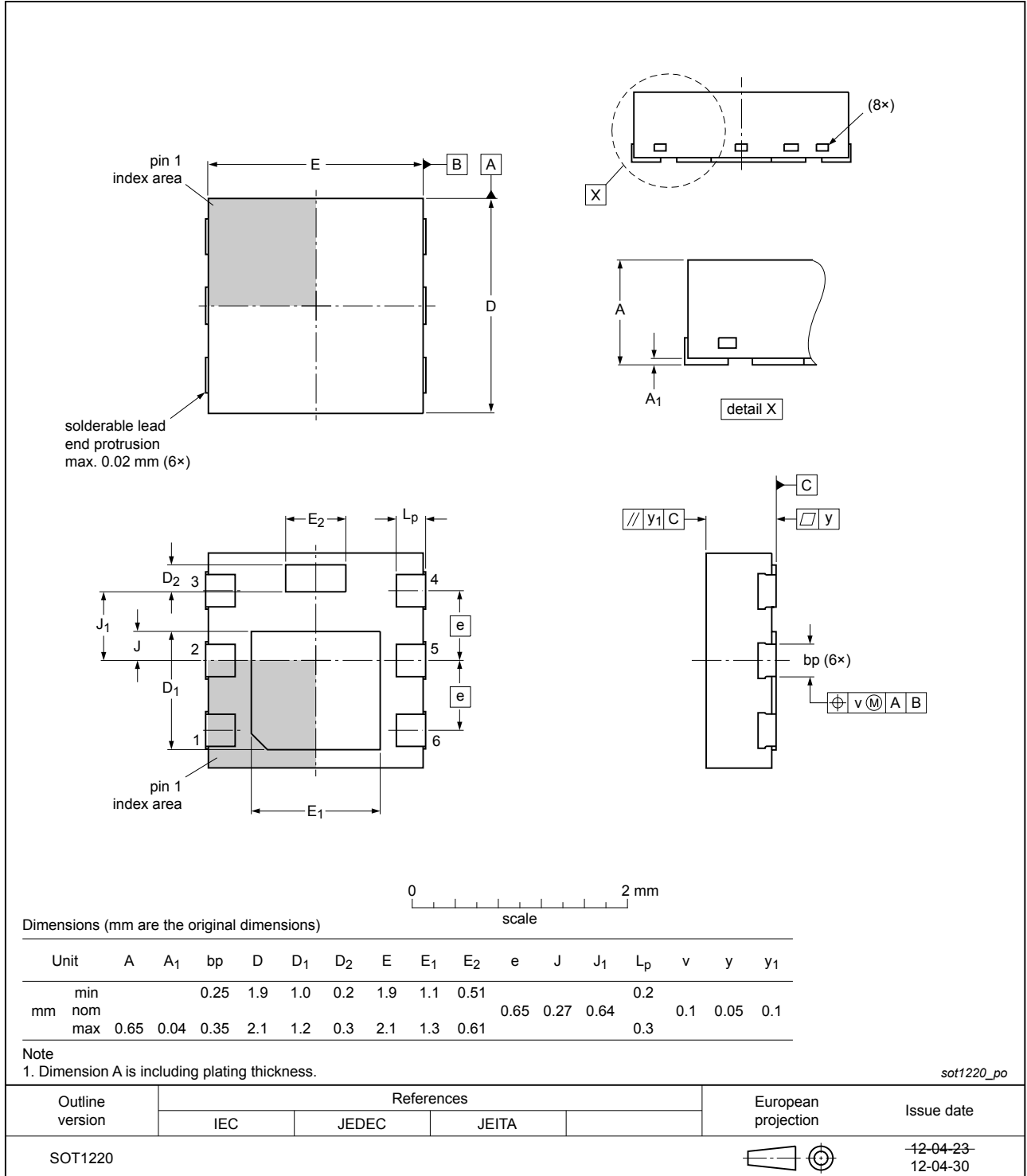


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

13. Soldering

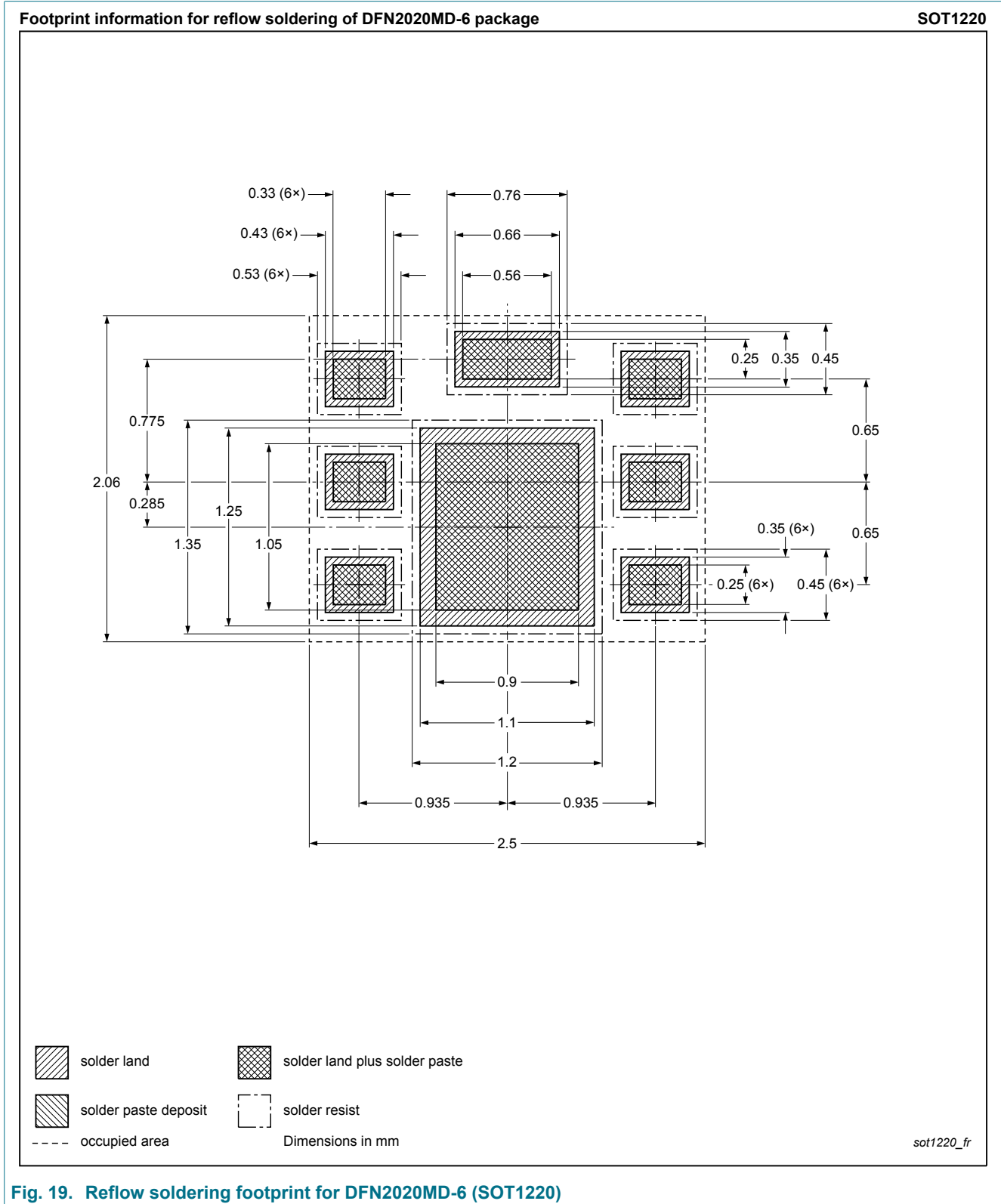


Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

14. Revision history

Table 8. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--------------|--------------------|---------------|------------|
| PMPB100ENE v.1 | 20180426 | Product data sheet | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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