

30 V, single N-channel Trench MOSFET 26 November 2014

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- 1 kV ESD protection
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction
- Tin-plated, 100% solderable side pads for optical solder inspection

3. Applications

- Charging switch for portable devices
- DC-to-DC converters
- Power management in battery-driven portables
- Hard disk and computing power management

4. Quick reference data

Table 1. Qui	ck reference data						
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	30	V
V _{GS}	gate-source voltage			-12	-	12	V
I _D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C; t ≤ 5 s	[1]	-	-	5	А
Static characteristics							
R _{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I _D = 5 A; T _j = 25 °C		-	28	33	mΩ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

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Pinning information 5.

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain		D
2	D	drain		
3	G	gate		G (The second s
4	S	source		
5	D	drain	Transparent top view	
6	D	drain	DFN2020MD-6 (SOT1220)	S 017aaa255
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information							
Type number	Package						
	Name	Description	Version				
PMPB29XNE	DFN2020MD-6	DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220				

7. Marking

Table 4. Marking codes	
Type number	Marking code
PMPB29XNE	1N

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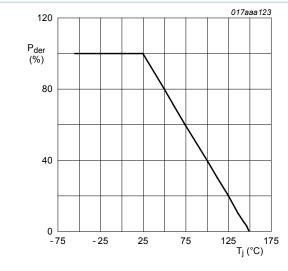
8. Limiting values

Table 5.Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	30	V
V _{GS}	gate-source voltage			-12	12	V
ID	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C; t ≤ 5 s	[1]	-	5	А
		V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	5	А
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	-	3.2	А
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \ \mu s$		-	12	А
P _{tot}	total power dissipation	T _{amb} = 25 °C	[1]	-	1.7	W
		T _{amb} = 25 °C; t ≤ 5 s	[1]	-	3.5	W
		T _{sp} = 25 °C		-	12.5	W
Tj	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-dra	in diode					
I _S	source current	T _{amb} = 25 °C	[1]	-	1.9	А

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².





$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

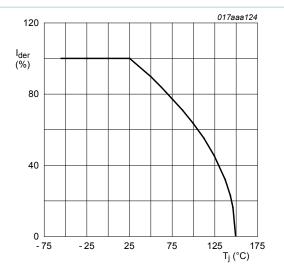


Fig. 2. Normalized continuous drain current as a function of junction temperature

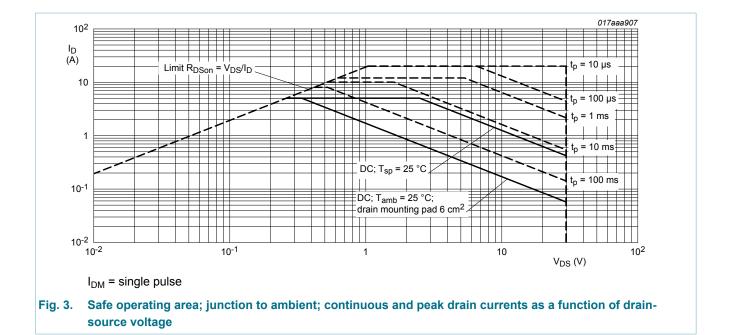
$$I_{der} = \frac{I_D}{I_{D(25^\circ \text{C})}} \times 100 \%$$

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9. Thermal characteristics

Table 6. T	Thermal characteristics						
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
ui(j-α)	thermal resistance	in free air	[1]	-	235	270	K/W
	from junction to ambient		[2]	-	67	74	K/W
	ampient	in free air; t ≤ 5 s	[2]	-	33	36	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	5	10	K/W

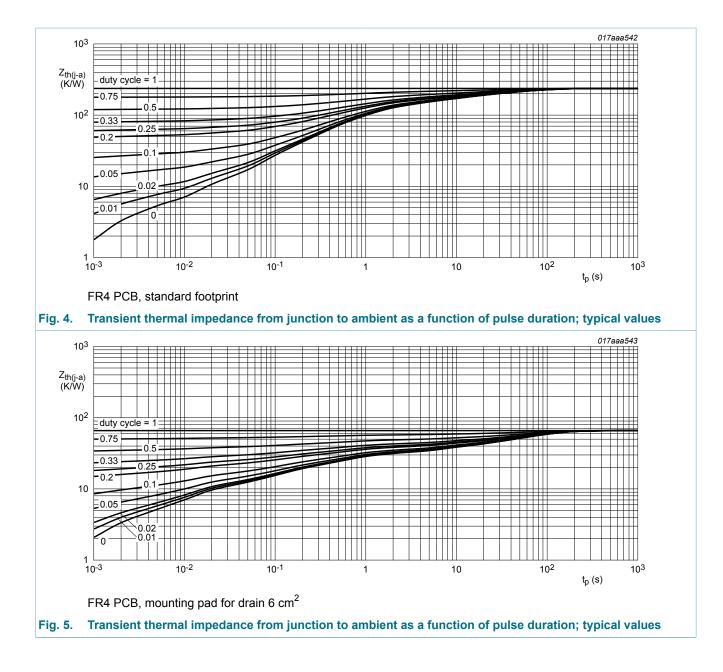
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

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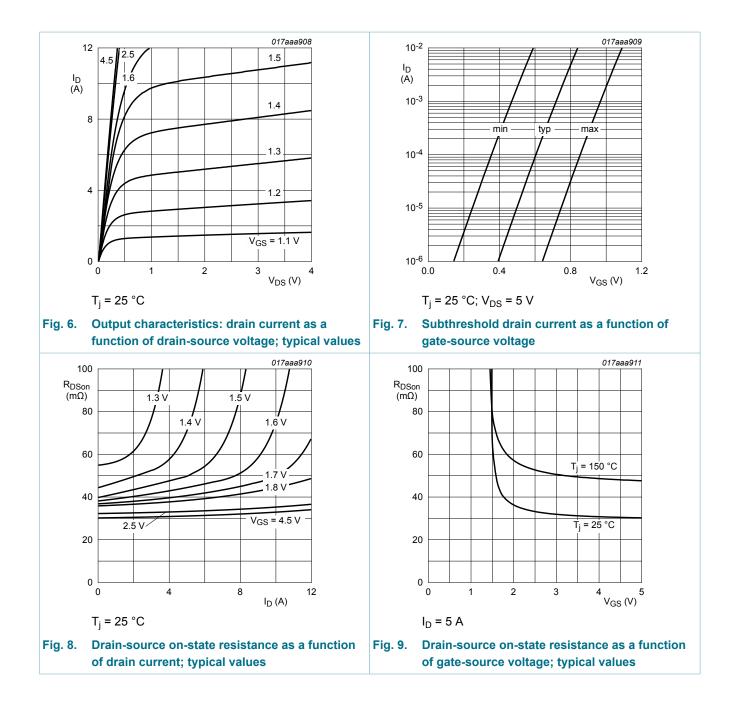


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10. Characteristics

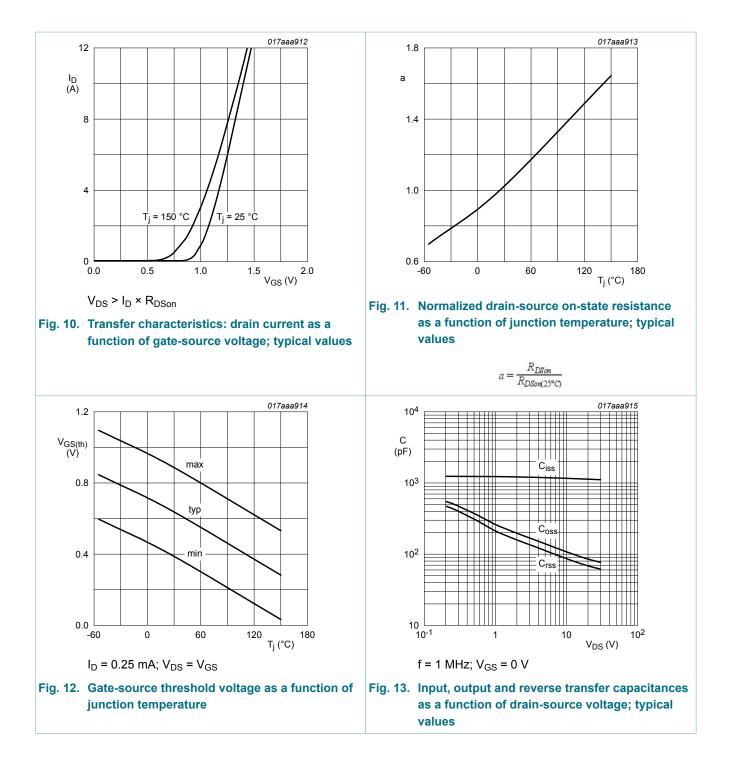
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics	11				
V _{(BR)DSS}	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	30	-	-	V
V _{GSth}	gate-source threshold voltage	I_D = 250 µA; V_{DS} = V_{GS} ; T_j = 25 °C	0.4	0.65	0.9	V
I _{DSS}	drain leakage current	V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	μA
I _{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C	-	-	10	μA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C	-	-	-10	μA
R _{DSon}	drain-source on-state	V _{GS} = 4.5 V; I _D = 5 A; T _j = 25 °C	-	28	33	mΩ
	resistance	V _{GS} = 4.5 V; I _D = 5 A; T _j = 150 °C	-	46	54	mΩ
		V_{GS} = 2.5 V; I _D = 3 A; T _j = 25 °C	-	32	40	mΩ
		V _{GS} = 1.8 V; I _D = 1.9 A; T _j = 25 °C	-	37	50	mΩ
9 _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 5 A; T _j = 25 °C	-	30	-	S
R _G	gate resistance	f = 1 MHz; T _j = 25 °C	-	1.8	-	Ω
Dynamic ch	aracteristics	· · · · ·				
Q _{G(tot)}	total gate charge	V_{DS} = 15 V; I _D = 5 A; V _{GS} = 4.5 V;	-	12.4	18.6	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	1.2	-	nC
Q _{GD}	gate-drain charge	-	-	2.1	-	nC
C _{iss}	input capacitance	V _{DS} = 15 V; f = 1 MHz; V _{GS} = 0 V;	-	1150	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	110	-	pF
C _{rss}	reverse transfer capacitance		-	85	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = 15 V; I _D = 5 A; V _{GS} = 4.5 V;	-	8	-	ns
t _r	rise time	R _{G(ext)} = 6 Ω; T _j = 25 °C	-	17	-	ns
t _{d(off)}	turn-off delay time		-	33	-	ns
t _f	fall time		-	32	-	ns
Source-drai	in diode	· · · · · · · · · · · · · · · · · · ·	I			
V _{SD}	source-drain voltage	I _S = 1.9 A; V _{GS} = 0 V; T _i = 25 °C	-	0.6	1.2	V

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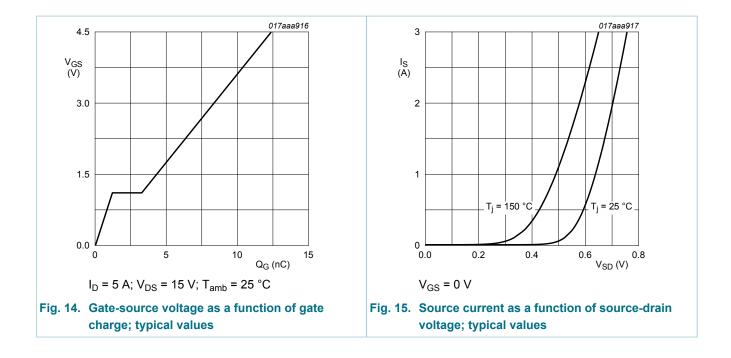
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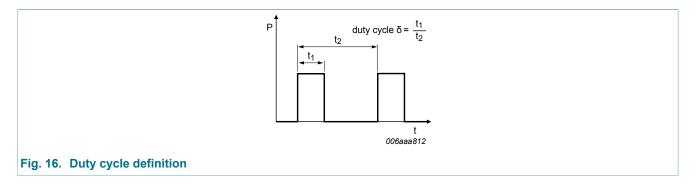
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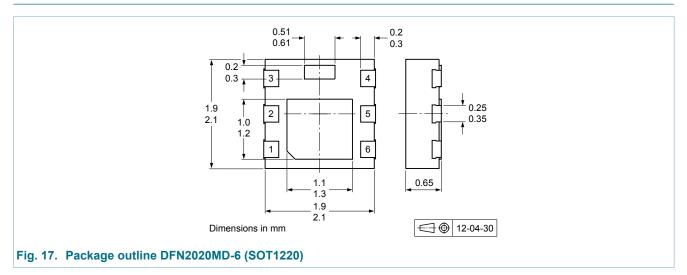


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11. Test information

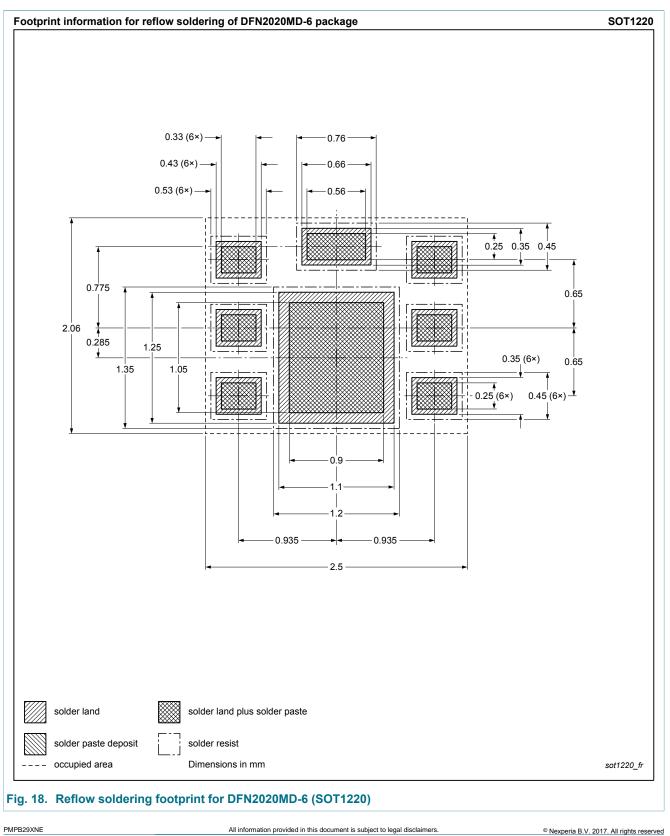


12. Package outline



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13. Soldering



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14. Revision history

Table 8. Revision h	istory			
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB29XNE v.2	20141126	Product data sheet	-	PMPB29XNE v.1
Modifications:	 3D package outline Features and bene Table 5: updated 		·	
PMPB29XNE v.1	20121130	Product data sheet	-	-

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15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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	Features and benefits

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