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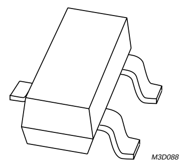



# PMV213SN

## µTrenchMOS™ standard level FET

**Rev. 02 — 19 February 2003** **Product data**

# 1. Product profile

## 1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PMV213SN in SOT23.

## 1.2 Features

- Low on-state resistance in a small surface mount package.

## 1.3 Applications

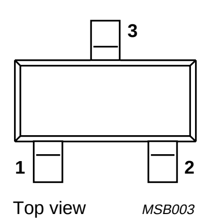
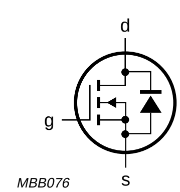
- DC-to-DC primary side switching.

## 1.4 Quick reference data

- $V_{DS} \leq 100$ V
- $I_D \leq 1.9$ A
- $P_{tot} \leq 2$ W
- $R_{DSon} \leq 250$ mΩ

# 2. Pinning information

**Table 1: Pinning - SOT23 simplified outline and symbol**

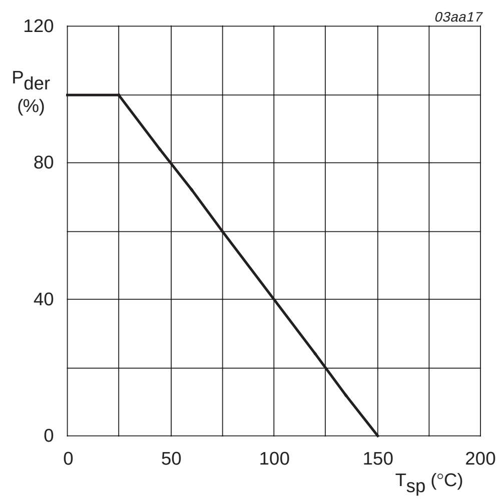
| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1 | gate (g) |   SOT23 |   |
| 2 | source (s) | | |
| 3 | drain (d) | | |

# 3. Limiting values

**Table 2: Limiting values**

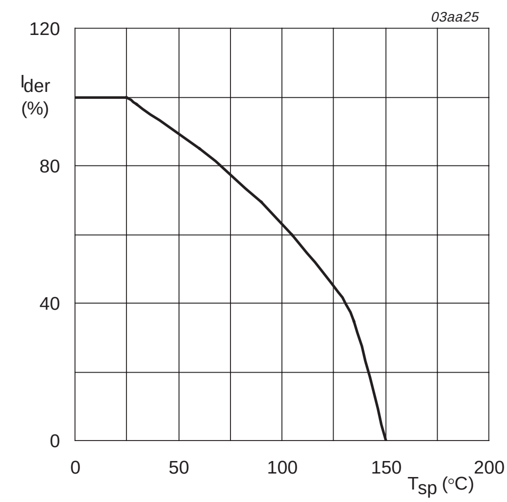
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C | - | 100 | V |
| $V_{DGR}$ | drain-gate voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C; $R_{GS}$ = 20 kΩ | - | 100 | V |
| $V_{GS}$ | gate-source voltage (DC) | | - | ±30 | V |
| $I_D$ | drain current (DC) | $T_{sp}$ = 25 °C; $V_{GS}$ = 10 V; Figure 2 and 3 | - | 1.9 | A |
| | | $T_{sp}$ = 100 °C; $V_{GS}$ = 10 V; Figure 2 | - | 1.2 | A |
| $I_{DM}$ | peak drain current | $T_{sp}$ = 25 °C; pulsed; $t_p$ ≤ 10 μs; Figure 3 | - | 7.6 | A |
| $P_{tot}$ | total power dissipation | $T_{sp}$ = 25 °C; Figure 1 | - | 2 | W |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_j$ | junction temperature | | –55 | +150 | °C |
| **Source-drain diode** | | | | | |
| $I_S$ | source (diode forward) current (DC) | $T_{sp}$ = 25 °C | - | 1.7 | A |
| $I_{SM}$ | peak source (diode forward) current | $T_{sp}$ = 25 °C; pulsed; $t_p$ ≤ 10 μs | - | 6.9 | A |



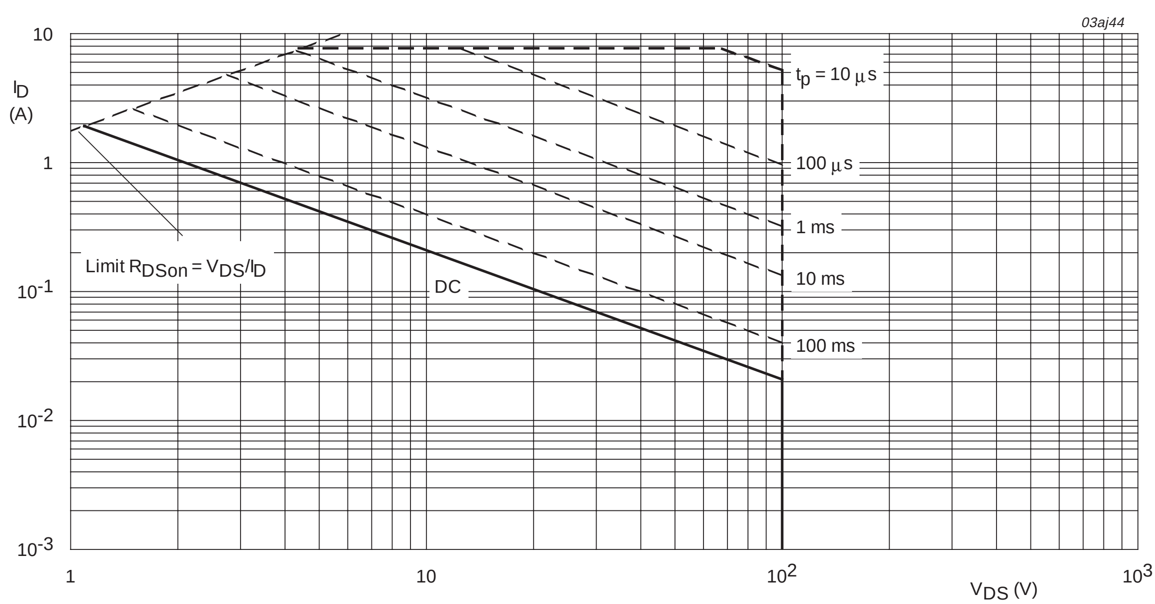

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of solder point temperature.**




$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

**Fig 2. Normalized continuous drain current as a function of solder point temperature.**




$T_{sp}$ = 25 °C; $I_{DM}$ is single pulse; $V_{GS}$ = 10V

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

## 4. Thermal characteristics

**Table 3: Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | Figure 4 | - | - | 60 | K/W |

### 4.1 Transient thermal impedance

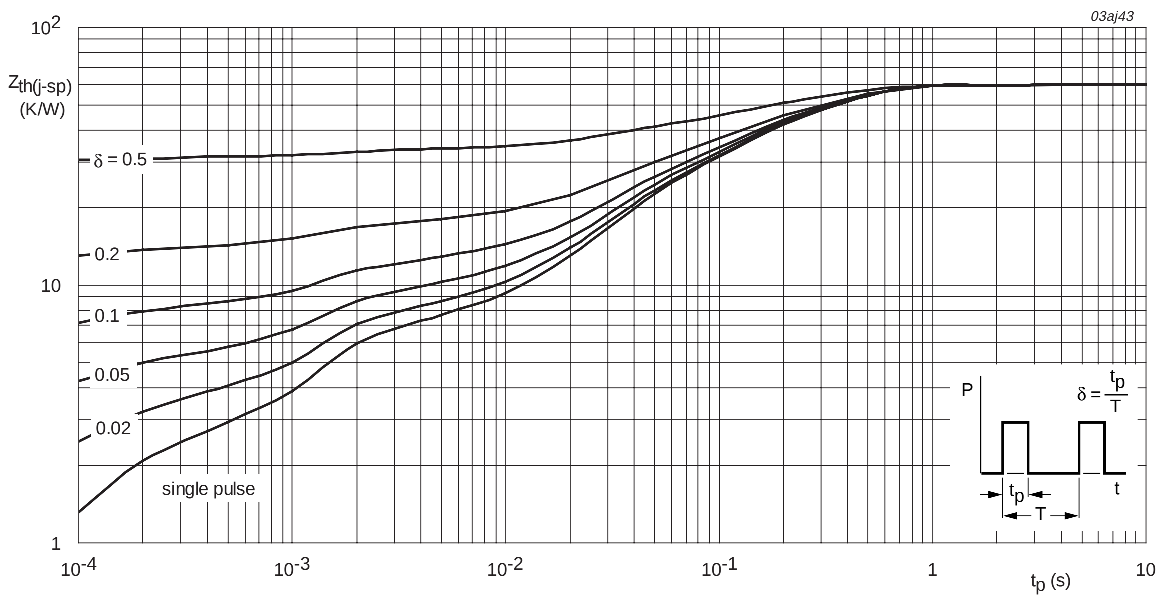


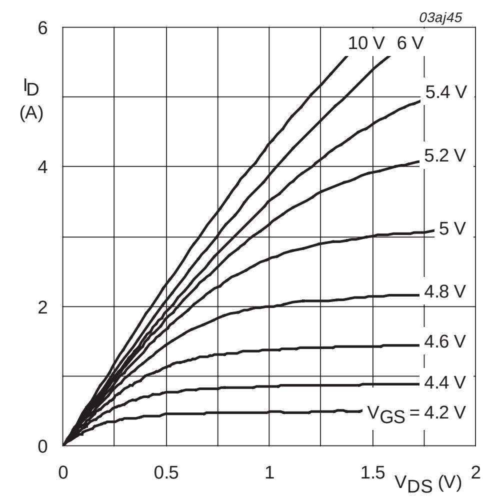

**Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.**

# 5. Characteristics

**Table 4: Characteristics**

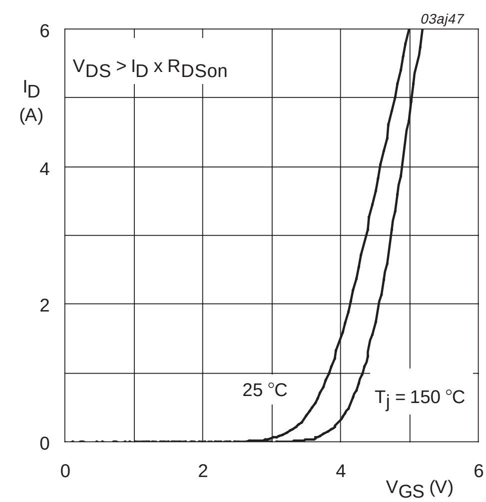
*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | 100 | - | - | V |
| | | $T_j$ = –55 °C | 90 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; Figure 9 | | | | |
| | | $T_j$ = 25 °C | 2 | 3 | 4 | V |
| | | $T_j$ = 150 °C | 1.2 | - | - | V |
| | | $T_j$ = –55 °C | - | - | 4.4 | V |
| $I_{DSS}$ | drain-source leakage current | $V_{DS}$ = 100 V; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | - | - | 1 | µA |
| | | $T_j$ = 150 °C | - | - | 100 | µA |
| $I_{GSS}$ | gate-source leakage current | $V_{GS}$ = ±20 V; $V_{DS}$ = 0 V | - | 10 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 0.5 A; Figure 7 and 8 | | | | |
| | | $T_j$ = 25 °C | - | 213 | 250 | mΩ |
| | | $T_j$ = 150 °C | - | 490 | 575 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{g(tot)}$ | total gate charge | $I_D$ = 1.2 A; $V_{DD}$ = 80 V; $V_{GS}$ = 10 V; Figure 13 | - | 7 | - | nC |
| $Q_{gs}$ | gate-source charge | | - | 1.4 | - | nC |
| $Q_{gd}$ | gate-drain (Miller) charge | | - | 2.5 | - | nC |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; f = 1 MHz; Figure 11 | - | 330 | - | pF |
| $C_{oss}$ | output capacitance | | - | 36 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 22 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DD}$ = 50 V; $R_L$ = 33 Ω; $V_{GS}$ = 10 V; $R_G$ = 6 Ω | - | 5.5 | - | ns |
| $t_r$ | rise time | | - | 5 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 9.5 | - | ns |
| $t_f$ | fall time | | - | 3 | - | ns |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain (diode forward) voltage | $I_S$ = 1.5 A; $V_{GS}$ = 0 V; Figure 12 | - | 0.83 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 1.2 A; $dI_S/dt$ = –100 A/µs; $V_{GS}$ = 0 V | - | 36 | - | ns |
| $Q_r$ | recovered charge | | - | 23 | - | nC |



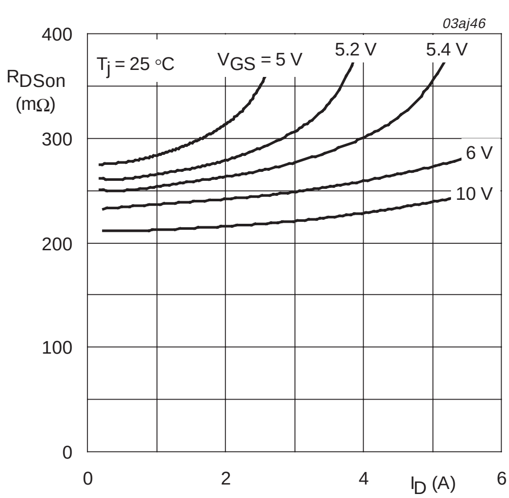

$T_j = 25\ °C$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



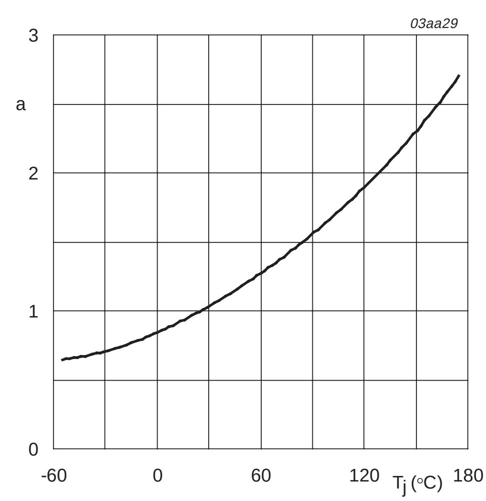

$T_j = 25\ °C$ and $150\ °C$; $V_{DS} > I_D \times R_{DSon}$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



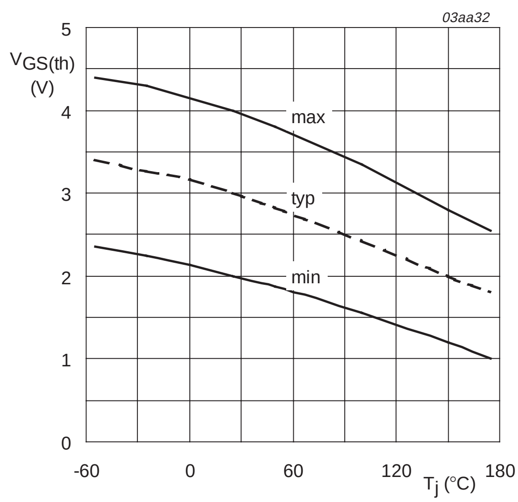

$T_j = 25\ °C$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



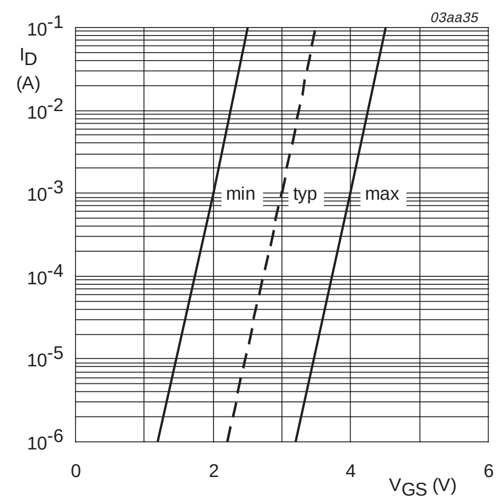

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



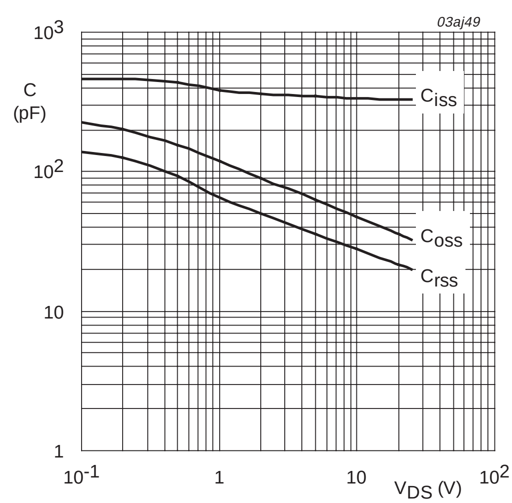

$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



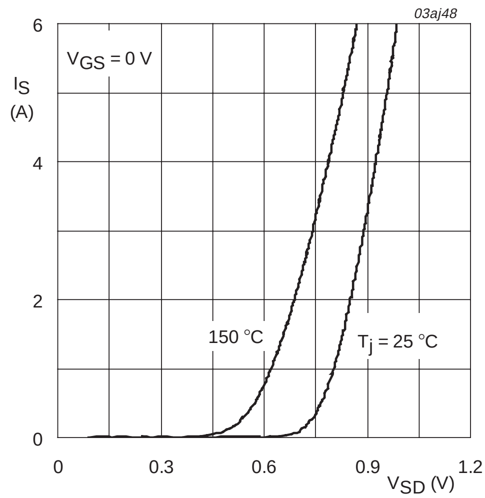

$T_j$ = 25 °C

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



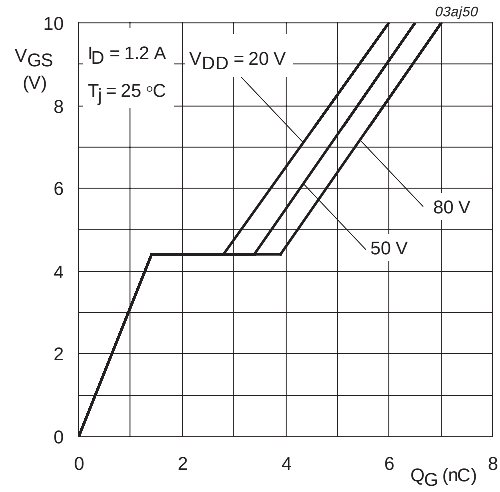

$V_{GS}$ = 0 V; f = 1 MHz

**Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**




$T_j$ = 25 °C and 150 °C; $V_{GS}$ = 0 V

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**

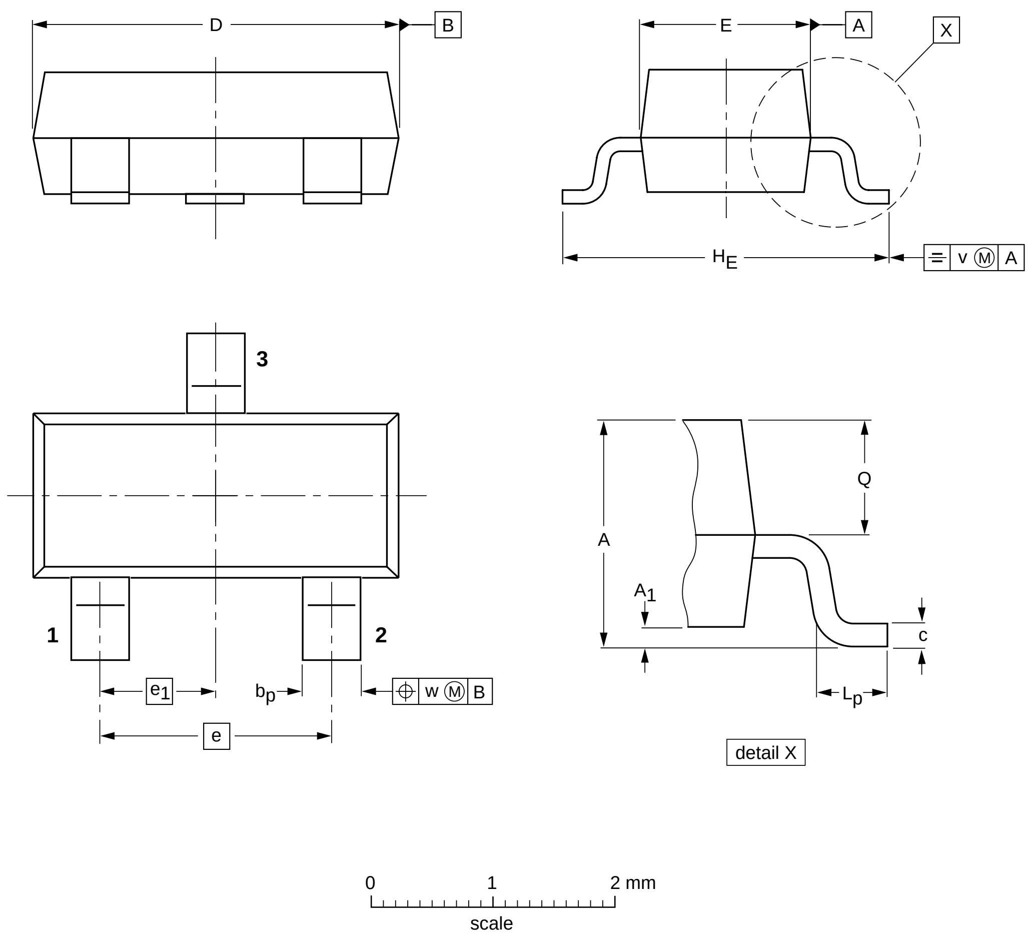



$I_D$ = 1.2 A; $V_{DD}$ = 20 V, 50 V, 80 V

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**

## 6. Package outline

**Plastic surface mounted package; 3 leads** **SOT23**




DIMENSIONS (mm are the original dimensions)

| UNIT | A | $A_1$ max. | $b_p$ | c | D | E | e | $e_1$ | $H_E$ | $L_p$ | Q | v | w |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.9 | 0.1 | 0.48<br>0.38 | 0.15<br>0.09 | 3.0<br>2.8 | 1.4<br>1.2 | 1.9 | 0.95 | 2.5<br>2.1 | 0.45<br>0.15 | 0.55<br>0.45 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT23 | | TO-236AB | | | | ~~97-02-28~~<br>99-09-13 |

**Fig 14. SOT23.**

## 7. Revision history

Table 5: Revision history

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 02 | 20030219 | - | **Product data (9397 750 11128)**<br>Modifications:<br>• Section 1.4 "Quick reference data" $I_D$ modified due to improved $R_{th}$.<br>• Section 1.4 "Quick reference data" $P_{tot}$ modified due to improved $R_{th}$.<br>• Section 3 "Limiting values" $I_D$, $I_{DM}$, $P_{tot}$, $I_S$, $I_{SM}$ modified due to improved $R_{th}$.<br>• Section 3 "Limiting values" Figure 3 SOA graph modified due to improved $R_{th}$.<br>• Section 4 "Thermal characteristics" $R_{th(j-sp)}$ improved.<br>• Section 4 "Thermal characteristics" Figure 4 to reflect the improvement in $R_{th(j-sp)}$. |
| 01 | 20030115 | - | **Product data (9397 750 10893)** |

## 8. Data sheet status

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|---|---|---|---|
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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