PMV50EPEA

30 V, P-channel Trench MOSFET

30 June 2016 — **Product data sheet**

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic level compatible
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

4. Quick reference data

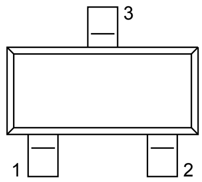
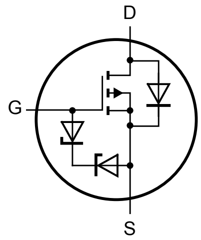
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	-30	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	V_{GS} = -10 V; T_{amb} = 25 °C	[1]	-	-	-4.2	A
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_D = -4.2 A; T_j = 25 °C		-	35	45	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 **TO-236AB (SOT23)**	
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMV50EPEA	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code [1]
PMV50EPEA	DQ%

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-30	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	V_{GS} = -10 V; T_{amb} = 25 °C	[1]	-	-4.2	A
		V_{GS} = -10 V; T_{amb} = 100 °C	[1]	-	-2.7	A
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	-16.9	A
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(init)}$ = 25 °C; I_D = -1.3 A; DUT in avalanche (unclamped)		-	19.5	mJ
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	480	mW
			[1]	-	1.2	W
		T_{sp} = 25 °C		-	6.95	W
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	-4	A
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[3] Measured between all pins.

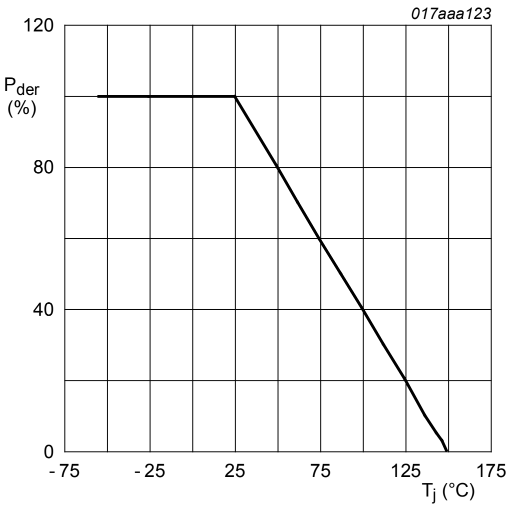


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

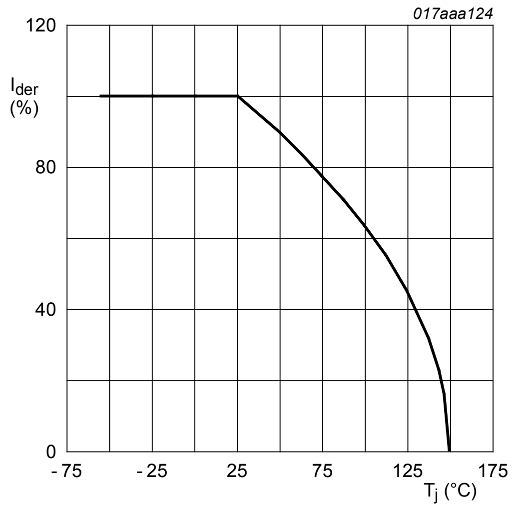
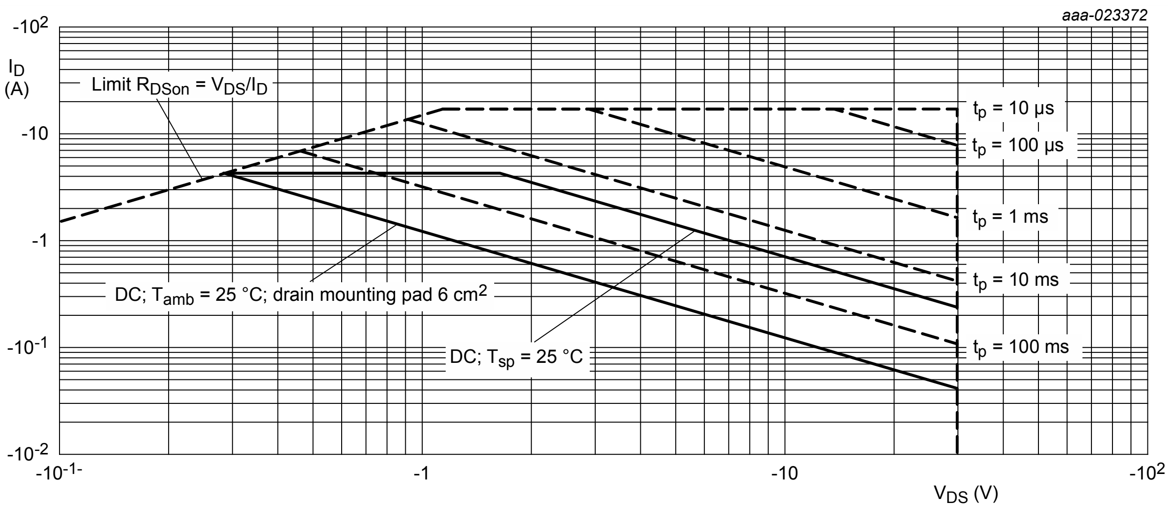


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$



I_{DM} = single pulse

Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

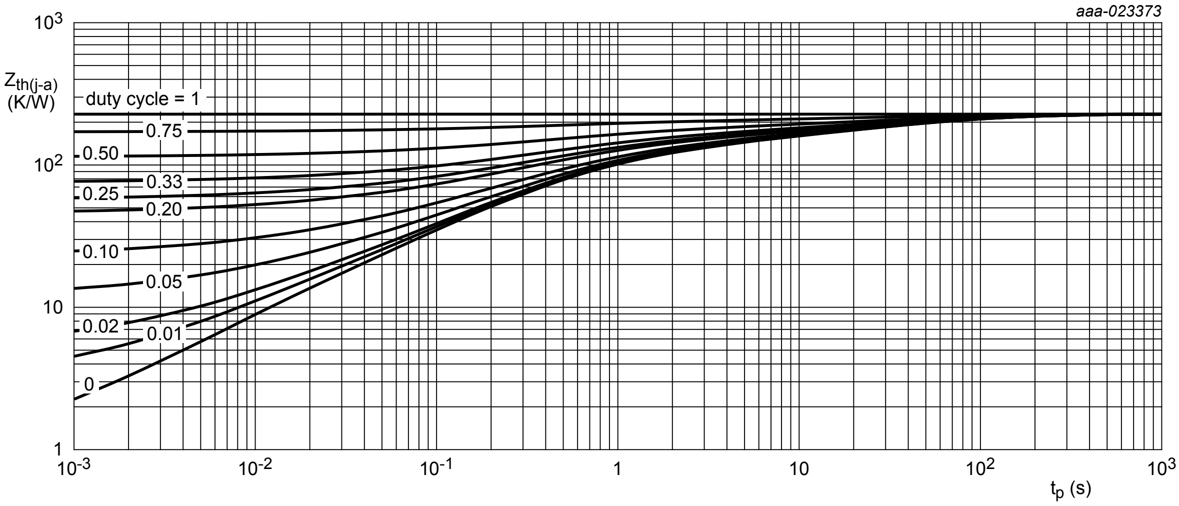
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	227	261	K/W
			[2]	-	91	104	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	13	18	K/W

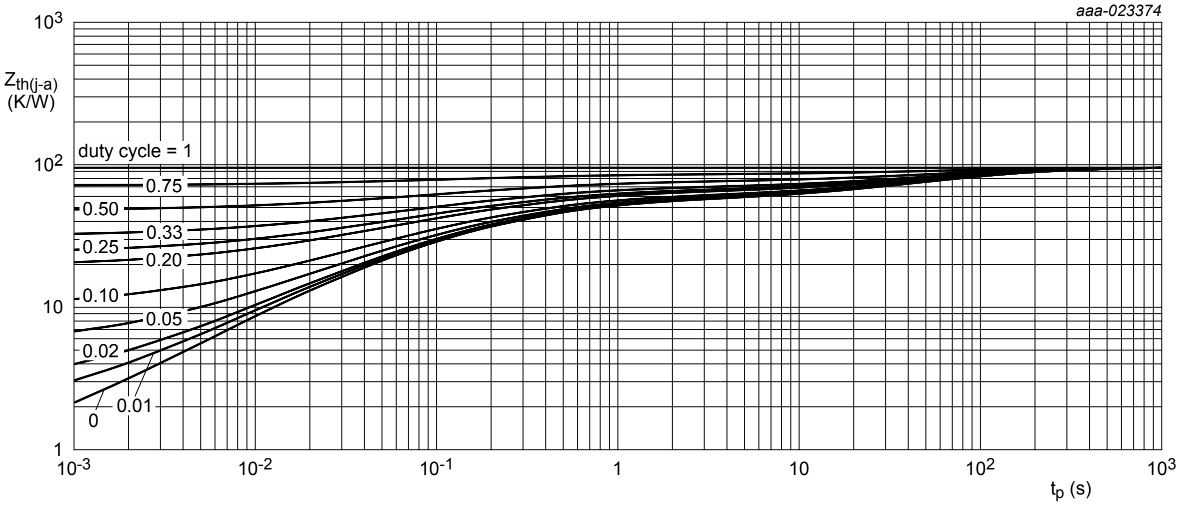
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2.



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



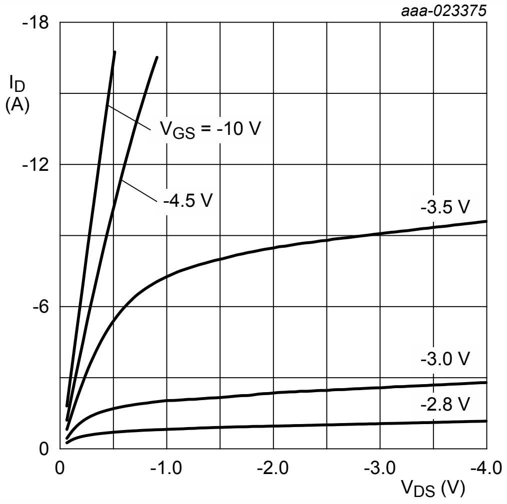
FR4 PCB, mounting pad for drain 6 cm^2

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

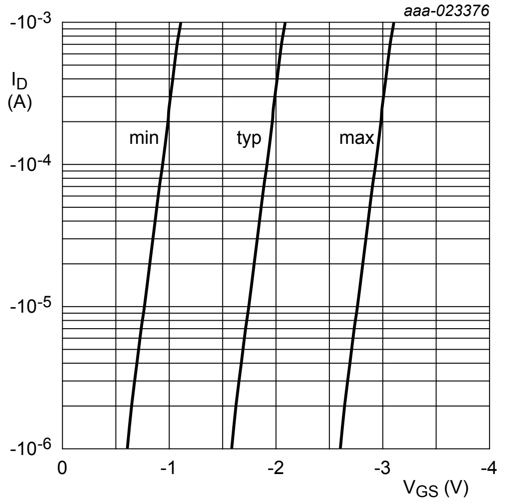
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 µA; V_{GS} = 0 V; T_j = 25 °C		-30	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -250 µA; V_{DS}=V_{GS}; T_j = 25 °C		-1	-2	-3	V
I_{DSS}	drain leakage current	V_{DS} = -30 V; V_{GS} = 0 V; T_j = 25 °C		-	-	-1	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	10	µA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-10	µA
		V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	-	2	µA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-2	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_D = -4.2 A; T_j = 25 °C		-	35	45	mΩ
		V_{GS} = -10 V; I_D = -4.2 A; T_j = 150 °C		-	51	67	mΩ
		V_{GS} = -4.5 V; I_D = -3.3 A; T_j = 25 °C		-	49	72	mΩ
g_{fs}	forward transconductance	V_{DS} = -10 V; I_D = -4.2 A; T_j = 25 °C		-	13.5	-	S
R_G	gate resistance	f = 1 MHz		-	13	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = -15 V; I_D = -4.2 A; V_{GS} = -10 V; T_j = 25 °C		-	12.8	19.2	nC
Q_{GS}	gate-source charge			-	2.2	-	nC
Q_{GD}	gate-drain charge			-	2.2	-	nC
C_{iss}	input capacitance	V_{DS} = -15 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	793	-	pF
C_{oss}	output capacitance			-	134	-	pF
C_{rss}	reverse transfer capacitance			-	84	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -15 V; I_D = -4.2 A; V_{GS} = -10 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	6	-	ns
t_r	rise time			-	19	-	ns
$t_{d(off)}$	turn-off delay time			-	36	-	ns
t_f	fall time			-	19	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = -4 A; V_{GS} = 0 V; T_j = 25 °C		-	-0.75	-1.2	V



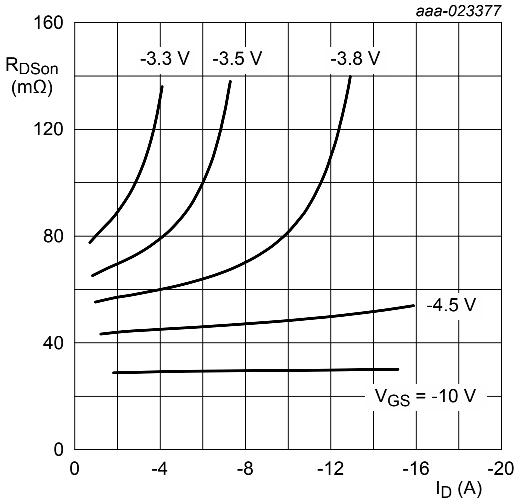
T_j = 25 °C

Fig. 6. **Output characteristics: drain current as a function of drain-source voltage; typical values**



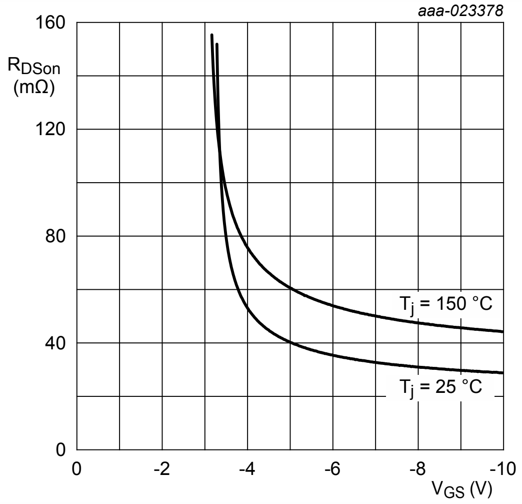
V_{DS} = -5 V
T_j = 25 °C

Fig. 7. **Sub-threshold drain current as a function of gate-source voltage**



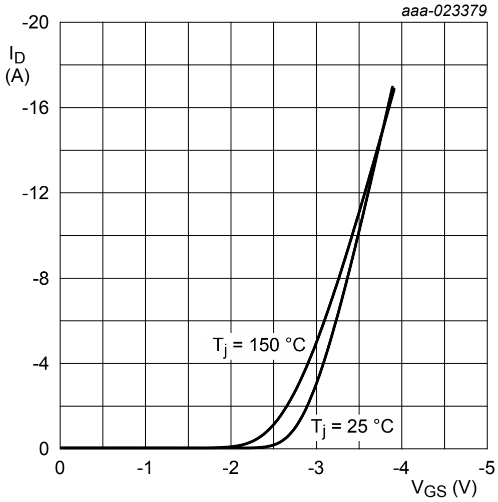
T_j = 25 °C

Fig. 8. **Drain-source on-state resistance as a function of drain current; typical values**



I_D = -4 A

Fig. 9. **Drain-source on-state resistance as a function of gate-source voltage; typical values**



$V_{DS} > I_D \times R_{DSon}$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

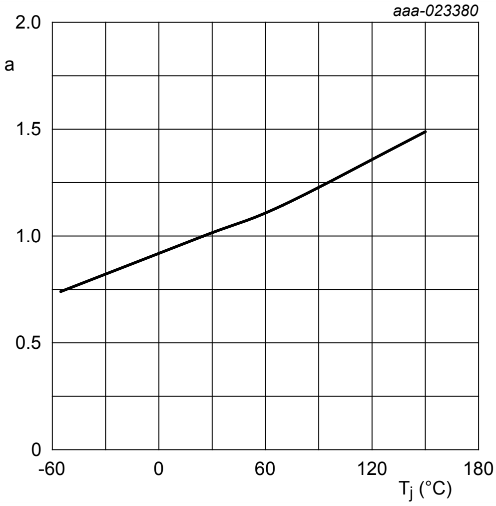
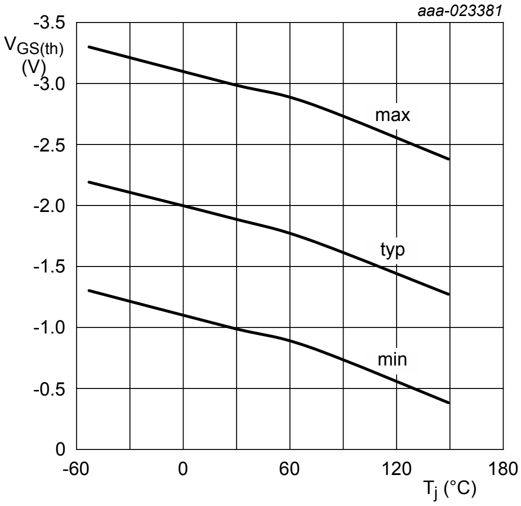


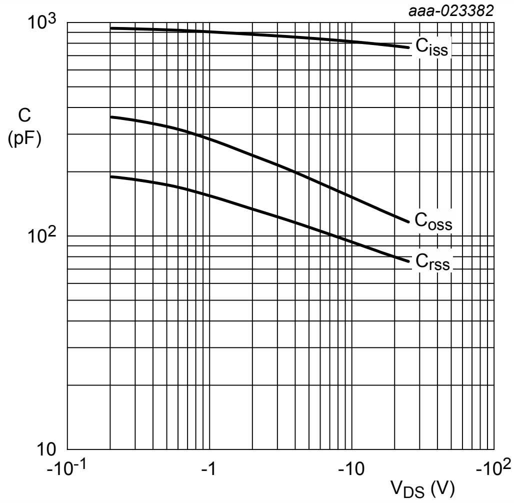
Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$



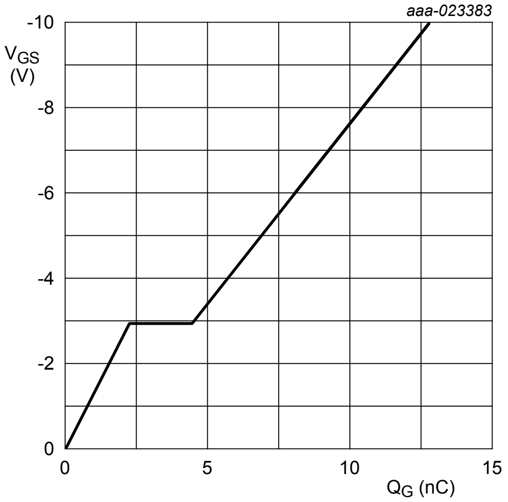
I_D = - 250 µA; $V_{DS} = V_{GS}$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{DS} = -15 V; I_D = -4 A

Fig. 14. Gate-source voltage as a function of gate charge; typical values

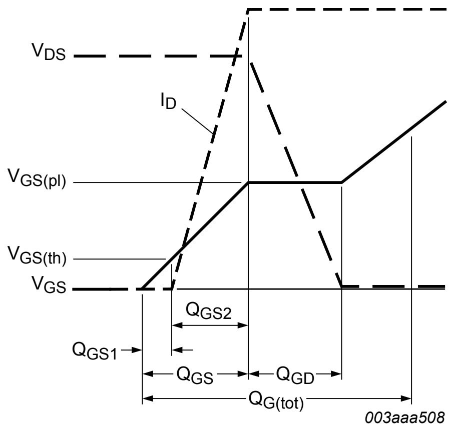
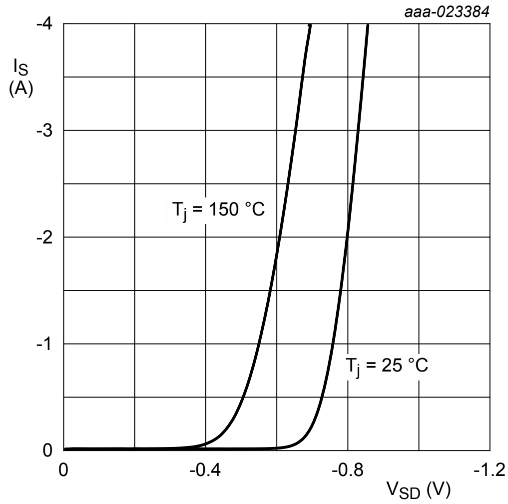


Fig. 15. Gate charge waveform definitions



V_{GS} = 0 V

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

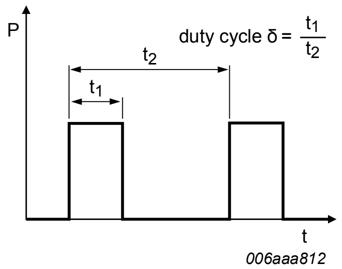


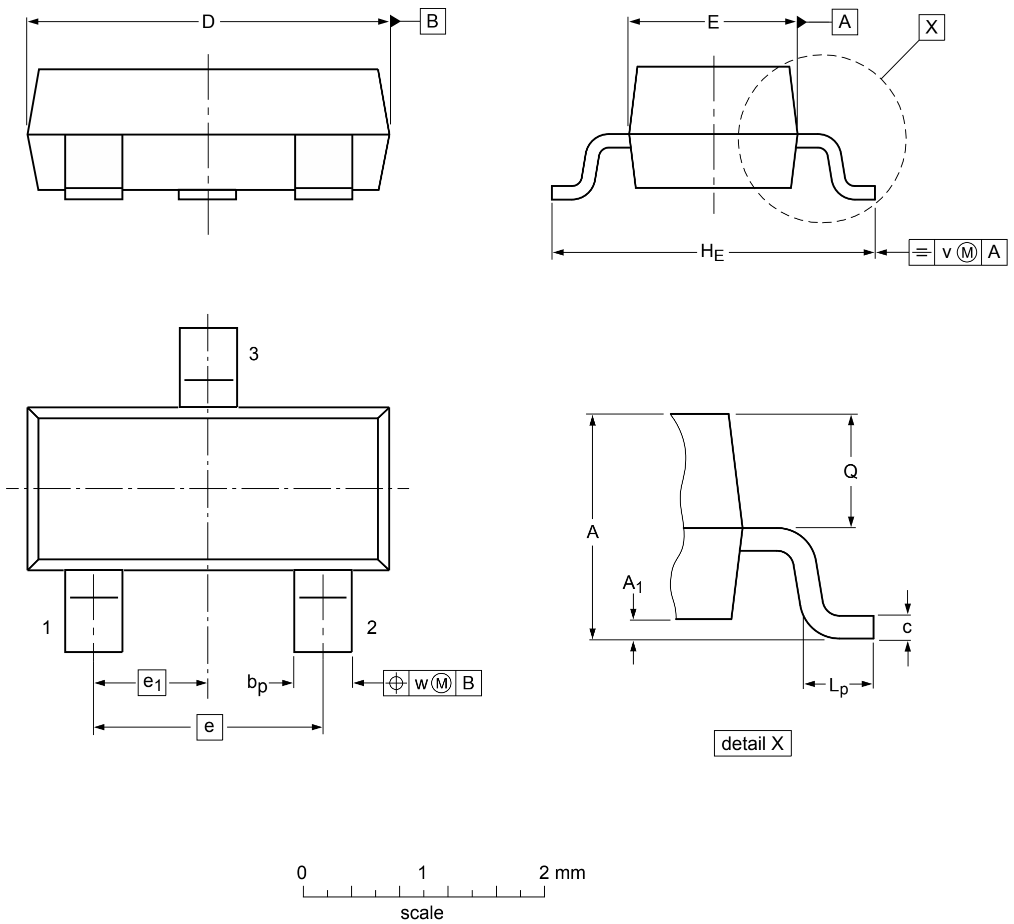
Fig. 17. Duty cycle definition

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

Plastic surface-mounted package; 3 leads **SOT23**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	max	1.1	0.1	0.48	0.15	3.0	1.4			2.5	0.45	0.55		
	nom							1.9	0.95				0.2	0.1
	min	0.9		0.38	0.09	2.8	1.2			2.1	0.15	0.45		

sot023_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				~~14-06-19~~ 14-09-22

Fig. 18. Package outline TO-236AB (SOT23)

13. Soldering

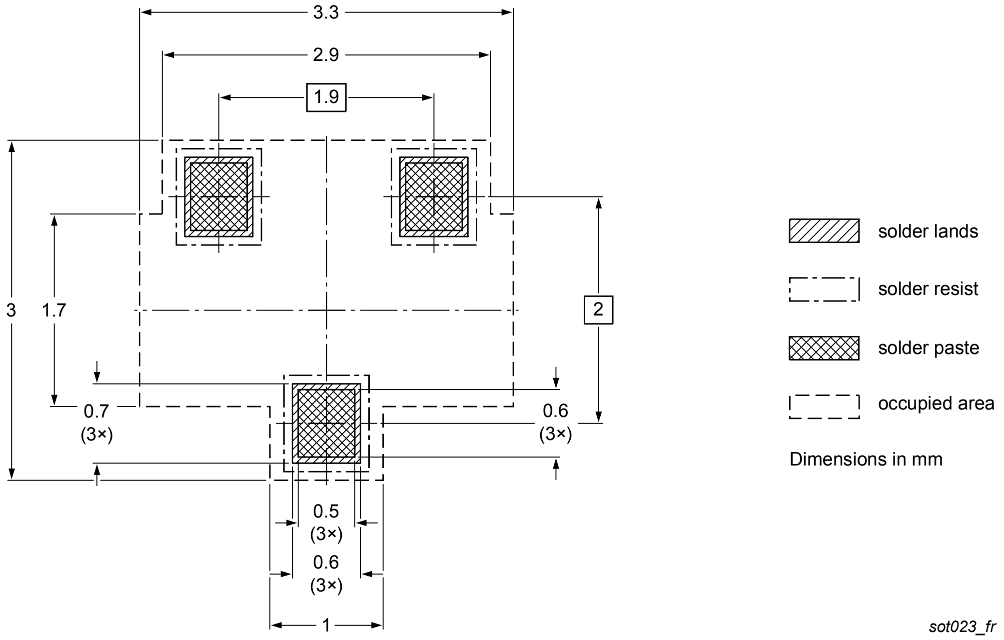


Fig. 19. Reflow soldering footprint for TO-236AB (SOT23)

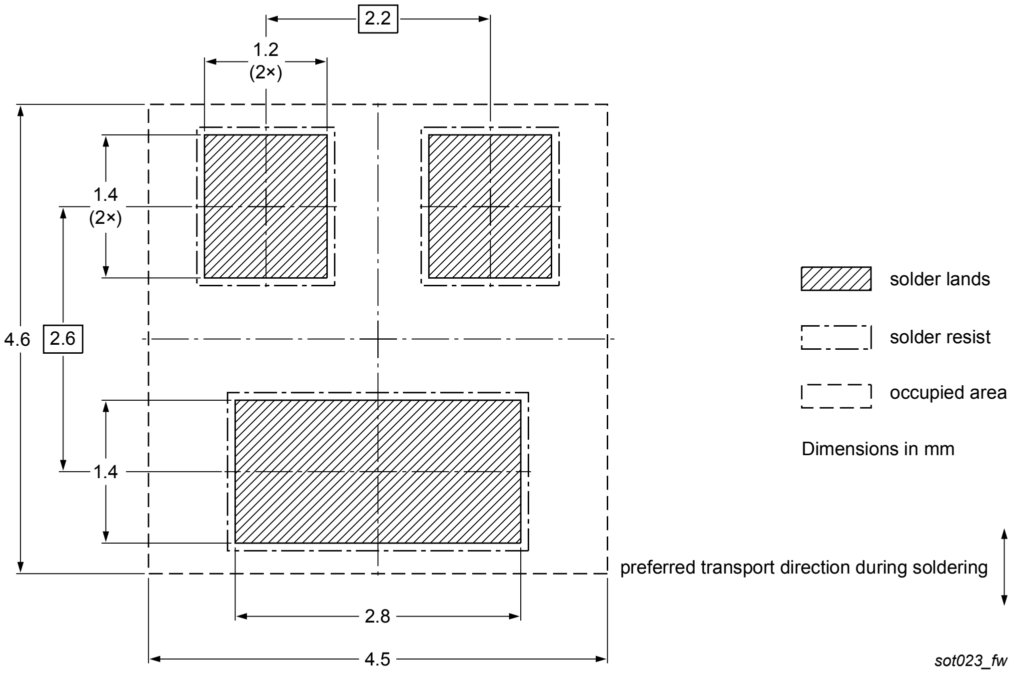


Fig. 20. Wave soldering footprint for TO-236AB (SOT23)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMV50EPEA v.1	20160630	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 30 June 2016

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