

# PMZB670UPE

# 20 V, single P-channel Trench MOSFET Rev. 3 — 23 March 2012

Product data sheet

#### 1. **Product profile**

### 1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Very fast switching
- Low threshold voltage
- Trench MOSFET technology
- ESD protection up to 2 kV
- Ultra thin package profile of 0.37 mm

### 1.3 Applications

- Relay driver
- High-speed line driver

- High-side loadswitch
- Switching circuits

#### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> = 25 °C		-	-	-20	V
V <sub>GS</sub>	gate-source voltage			-8	-	8	V
I <sub>D</sub>	drain current	$V_{GS}$ = -4.5 V; $T_{amb}$ = 25 °C	<u>[1]</u>	-	-	-680	mA
Static charact	eristics						
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -400 \text{ mA}; T_j = 25 \text{ °C}$		-	0.67	0.85	Ω

<sup>[1]</sup> Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.



### 2. Pinning information

Table 2. Pinning information

	•	,		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source	1 3	D
3	D	drain	Transparent top view  DFN1006B-3 (SOT883B)	G
				017aaa259

### 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMZB670UPE	DFN1006B-3	Leadless ultra small plastic package; 3 solder lands; body $1.0 \times 0.6 \times 0.37$ mm	SOT883B

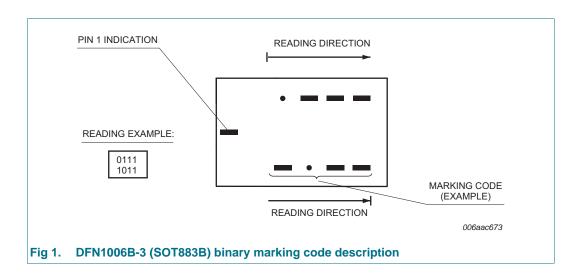
### 4. Marking

Table 4. Marking codes

Type number	Marking code <sup>[1]</sup>
PMZB670UPE	0000 1011

<sup>[1]</sup> For DFN1006B-3 (SOT883B) binary marking code description see Figure 1.

### 4.1 Binary marking code description



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### 5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25  ^{\circ}C$		-	-20	V
$V_{GS}$	gate-source voltage			-8	8	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C	<u>[1]</u>	-	-680	mΑ
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 100 °C	<u>[1]</u>	-	-425	mΑ
I <sub>DM</sub>	peak drain current	$T_{amb}$ = 25 °C; single pulse; $t_p \le 10 \mu s$		-	-2.7	Α
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	360	mW
			<u>[1]</u>	-	715	mW
		T <sub>sp</sub> = 25 °C		-	2700	mW
Tj	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
Source-drai	n diode					
Is	source current	T <sub>amb</sub> = 25 °C	<u>[1]</u>	-	-680	mΑ
ESD maxim	um rating					
V <sub>ESD</sub>	electrostatic discharge voltage	НВМ	[3]	-	2000	V

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.

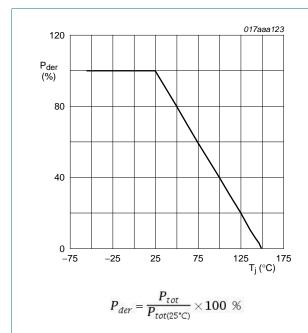
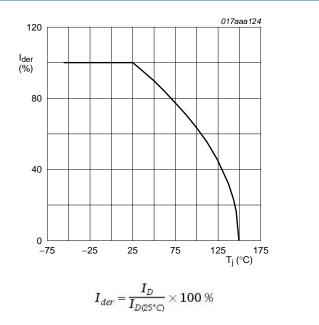


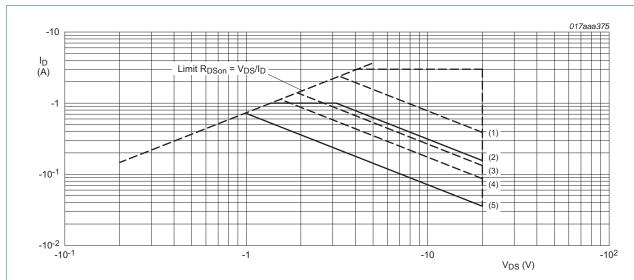
Fig 2. Normalized total power dissipation as a function of junction temperature



ig 3. Normalized continuous drain current as a function of junction temperature

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I<sub>DM</sub> = single pulse

- (1)  $t_p = 1 \text{ ms}$
- (2) DC;  $T_{sp} = 25 \, ^{\circ}\text{C}$
- (3)  $t_p = 10 \text{ ms}$
- (4)  $t_p = 100 \text{ ms}$
- (5) DC;  $T_{amb} = 25 \, ^{\circ}C$ ; drain mounting pad 1 cm<sup>2</sup>

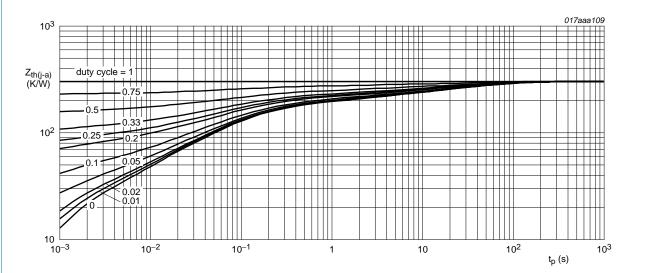
Fig 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

### 6. Thermal characteristics

Table 6. Thermal characteristics

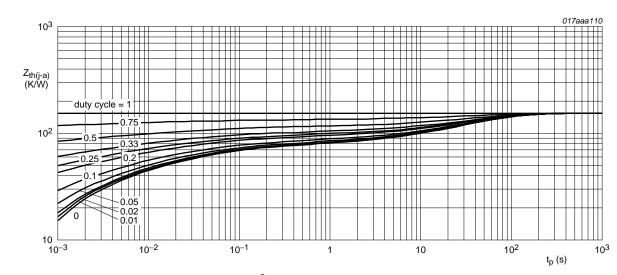
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance	in free air	<u>[1]</u>	-	305	360	K/W
	from junction to ambient		<u>[2]</u>	-	150	175	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point			-	-	40	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.



FR4 PCB, standard footprint

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm<sup>2</sup>

Fig 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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### 7. Characteristics

Table 7. Characteristics

Table 7.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	-20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \ \mu A; \ V_{DS} = V_{GS}; \ T_j = 25 \ ^{\circ}C$	-0.5	-0.9	-1.3	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = -20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-1	μΑ
		$V_{DS} = -20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$	-	-	-10	μΑ
I <sub>GSS</sub>	gate leakage current	$V_{GS} = 8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-2	μΑ
		$V_{GS} = -8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-2	μΑ
		$V_{GS} = 4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-0.5	μΑ
		$V_{GS} = -4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-0.5	μΑ
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = -4.5 V; $I_D$ = -400 mA; $T_j$ = 25 °C	-	0.67	0.85	Ω
		$V_{GS}$ = -4.5 V; $I_{D}$ = -400 mA; $T_{j}$ = 150 °C	-	1.1	1.4	Ω
		$V_{GS}$ = -2.5 V; $I_D$ = -200 mA; $T_j$ = 25 °C	-	1.2	1.5	Ω
		$V_{GS} = -1.8 \text{ V}; I_D = -10 \text{ mA}; T_j = 25 \text{ °C}$	-	1.8	2.8	Ω
9 <sub>fs</sub>	forward transconductance	$V_{DS} = -10 \text{ V}; I_D = -200 \text{ mA}; T_j = 25 \text{ °C}$	-	610	-	mS
Dynamic	characteristics					
Q <sub>G(tot)</sub>	total gate charge	$V_{DS} = -10 \text{ V}; I_D = -400 \text{ mA};$	-	0.76	1.14	nC
$Q_{GS}$	gate-source charge	$V_{GS} = -4.5 \text{ V}; T_j = 25 \text{ °C}$	-	0.28	-	nC
$Q_{GD}$	gate-drain charge		-	0.18	-	nC
C <sub>iss</sub>	input capacitance	$V_{DS} = -10 \text{ V; } f = 1 \text{ MHz; } V_{GS} = 0 \text{ V;}$	-	58	87	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C	-	21	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	12	-	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = -10 V; $R_L$ = 250 $\Omega$ ; $V_{GS}$ = -4.5 V;	-	18	36	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	30	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	80	160	ns
t <sub>f</sub>	fall time		-	72	-	ns
Source-di	rain diode					
$V_{SD}$	source-drain voltage	$I_S = -300 \text{ mA}; V_{GS} = 0 \text{ V}; T_i = 25 \text{ °C}$	-0.48	-0.84	-1.2	V

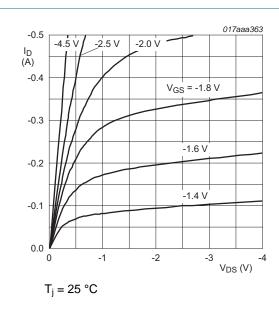
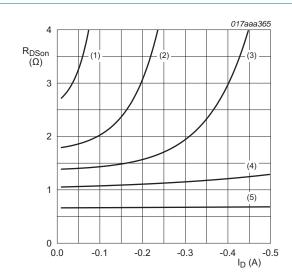


Fig 7. Output characteristics: drain current as a function of drain-source voltage; typical values



 $T_i = 25 \, ^{\circ}C$ 

(1)  $V_{GS} = -1.5 \text{ V}$ 

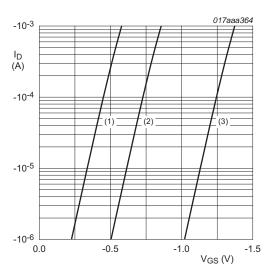
(2)  $V_{GS} = -1.8 \text{ V}$ 

(3)  $V_{GS} = -2.0 \text{ V}$ 

(4)  $V_{GS} = -2.5 \text{ V}$ 

(5)  $V_{GS} = -4.5 \text{ V}$ 

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



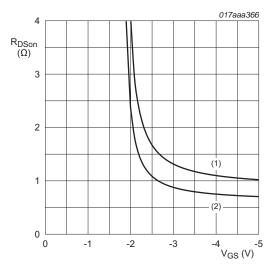
 $T_{j} = 25 \, ^{\circ}\text{C}; \, V_{DS} = -5 \, \text{V}$ 

(1) minimum values

(2) typical values

(3) maximum values

Fig 8. Sub-threshold drain current as a function of gate-source voltage

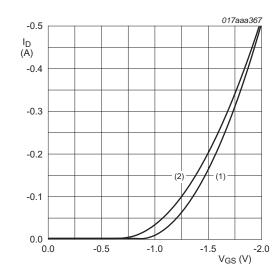


 $I_D = -400 \text{ mA}$ 

(1)  $T_i = 150 \, ^{\circ}C$ 

(2)  $T_i = 25 \, ^{\circ}C$ 

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

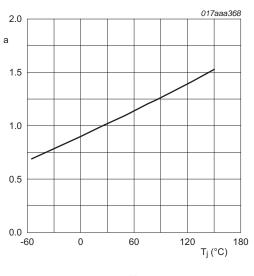


 $V_{DS} > I_D \times R_{DSon}$ 

(1) 
$$T_j = 25 \, ^{\circ}C$$

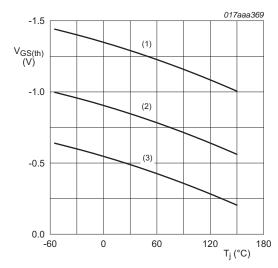
(2) 
$$T_i = 150 \, ^{\circ}\text{C}$$

Fig 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values



 $\mathbf{a} = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$ 

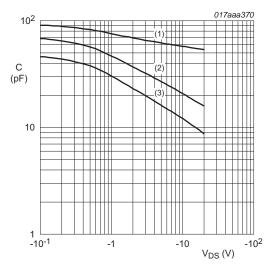
Fig 12. Normalized drain-source on-state resistance as a function of ambient temperature; typical values



 $I_D$  = -0.25 mA;  $V_{DS}$  =  $V_{GS}$ 

- (1) maximum values
- (2) typical values
- (3) minimum values

Fig 13. Gate-source threshold voltage as a function of junction temperature



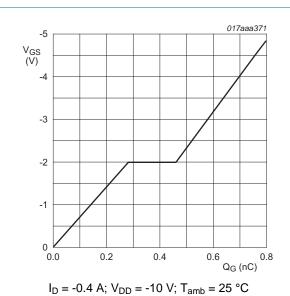
 $f = 1 MHz; V_{GS} = 0 V$ 

- (1) C<sub>iss</sub>
- (2) C<sub>oss</sub>
- (3) C<sub>rss</sub>

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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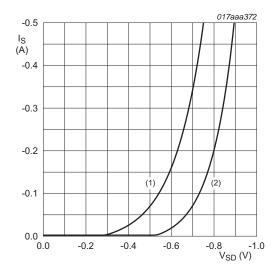
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V<sub>DS</sub> — V<sub>GS(pl)</sub> V<sub>GS(th)</sub> V<sub>GS</sub> — Q<sub>GS1</sub> Q<sub>GS2</sub> — Q<sub>GD</sub> — Q<sub>GD</sub> — Q<sub>GG(tot)</sub> 017aaa137

Fig 15. Gate-source voltage as a function of gate charge; typical values

Fig 16. Gate charge waveform definitions



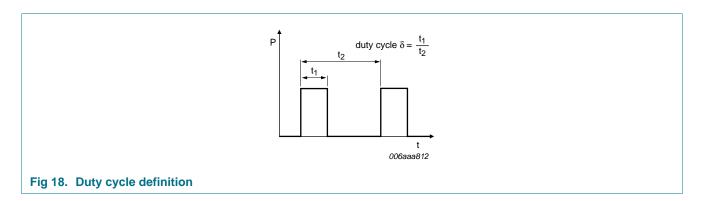
 $V_{GS} = 0 V$ 

(1)  $T_{amb} = 150 \, ^{\circ}C$ 

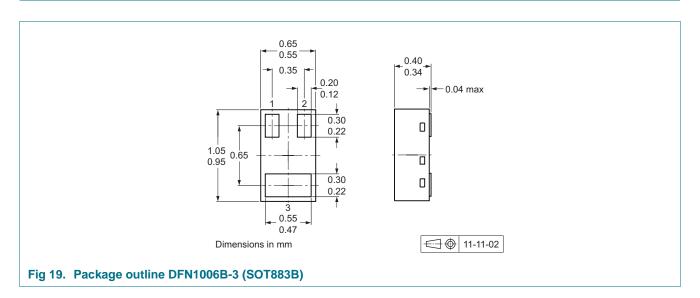
(2)  $T_{amb} = 25 \, ^{\circ}C$ 

Fig 17. Source current as a function of source-drain voltage; typical values

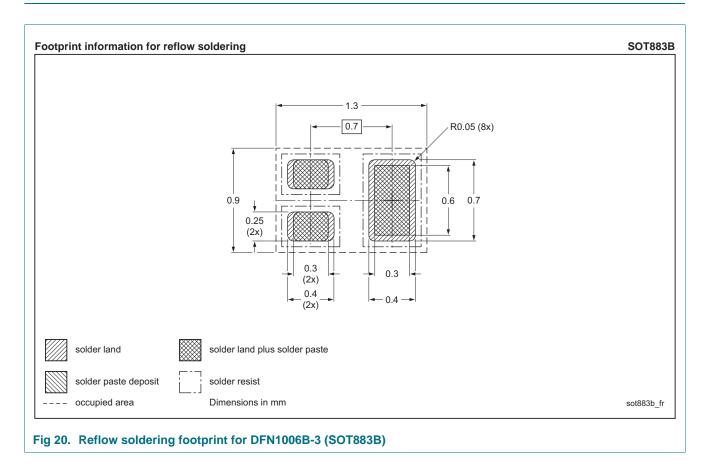
### 8. Test information



### 9. Package outline



### 10. Soldering



### 11. Revision history

### Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMZB670UPE v.3	20120323	Product data sheet	-	PMZB670UPE v.2
Modifications:	• 1.2 "Features	and benefits" is corrected.		
PMZB670UPE v.2	20120207	Product data sheet	-	PMZB670UPE v.1
PMZB670UPE v.1	20120131	Product data sheet	-	-

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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## PMZB670UPE

### 20 V, single P-channel Trench MOSFET

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