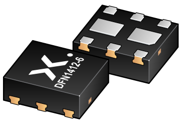


# PRMH10

## 50 V, 100 mA NPN/NPN Resistor-Equipped double Transistors (RET)

14 September 2018 Product data sheet

## 1. General description

NPN/NPN Resistor-Equipped double Transistors (RET) in an ultra small DFN1412-6 (SOT1268) leadless Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PRMD10.

## 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm
- AEC-Q101 qualified

## 3. Applications

- Digital applications
- Cost-saving alternative to BC847/BC857 series in digital applications
- Control of IC inputs
- Switching loads

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Per transistor** | | | | | | | |
| $V_{CEO}$ | collector-emitter voltage | open base | | - | - | 50 | V |
| $I_O$ | output current | | | - | - | 100 | mA |
| $h_{FE}$ | DC current gain | $V_{CE}$ = 5 V; $I_C$ = 10 mA; $T_{amb}$ = 25 °C | | 100 | - | - | |
| R1 | bias resistor 1 | $T_{amb}$ = 25 °C | [1] | 1.54 | 2.2 | 2.86 | kΩ |
| R2/R1 | bias resistor ratio | | [1] | 17 | 21 | 26 | |

[1] See section "Test information" for resistor calculation and test conditions.

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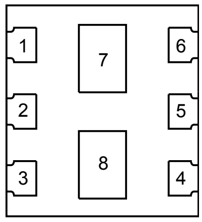
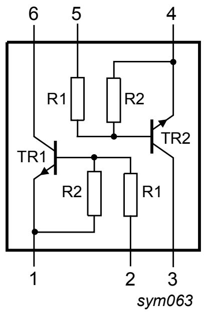
## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | GND1 | GND (emitter) TR1 | <br>Transparent top view<br>DFN1412-6<br>(SOT1268) |  |
| 2 | I1 | input (base) TR1 | | |
| 3 | O2 | output (collector) TR2 | | |
| 4 | GND2 | GND (emitter) TR2 | | |
| 5 | I2 | input (base) TR2 | | |
| 6 | O1 | output (collector) TR1 | | |
| 7 | O1 | output (collector) TR1 | | |
| 8 | O2 | output (collector) TR2 | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PRMH10 | DFN1412-6 | plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.4 mm x 1.2 mm x 0.47 mm | SOT1268 |

## 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PRMH10 | C3 |

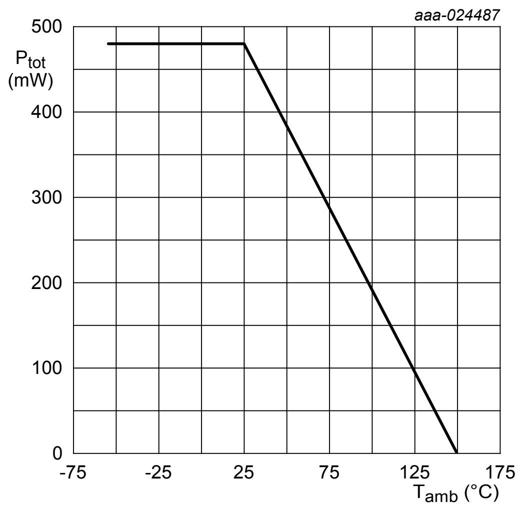
## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Per transistor** | | | | | | |
| $V_{CBO}$ | collector-base voltage | open emitter | | - | 50 | V |
| $V_{CEO}$ | collector-emitter voltage | open base | | - | 50 | V |
| $V_{EBO}$ | emitter-base voltage | open collector | | - | 5 | V |
| $V_I$ | input voltage | positive | | - | 12 | V |
| | | negative | | - | -5 | V |
| $I_O$ | output current | | | - | 100 | mA |
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | [1] | - | 325 | mW |
| **Per device** | | | | | | |
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | [1] | - | 480 | mW |
| $T_j$ | junction temperature | | | - | 150 | °C |
| $T_{amb}$ | ambient temperature | | | -55 | 150 | °C |
| $T_{stg}$ | storage temperature | | | -65 | 150 | °C |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.




FR4 PCB, standard footprint

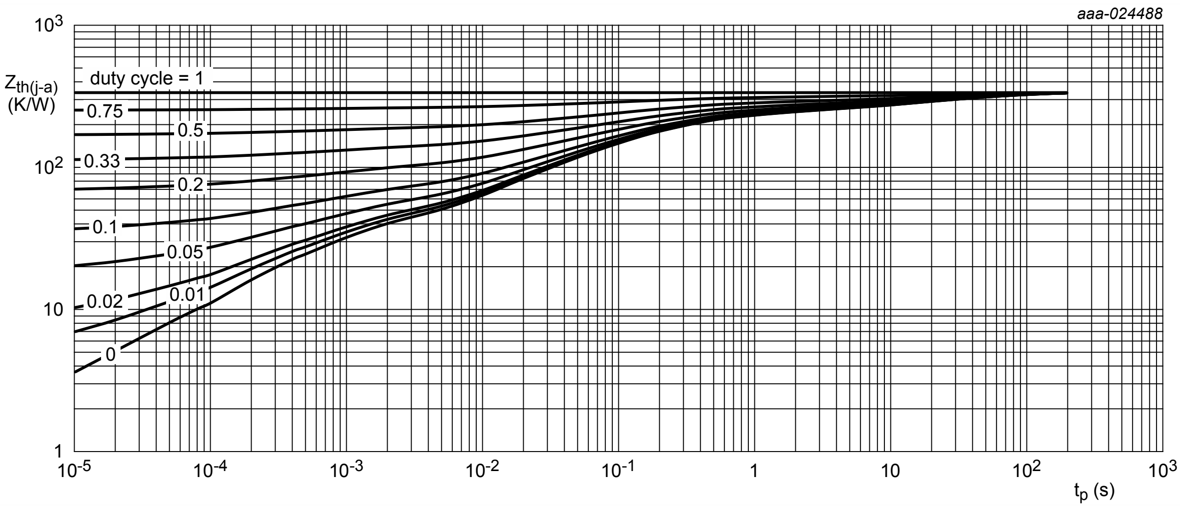
**Fig. 1. Per device: Power derating curve**

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Per transistor** | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 385 | K/W |
| **Per device** | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 261 | K/W |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.




FR4 PCB, standard footprint

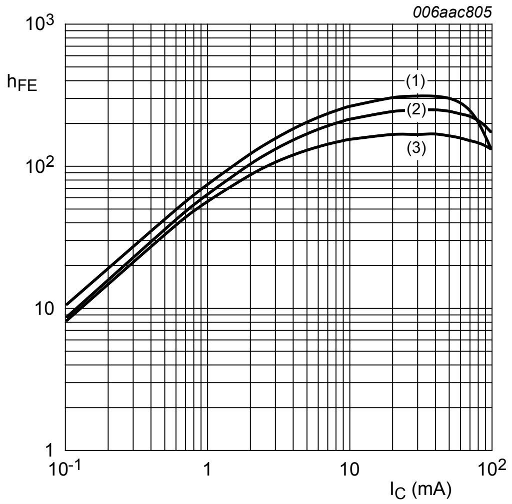
**Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

# 10. Characteristics

**Table 7. Characteristics**

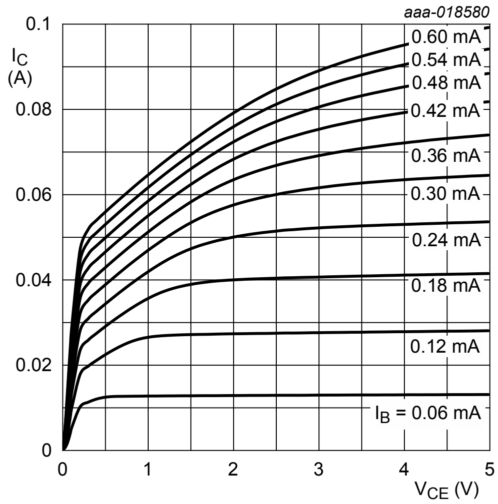
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Per transistor** | | | | | | | |
| $I_{CEO}$ | collector-emitter cut-off current | $V_{CE}$ = 30 V; $I_B$ = 0 A; $T_{amb}$ = 25 °C | | - | - | 100 | nA |
| | | $V_{CE}$ = 30 V; $I_B$ = 0 A; $T_j$ = 150 °C | | - | - | 5 | µA |
| $I_{CBO}$ | collector-base cut-off current | $V_{CB}$ = 50 V; $I_E$ = 0 A; $T_{amb}$ = 25 °C | | - | - | 100 | nA |
| $I_{EBO}$ | emitter-base cut-off current | $V_{EB}$ = 5 V; $I_C$ = 0 A; $T_{amb}$ = 25 °C | | - | - | 180 | µA |
| $h_{FE}$ | DC current gain | $V_{CE}$ = 5 V; $I_C$ = 10 mA; $T_{amb}$ = 25 °C | | 100 | - | - | |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = 5 mA; $I_B$ = 0.25 mA; $T_{amb}$ = 25 °C | | - | - | 100 | mV |
| $V_{I(off)}$ | off-state input voltage | $V_{CE}$ = 5 V; $I_C$ = 100 µA; $T_{amb}$ = 25 °C | | - | 0.6 | 0.5 | V |
| $V_{I(on)}$ | on-state input voltage | $V_{CE}$ = 0.3 V; $I_C$ = 5 mA; $T_{amb}$ = 25 °C | | 1.1 | 0.75 | - | V |
| R1 | bias resistor 1 | $T_{amb}$ = 25 °C | [1] | 1.54 | 2.2 | 2.86 | kΩ |
| R2/R1 | bias resistor ratio | | [1] | 17 | 21 | 26 | |
| $C_C$ | collector capacitance | $V_{CB}$ = 10 V; $I_E$ = 0 A; $i_e$ = 0 A; f = 1 MHz; $T_{amb}$ = 25 °C | | - | - | 2.5 | pF |
| $f_T$ | transition frequency | $V_{CE}$ = 5 V; $I_C$ = 10 mA; f = 100 MHz; $T_{amb}$ = 25 °C | [2] | - | 230 | - | MHz |

[1] See section "Test information" for resistor calculation and test conditions.
[2] Characteristics of built-in transistor



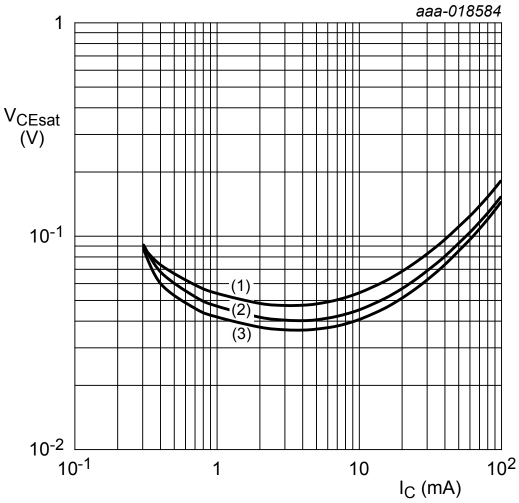

$V_{CE}$ = 5 V
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 3. DC current gain as a function of collector current; typical values**



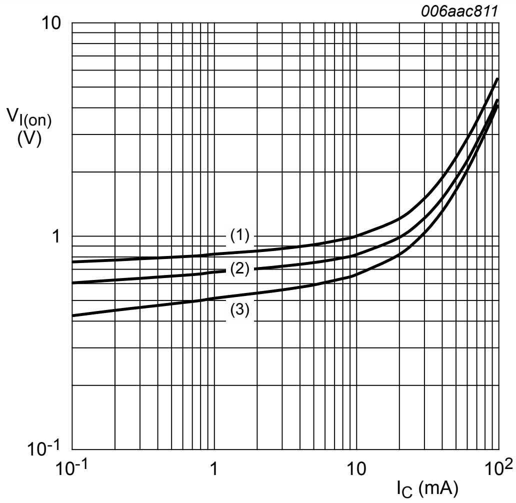

$T_{amb}$ = 25 °C

**Fig. 4. Collector current as a function of collector-emitter voltage; typical values**



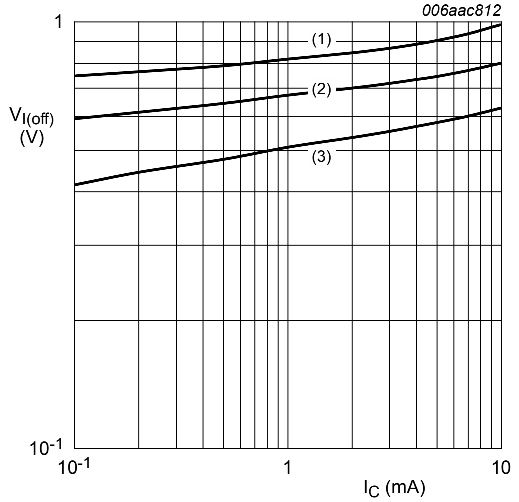

$I_C/I_B = 20$
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 5. Collector-emitter saturation voltage as a function of collector current; typical values**



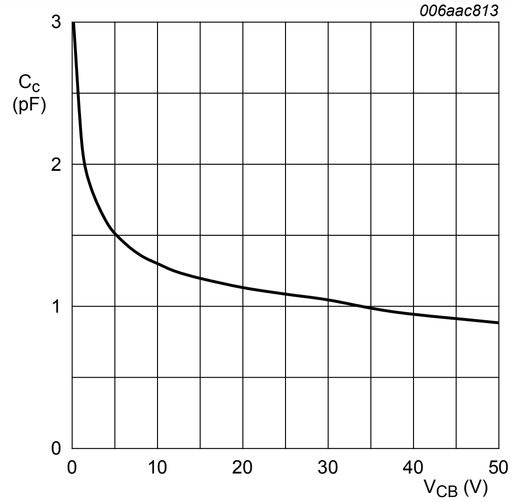

$V_{CE}$ = 0.3 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 6. On-state input voltage as a function of collector current; typical values**



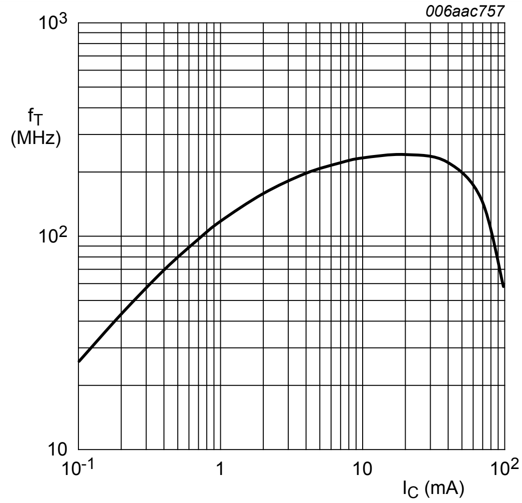

$V_{CE}$ = 5 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 7. Off-state input voltage as a function of collector current; typical values**




f = 1 MHz; $T_{amb}$ = 25 °C

**Fig. 8. Collector capacitance as a function of collector-base voltage; typical values**




$V_{CE}$ = 5 V; $T_{amb}$ = 25 °C

**Fig. 9. Transition frequency as a function of collector current; typical values of built-in transistor**

## 11. Test information

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

### Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I_{I2}) - V(I_{I1})}{I_{I2} - I_{I1}}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I_{I4}) - V(I_{I3})}{R1 \cdot (I_{I4} - I_{I3})} - 1$$

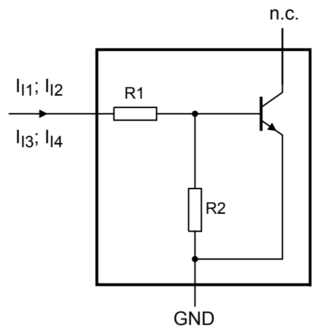



**Fig. 10. Per transistor: Resistor test circuit**

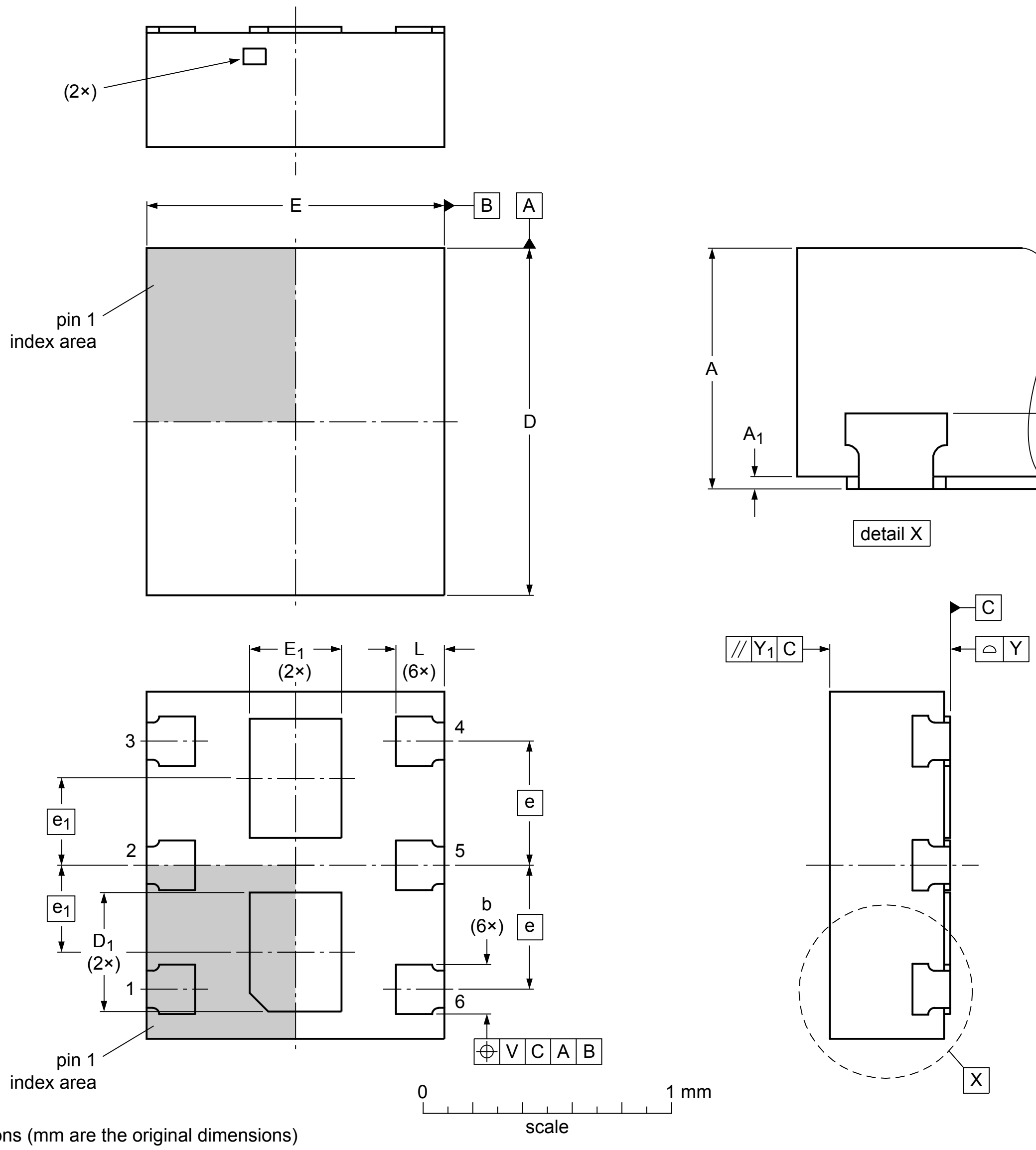
### Resistor test conditions

**Table 8. Resistor test conditions**

| R1 (kΩ) | R2 (kΩ) | Test conditions | | | |
|---|---|---|---|---|---|
| | | $I_{I1}$ | $I_{I2}$ | $I_{I3}$ | $I_{I4}$ |
| 2.2 | 47 | 90 µA | 140 µA | -55 µA | -105 µA |

# 12. Package outline

**DFN1412-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.4 x 1.2 x 0.47 mm** **SOT1268**




Dimensions (mm are the original dimensions)

| Unit(1) | | A | $A_1$ | b | D | $D_1$ | E | $E_1$ | e | $e_1$ | L | T | V | Y | $Y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | min | 0.44 | 0.00 | 0.15 | 1.35 | 0.43 | 1.15 | 0.32 | | | 0.145 | 0.10 | | | |
| | nom | 0.47 | | 0.20 | 1.40 | 0.48 | 1.20 | 0.37 | 0.5 | 0.35 | 0.195 | 0.16 | 0.1 | 0.05 | 0.05 |
| | max | 0.50 | 0.04 | 0.25 | 1.45 | 0.53 | 1.25 | 0.42 | | | 0.245 | 0.22 | | | |

Note
1. Dimension A is including plating thickness.

*sot1268_po*

| Outline version | References: IEC | References: JEDEC | References: JEITA | | European projection | Issue date |
|---|---|---|---|---|---|---|
| SOT1268 | | - - - | | | | ~~18-08-23~~ 18-09-11 |

**Fig. 11. Package outline DFN1412-6 (SOT1268)**

# 13. Soldering

**Footprint information for reflow soldering of DFN1412-6 package** **SOT1268**

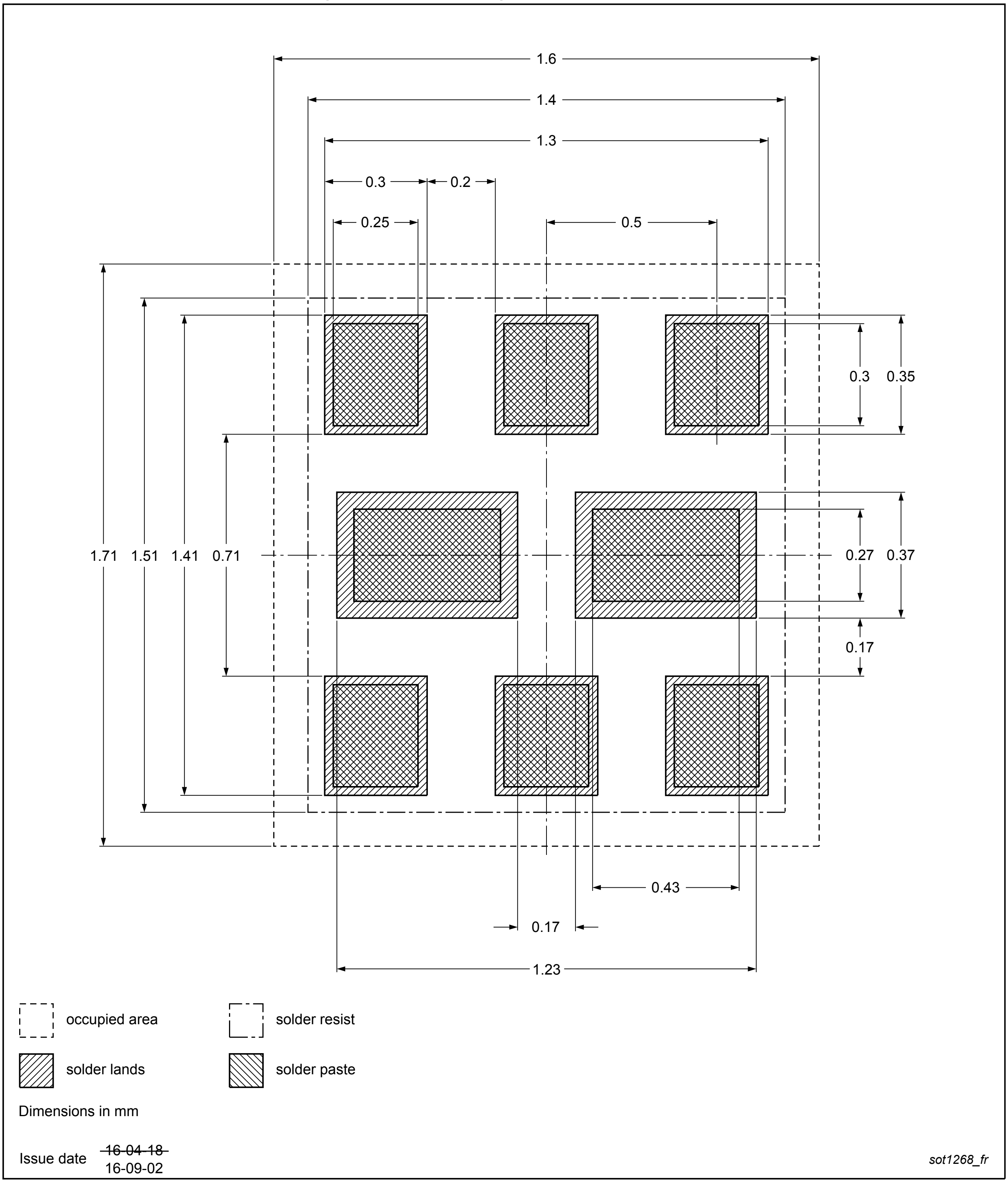



**Fig. 12. Reflow soldering footprint for DFN1412-6 (SOT1268)**

## 14. Revision history

**Table 9. Revision history**

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PRMH10 v.2 | 20180914 | Product data sheet | - | PRMH10 v.1 |
| Modifications: | • Package outline drawing updated: Unit T added | | | |
| PRMH10 v.1 | 20170727 | Product data sheet | - | - |

# 15. Legal information

### Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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## Contents





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**Date of release: 14 September 2018**