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Team Nexperia

Ultra low capacitance double rail-to-rail ESD protection

Rev. 02 — 19 February 2009

Product data sheet

1. Product profile

1.1 General description

Ultra low capacitance double rail-to-rail ElectroStatic Discharge (ESD) protection devices in leadless ultra small Surface-Mounted Device (SMD) plastic packages.

The devices are designed to protect two Hi-Speed data lines or high-frequency signal lines from the damage caused by ESD and other transients.

PRTR5V0U2F and PRTR5V0U2K integrate two ultra low capacitance rail-to-rail ESD protection channels and one additional ESD protection diode each to ensure signal line protection even if no supply voltage is available.

Table 1.Product overview

Type number	Package		Package configuration
	NXP	JEDEC	
PRTR5V0U2F	SOT886	MO-252	leadless ultra small
PRTR5V0U2K	SOT891	-	leadless ultra small

1.2 Features

- ESD protection of two Hi-Speed data lines or high-frequency signal lines
- Ultra low input/output to ground capacitance: C_(I/O-GND) = 1 pF
- ESD protection up to 8 kV
- IEC 61000-4-2, level 4 (ESD)
- Very low clamping voltage due to an integrated additional ESD protection diode
- Very low reverse current
- AEC-Q101 qualified
- Leadless ultra small SMD plastic packages

1.3 Applications

- USB 2.0 interfaces
- Digital Video Interface (DVI) / High Definition Multimedia Interface (HDMI) interfaces
- Mobile and cordless phones
- Personal Digital Assistants (PDA)
- Digital cameras
- Wide Area Network (WAN) / Local Area Network (LAN) systems
- PCs, notebooks, printers and other PC peripherals



Ultra low capacitance double rail-to-rail ESD protection

1.4 Quick reference data

Table 2. Quick reference data

 $T_{amb} = 25 \circ C$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per channe	el					
C _(I/O-GND)	input/output to ground capacitance	f = 1 MHz; V _(I/O-GND) = 0 V	<u>[1]</u> _	1.0	1.5	pF
C _(I/O-I/O)	input/output to input/output capacitance	f = 1 MHz; V _(I/O-I/O) = 0 V	<u>[2]</u> _	0.6	-	pF
Zener diod	e					
V _{RWM}	reverse standoff voltage		[3] _	-	5.5	V
C _{sup}	supply pin to ground capacitance	f = 1 MHz; V _{CC} = 0 V	<u>[3]</u> _	16	-	pF

[1] Measured from pin 1, 3, 4 or 6 to ground.

[3] Measured from pin 5 to ground.

2. Pinning information

Table	3. Pinning			
Pin	Symbol	Description	Simplified outline	Graphic symbol
PRTF	R5V0U2F (SOT	886)		
1	I/O1	input/output 1		
2	GND	ground		
3	I/O2	input/output 2		<u></u> _₩+₩_
4	I/O2	input/output 2		
5	V _{CC}	supply voltage		
6	I/O1	input/output 1	6 5 4 bottom view	3 006aab349

PRTR5V0U2K (SOT891)

1	I/O1	input/output 1		
2	GND	ground		
3	I/O2	input/output 2		<u></u> <u></u>
4	I/O2	input/output 2		
5	V _{CC}	supply voltage		
6	I/O1	input/output 1	6 5 4 bottom view	

2 of 12

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Ultra low capacitance double rail-to-rail ESD protection

3. Ordering information

Table 4. Ordering information					
Type number	Package				
	Name	Description	Version		
PRTR5V0U2F	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1.45 \times 0.5$ mm	SOT886		
PRTR5V0U2K	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1 \times 0.5$ mm	SOT891		

4. Marking

Table 5. Marking codes	
Type number	Marking code
PRTR5V0U2F	PF
PRTR5V0U2K	РК

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per device					
T _{amb}	ambient temperature		-40	+85	°C
T _{stg}	storage temperature		-55	+125	°C

Table 7. ESD maximum ratings

 $T_{amb} = 25 \circ C$ unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
Per chan	nel					
V _{ESD} electrostatic discharge voltage		IEC 61000-4-2 (contact discharge)	[1][2]	-	8	kV
		MIL-STD-883 (human body model)	[2]	-	10	kV

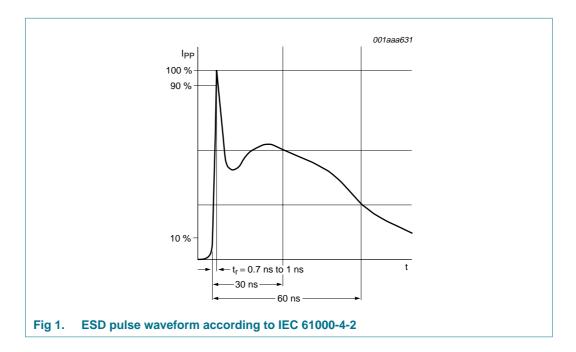
[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1, 3, 4 or 6 to pin 2 or 5.

Ultra low capacitance double rail-to-rail ESD protection

	Table 8.	ESD standards compliance
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Standard	Conditions
Per channel	
IEC 61000-4-2; level 4 (ESD)	> 8 kV (contact)
MIL-STD-883; class 3 (human body model)	> 4 kV



PRTR5V0U2F_PRTR5V0U2K_2

Ultra low capacitance double rail-to-rail ESD protection

6. Characteristics

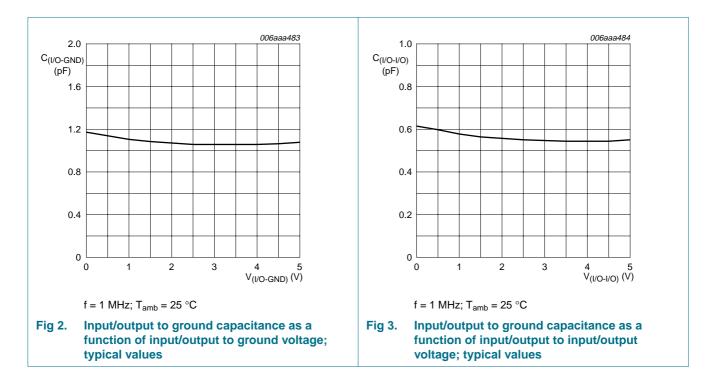
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per channe	əl					
I _R	reverse current	$V_R = 5 V$	<u>[1]</u> -	< 1	100	nA
C _(I/O-GND)	input/output to ground capacitance	f = 1 MHz; V _(I/O-GND) = 0 V	<u>[1]</u> -	1.0	1.5	pF
C _(I/O-I/O)	input/output to input/output capacitance	f = 1 MHz; V _(I/O-I/O) = 0 V	[2] _	0.6	-	pF
V _F	forward voltage	I _F = 1 mA	[3]	0.7	-	V
Zener diod	e					
V _{RWM}	reverse standoff voltage		[4]	-	5.5	V
V _{BR}	breakdown voltage		<mark>[4]</mark> 6	-	9	V
C _{sup}	supply pin to ground capacitance	f = 1 MHz; V _{CC} = 0 V	<u>[4]</u> _	16	-	pF

[1] Measured from pin 1, 3, 4 or 6 to ground.

[2] Measured from pin 1 or 6 to pin 3 or 4.

[3] Measured from pin 1, 3, 4 or 6 to pin 5.

[4] Measured from pin 5 to ground.

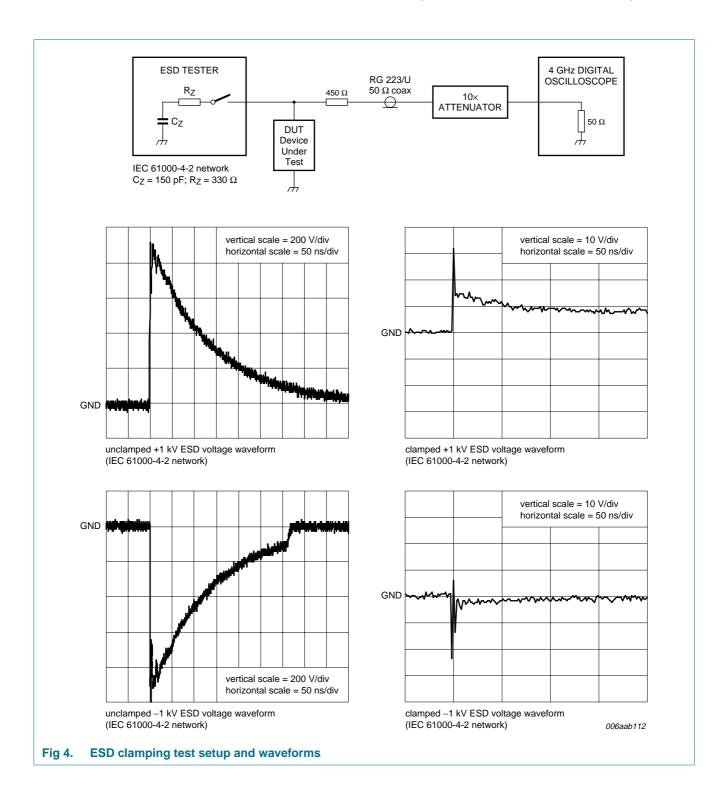


PRTR5V0U2F_PRTR5V0U2K_2

NXP Semiconductors

PRTR5V0U2F; PRTR5V0U2K

Ultra low capacitance double rail-to-rail ESD protection



PRTR5V0U2F_PRTR5V0U2K_2

Ultra low capacitance double rail-to-rail ESD protection

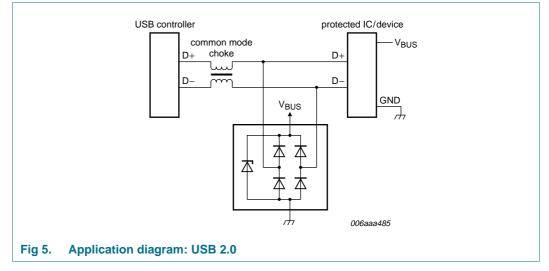
7. Application information

Handling data rates up to 480 Mbit/s, USB 2.0 interfaces require ESD protection devices with an extremely low line capacitance in order to avoid signal distortion.

With a capacitance of only 1 pF, the PRTR5V0U2F and the PRTR5V0U2K offer IEC 61000-4-2, level 4 compliant ESD protection.

PRTR5V0U2F and PRTR5V0U2K integrate two pairs of ultra low capacitance rail-to-rail ESD protection channels and one additional ESD protection diode each.

The additional ESD protection diode connected between ground and V_{CC} prevents charging of the supply.



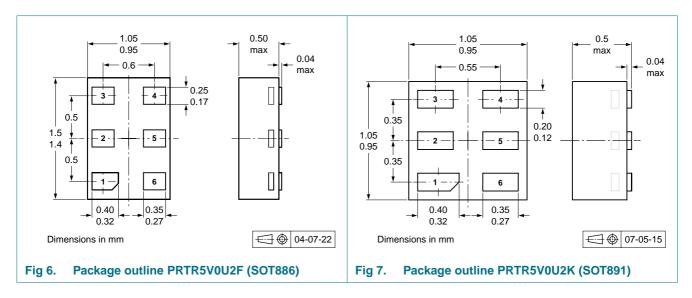
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the PRTR5V0U2F and the PRTR5V0U2K as close to the input terminal or connector as possible.
- 2. The path length between the PRTR5V0U2F or the PRTR5V0U2K and the protected line should be minimized.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Ultra low capacitance double rail-to-rail ESD protection

8. Package outline



9. Packing information

Table 10. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description		Packing quantity
				5000
PRTR5V0U2F	SOT886	4 mm pitch, 8 mm tape and reel; T1	[2]	-115
		4 mm pitch, 8 mm tape and reel; T4	[3]	-132
PRTR5V0U2K	SOT891	4 mm pitch, 8 mm tape and reel		-132

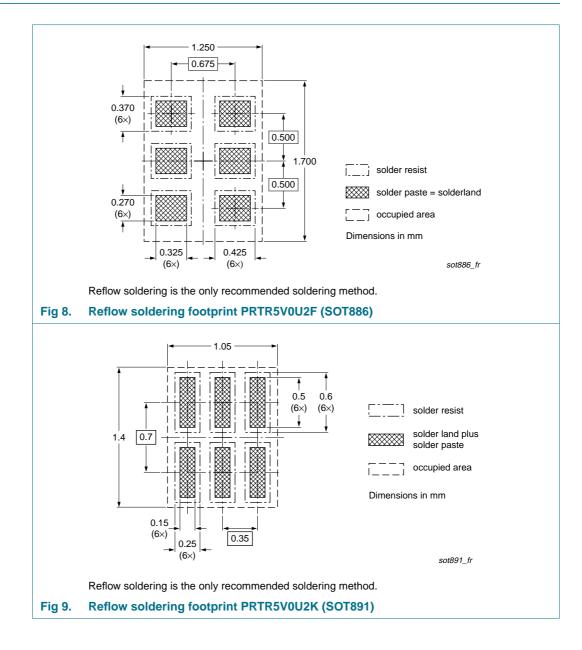
[1] For further information and the availability of packing methods, see Section 13.

[2] T1: normal taping

[3] T4: 90° rotated reverse taping

Ultra low capacitance double rail-to-rail ESD protection

10. Soldering



Ultra low capacitance double rail-to-rail ESD protection

11. Revision history

Table 11.Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PRTR5V0U2F_PRTR5V0U2K_2	20090219	Product data sheet	-	PRTR5V0U2F_PRTR5V0U2K_1
Modifications:	• Table 3 "Pi	nning": graphic symbo	ol amended	
PRTR5V0U2F_PRTR5V0U2K_1	20081106	Product data sheet	-	-

Ultra low capacitance double rail-to-rail ESD protection

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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PRTR5V0U2F_PRTR5V0U2K_2
Product data sheet

NXP Semiconductors

PRTR5V0U2F; PRTR5V0U2K

Ultra low capacitance double rail-to-rail ESD protection

14. Contents

1	Product profile 1
1.1	General description
1.2	Features
1.3	Applications 1
1.4	Quick reference data
2	Pinning information 2
3	Ordering information 3
4	Marking 3
5	Limiting values 3
6	Characteristics 5
7	Application information 7
8	Package outline 8
9	Packing information 8
10	Soldering
11	Revision history 10
12	Legal information 11
12.1	Data sheet status 11
12.2	Definitions 11
12.3	Disclaimers
12.4	Trademarks 11
13	Contact information 11
14	Contents 12

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Date of release: 19 February 2009 Document identifier: PRTR5V0U2F_PRTR5V0U2K_2



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