PSMN012-60YS

N-channel LFPAK 60 V, 11.1 mΩ standard level MOSFET

Rev. 01 — 5 January 2010 **Product data sheet**

1. Product profile

1.1 General description

Standard level N-channel MOSFET in LFPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Advanced TrenchMOS provides low RDSon and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LFPAK provides maximum power density in a Power SO8 package

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 175 °C	-	-	60	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 1	-	-	59	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	-	89	W
T_j	junction temperature		-55	-	175	°C
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 59 A; V_{sup} ≤ 60 V; R_{GS} = 50 Ω	-	-	71	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = 10 V; I_D = 30 A; V_{DS} = 30 V; see Figure 14 and 15	-	6.4	-	nC
$Q_{G(tot)}$	total gate charge		-	28.4	-	nC

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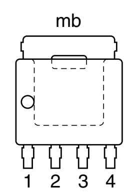
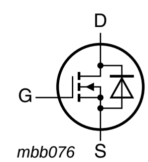
Table 1. Quick reference *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; T_j = 100 °C; see Figure 12	-	-	17.8	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 25 °C; see Figure 13	-	8	11.1	mΩ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 SOT669 (LFPAK)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

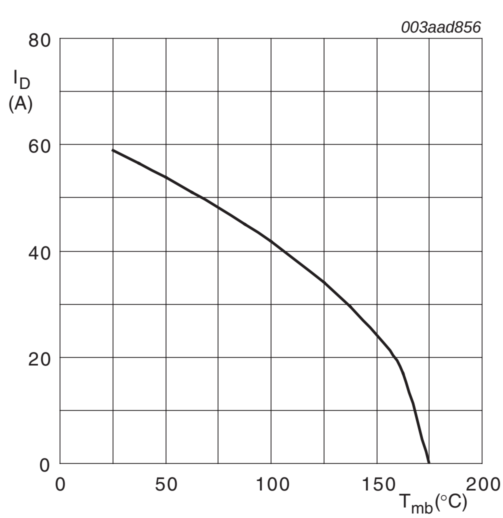
Type number	Package		
	Name	Description	Version
PSMN012-60YS	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

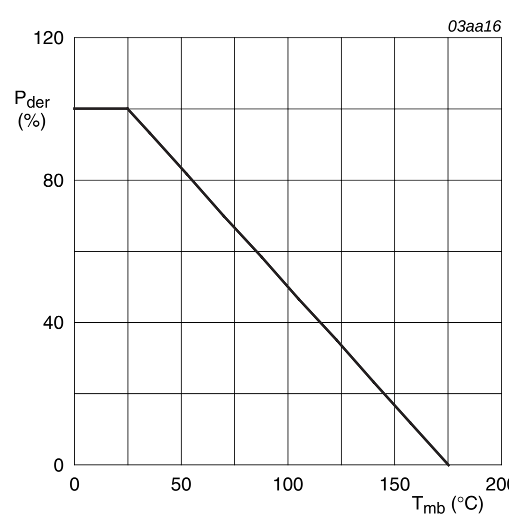
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	60	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C; $R_{GS} = 20$ kΩ	-	60	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 100$ °C; see Figure 1	-	42	A
		$V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1	-	59	A
I_{DM}	peak drain current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C; see Figure 3	-	236	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	89	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25$ °C	-	59	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C	-	236	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 59$ A; $V_{sup} \leq 60$ V; $R_{GS} = 50$ Ω	-	71	mJ



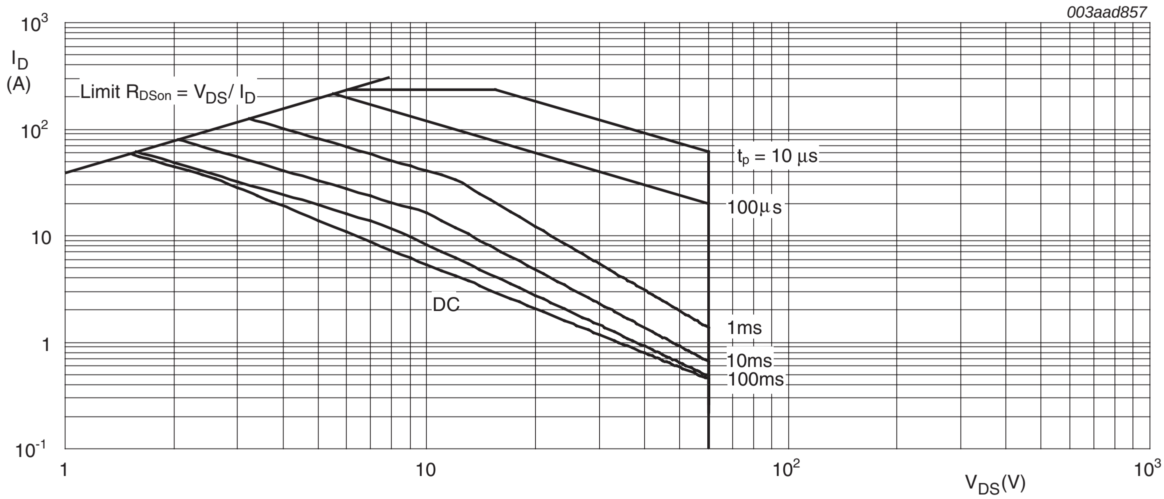
$$V_{GS} \geq 10 \text{ V}$$

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25$ °C; I_{DM} is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.8	1.68	K/W

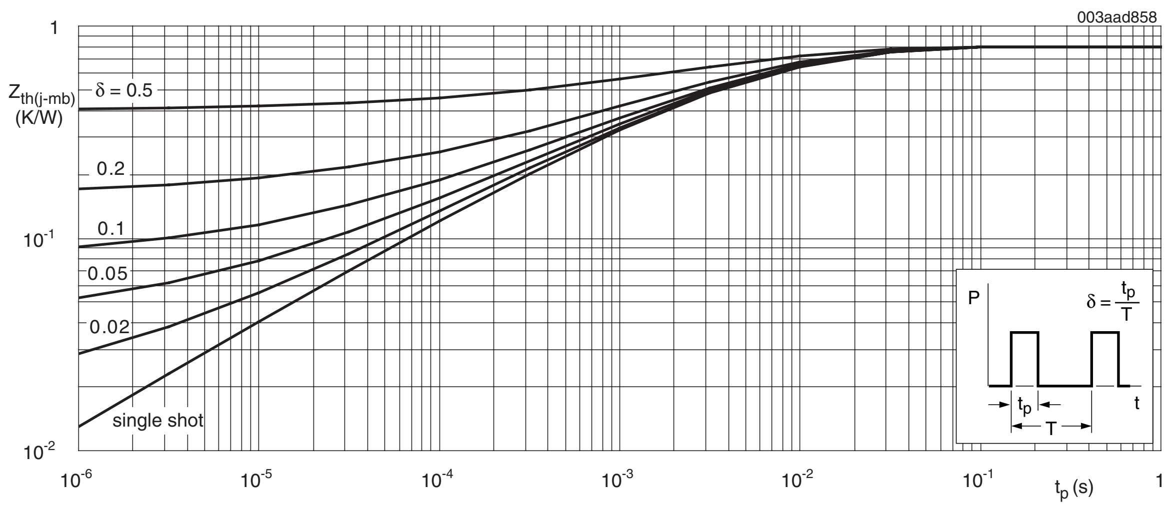


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

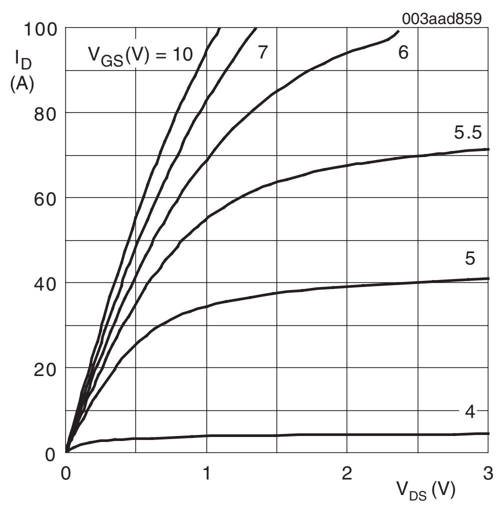
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	54	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}= V_{GS}; T_j = 25 °C; see Figure 10 and 11	2	3	4	V
V_{GSth}		I_D = 1 mA; V_{DS}= V_{GS}; T_j = -55 °C; see Figure 11	-	-	4.6	V
		I_D = 1 mA; V_{DS}= V_{GS}; T_j = 175 °C; see Figure 11	0.95	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	0.03	2	µA
		V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	-	50	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; T_j = 175 °C; see Figure 12	-	17	25.5	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 100 °C; see Figure 12	-	-	17.8	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 25 °C; see Figure 13	-	8	11.1	mΩ
R_G	gate resistance	f = 1 MHz	-	0.66	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 30 A; V_{DS} = 30 V; V_{GS} = 10 V; see Figure 14 and 15	-	28.4	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V	-	23.3	-	nC
Q_{GS}	gate-source charge	I_D = 30 A; V_{DS} = 30 V; V_{GS} = 10 V; see Figure 14 and 15	-	8.75	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	I_D = 30 A; V_{DS} = 30 V; V_{GS} = 10 V; see Figure 14	-	4.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3.9	-	nC
Q_{GD}	gate-drain charge	I_D = 30 A; V_{DS} = 30 V; V_{GS} = 10 V; see Figure 14 and 15	-	6.4	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	V_{DS} = 30 V; see Figure 14 and 15	-	4.8	-	V
C_{iss}	input capacitance	V_{DS} = 30 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 16	-	1685	-	pF
C_{oss}	output capacitance		-	245	-	pF
C_{rss}	reverse transfer capacitance		-	140	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 4.7 Ω	-	15.2	-	ns
t_r	rise time		-	12.6	-	ns
$t_{d(off)}$	turn-off delay time		-	28.7	-	ns
t_f	fall time		-	8.2	-	ns

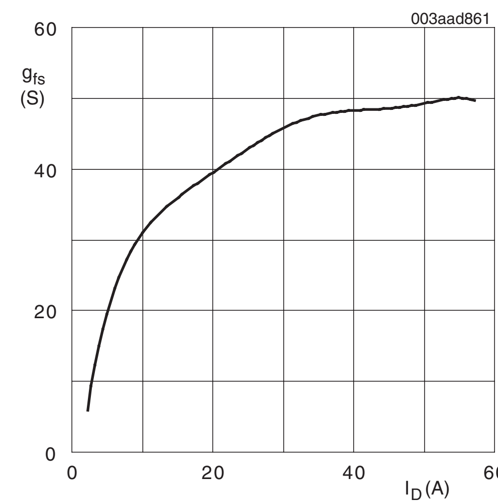
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 15 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 17	-	0.82	1.2	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V	-	35	-	ns
Q_r	recovered charge		-	41	-	nC



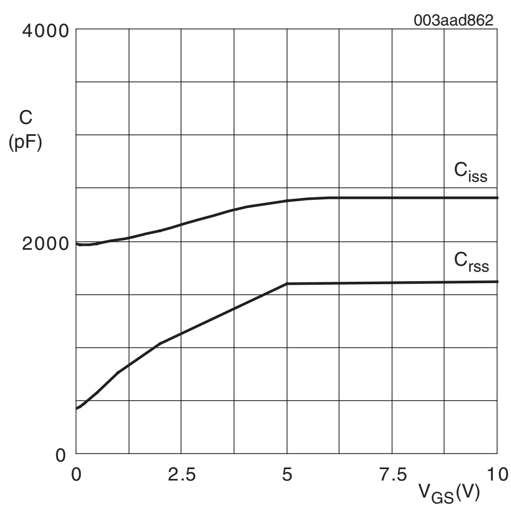
$T_j = 25\,°C$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



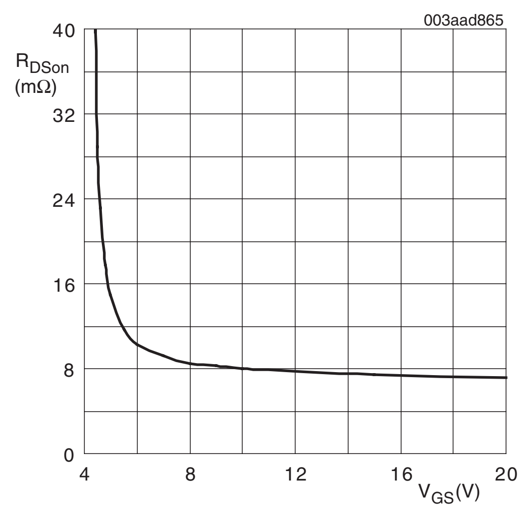
$T_j = 25$ °C; $V_{DS} = 15$ V

Fig 6. Forward transconductance as a function of drain current; typical values



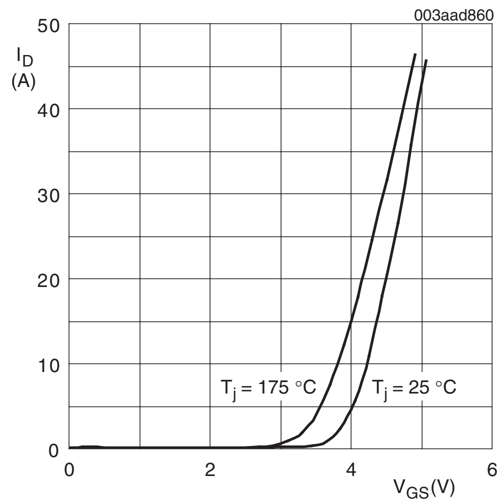
$V_{DS} = 0$ V; f = 1 MHz

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage, typical values



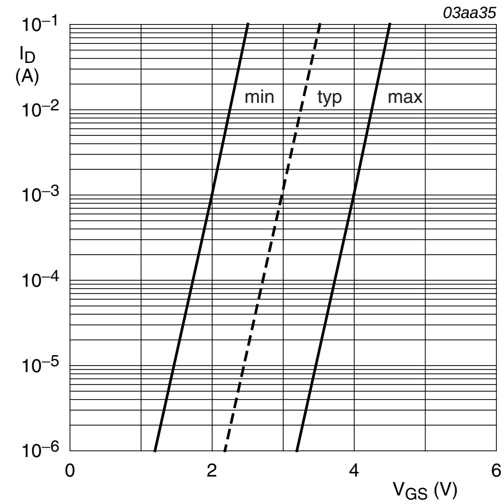
$T_j = 25$ °C; $I_D = 10$ A

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



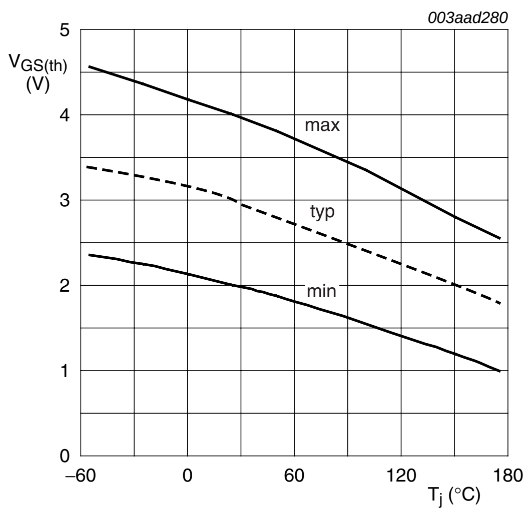
$V_{DS} > I_D \times R_{DSon}$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



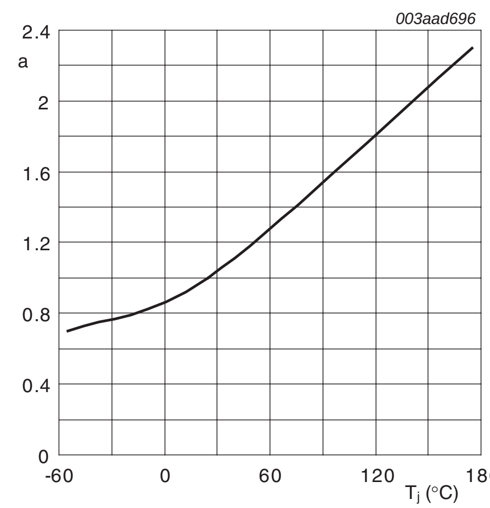
$T_j = 25\,°C; V_{DS} = 5V$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



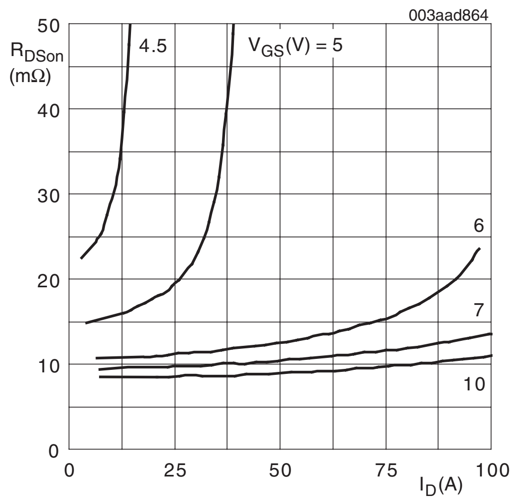
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature.



$T_j = 25\,°C$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

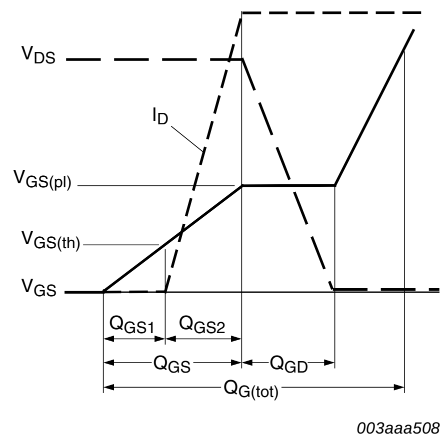
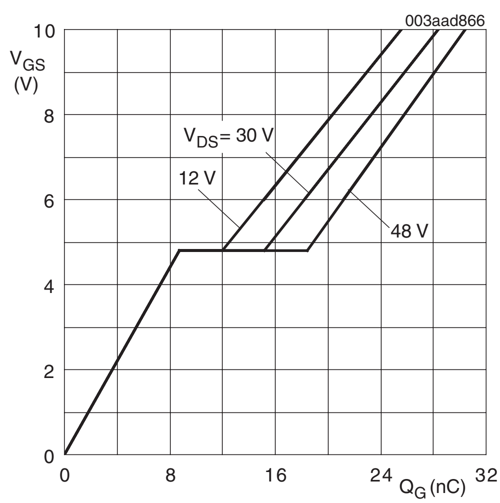
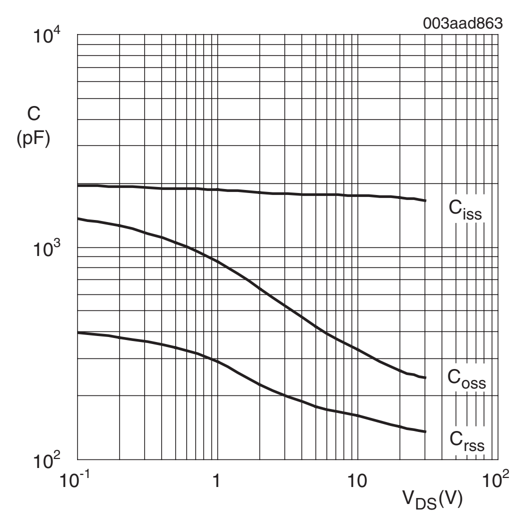


Fig 14. Gate charge waveform definitions



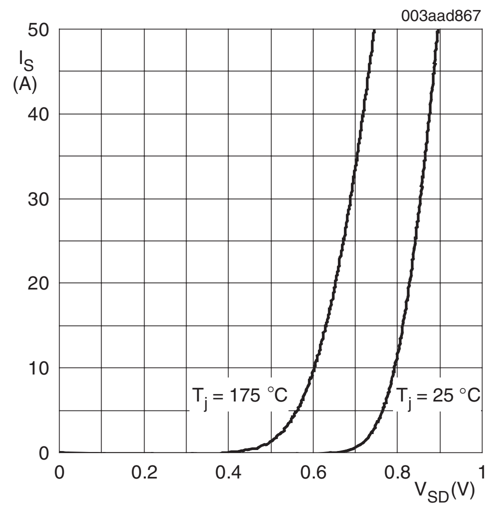
$T_j = 25\,°C; I_D = 30\,A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\,V$; f = 1 MHz

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

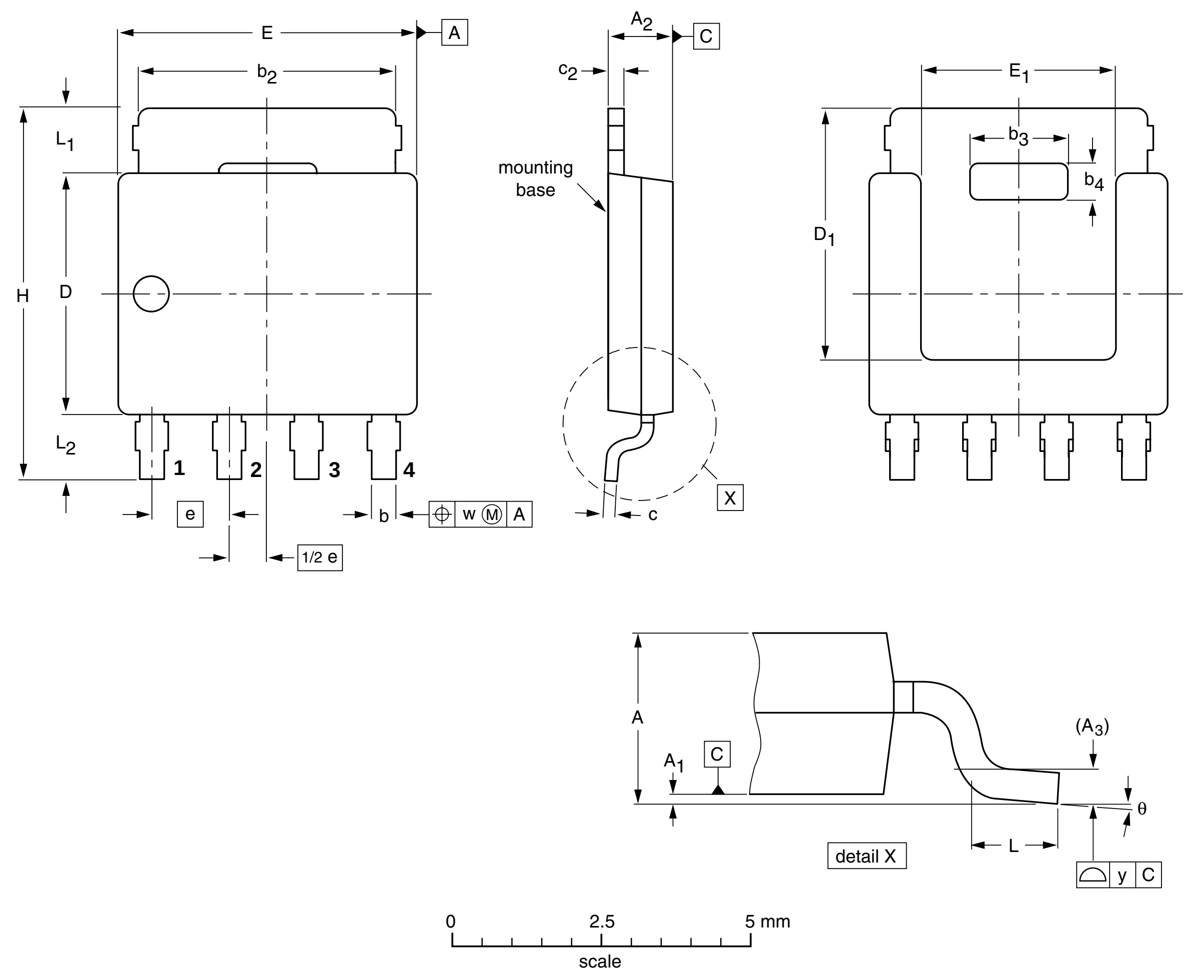


$V_{GS} = 0V$

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1) max	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~04-10-13~~ 06-03-16

Fig 18. Package outline SOT669 (LFPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN012-60YS_1	20100105	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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11. Contents

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