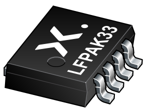

PSMN013-30MLC

N-channel 30 V 13.6 mΩ logic level MOSFET in LFPAK33 using NextPower Technology

23 February 2018 Product data sheet

1. General description

Logic level enhancement mode N-channel MOSFET in LFPAK33 package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

3. Applications

- DC-to-DC converters
- Load switching
- Synchronous buck regulator

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	30	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	39	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	38	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 10 A; T_j = 25 °C; Fig. 10		-	14.65	16.9	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; Fig. 10		-	11.8	13.6	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 10 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	1	-	nC
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 15 V; V_{GS} = 10 V; Fig. 12; Fig. 13		-	8	-	nC

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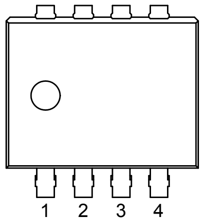
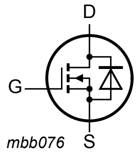
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK33 (SOT1210)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN013-30MLC	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 8 leads	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN013-30MLC	M13C30

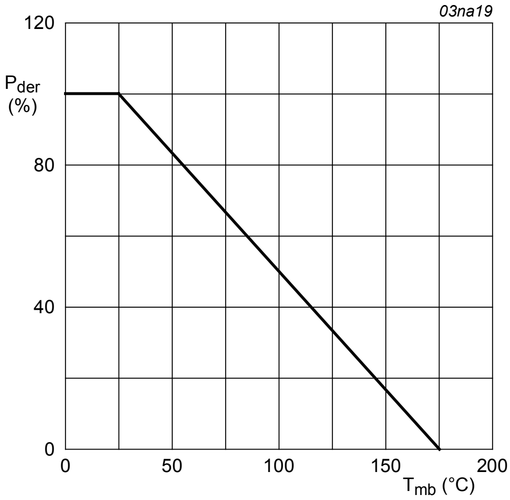
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

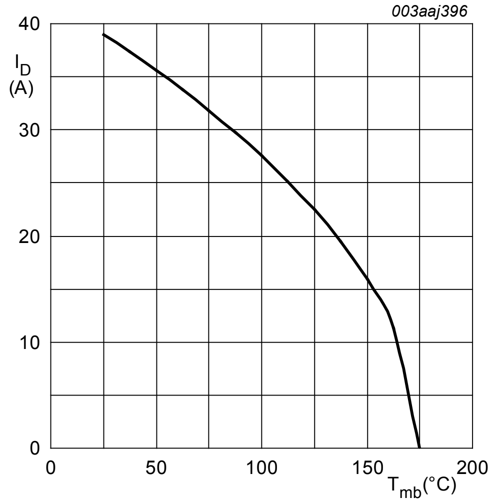
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	30	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	38	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	39	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	28	A
I_{DM}	peak drain current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C; Fig. 3		-	157	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	MM (JEDEC)		100	-	V
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	34	A
I_{SM}	peak source current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C		-	157	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 39 A; $V_{sup} \leq$ 30 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4		-	5.6	mJ



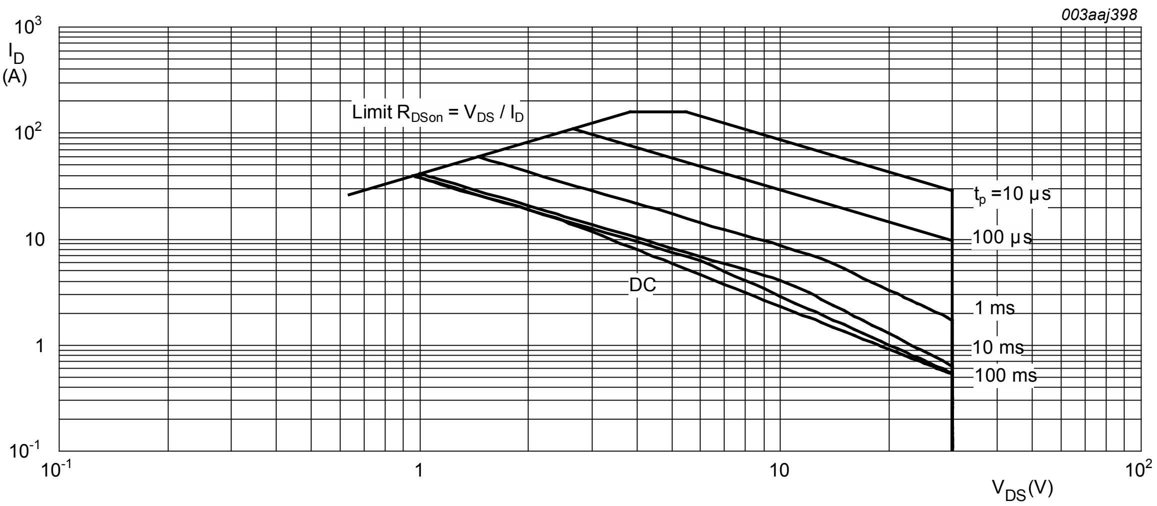
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



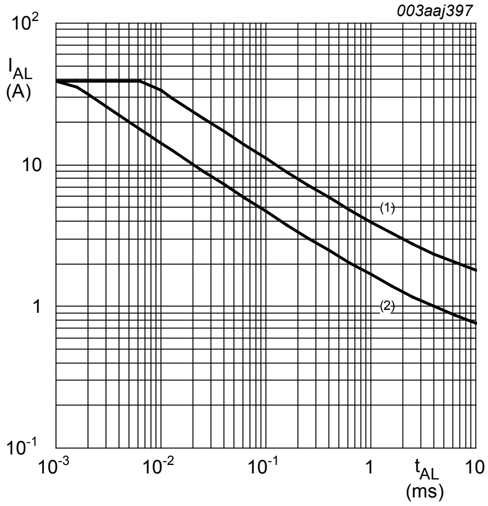
$V_{GS} \geq 10V$

Fig. 2. Continuous drain current as a function of mounting base temperature



$T_{mb} = 25°C$; I_{DM} *is a single pulse*

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\ (init)} = 25°C$; (2) $T_{j\ (init)} = 100°C$

Fig. 4. **Single pulse avalanche rating; avalanche current as a function of avalanche time**

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	3.8	3.99	K/W

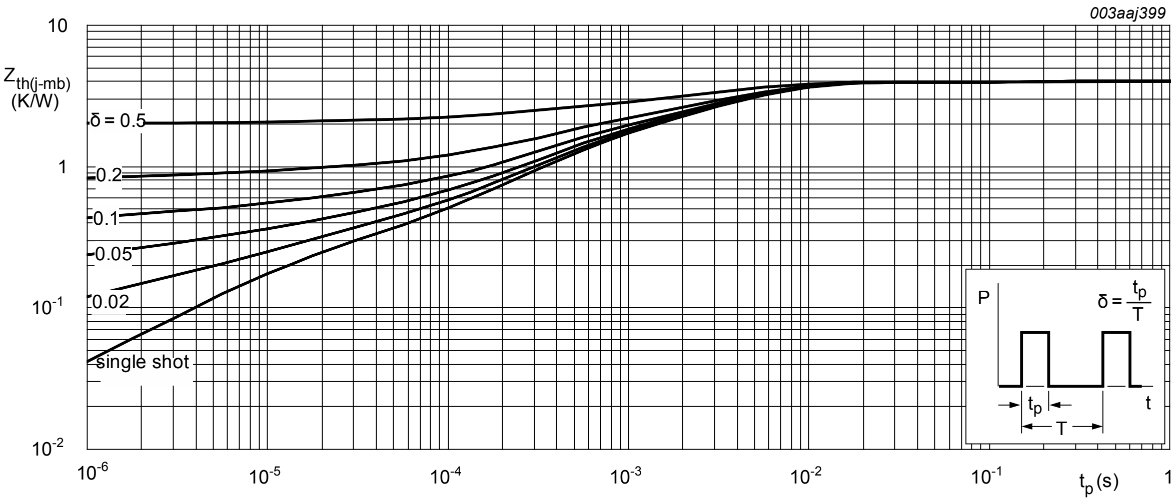


Fig. 5. **Transient thermal impedance from junction to mounting base as a function of pulse duration**

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		30	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		1.3	1.66	1.95	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature			-	-4	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 °C		-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 10 A; T_j = 25 °C; Fig. 10		-	14.65	16.9	mΩ
		V_{GS} = 4.5 V; I_D = 10 A; T_j = 150 °C; Fig. 10; Fig. 11		-	-	28.75	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; Fig. 10		-	11.8	13.6	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 150 °C; Fig. 10; Fig. 11		-	-	22.95	mΩ
R_G	gate resistance	f = 1 MHz		0.85	1.7	3.4	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 15 V; V_{GS} = 10 V; Fig. 12; Fig. 13		-	8	-	nC
		I_D = 10 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	3.7	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	7.4	-	nC
Q_{GS}	gate-source charge	I_D = 10 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	1.2	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	0.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	0.4	-	nC
Q_{GD}	gate-drain charge			-	1	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 10 A; V_{DS} = 15 V; Fig. 12; Fig. 13		-	2.6	-	V
C_{iss}	input capacitance	V_{DS} = 15 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 14		-	519	-	pF
C_{oss}	output capacitance			-	131	-	pF
C_{rss}	reverse transfer capacitance			-	37	-	pF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 1.5 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5 Ω		-	7	-	ns
t_r	rise time			-	9.8	-	ns
$t_{d(off)}$	turn-off delay time			-	9.6	-	ns
t_f	fall time			-	5.5	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 15 V; f = 1 MHz; T_j = 25 °C		-	3.7	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 10 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15		-	0.86	1.1	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 15 V		-	13.4	-	ns
Q_r	recovered charge			-	6.6	-	nC
t_a	reverse recovery rise time	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 15 V; Fig. 16		-	8.6	-	ns
t_b	reverse recovery fall time			-	4.8	-	ns

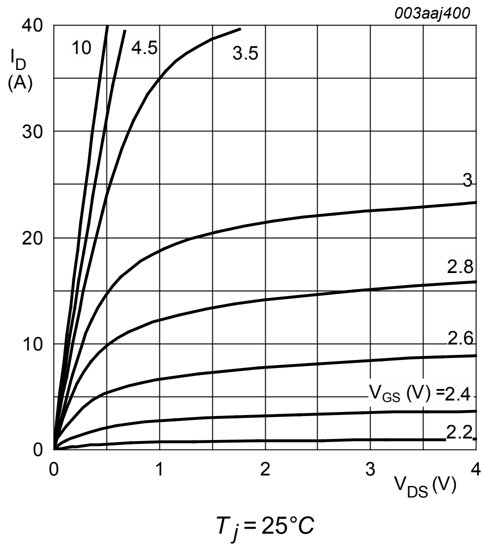


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

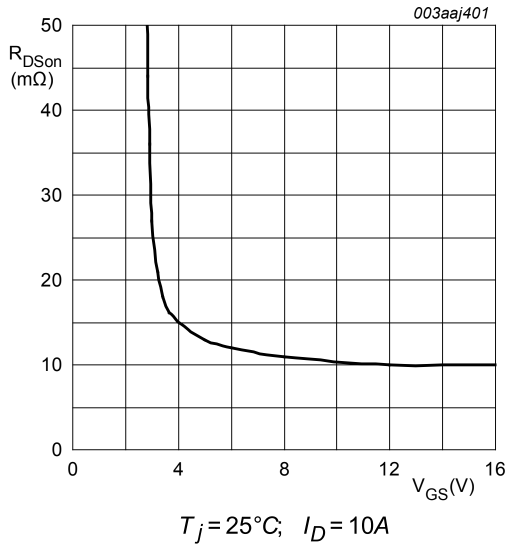
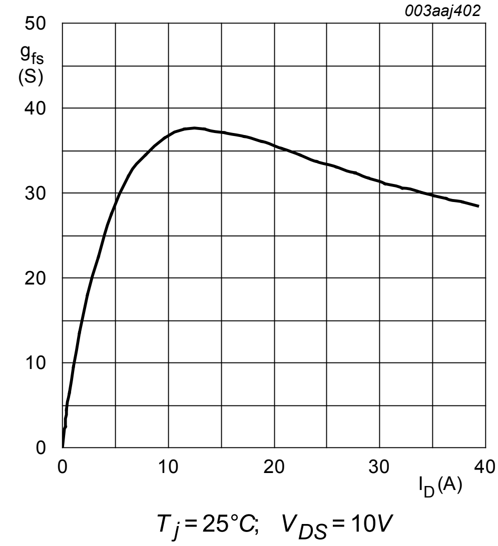
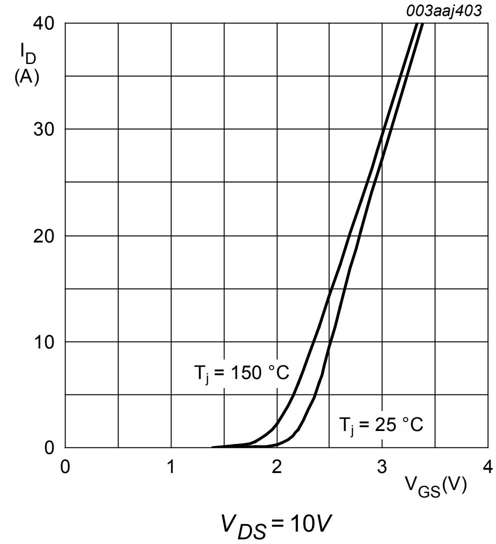


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



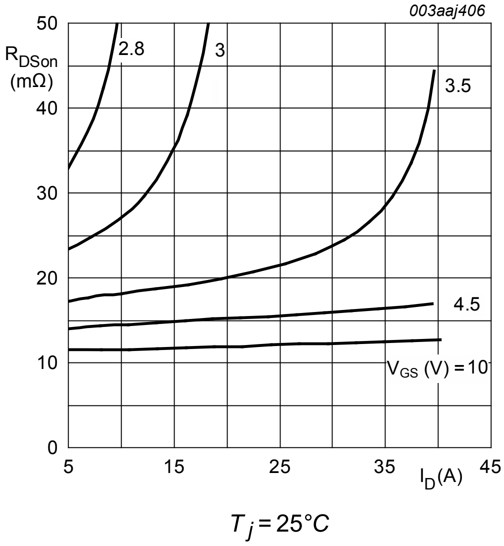
$T_j = 25°C$; $V_{DS} = 10V$

Fig. 8. Forward transconductance as a function of drain current; typical values



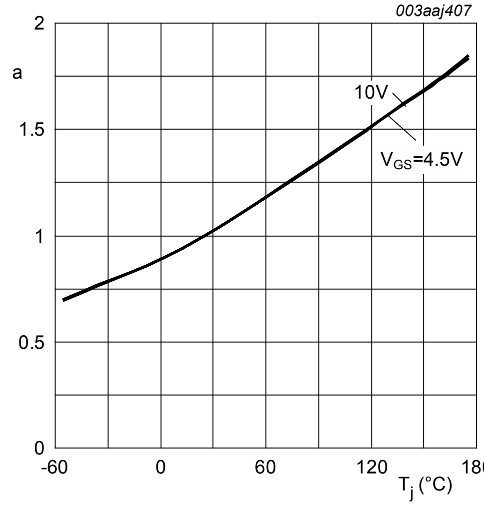
$V_{DS} = 10V$

Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



$T_j = 25°C$

Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}\,(25°C)}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

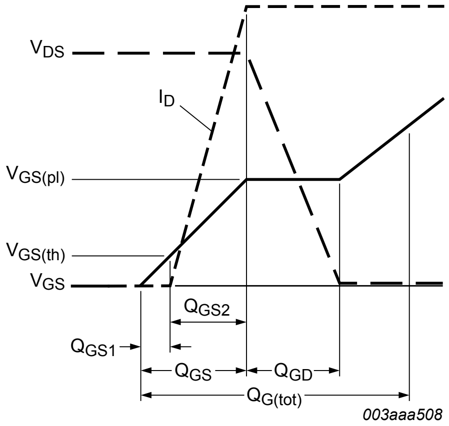


Fig. 12. Gate charge waveform definitions

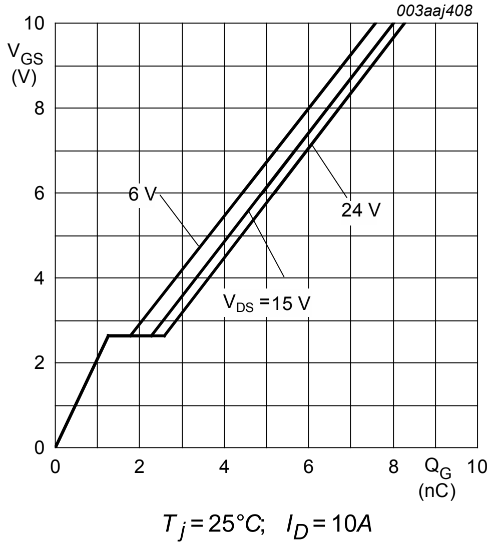


Fig. 13. Gate-source voltage as a function of gate charge; typical values

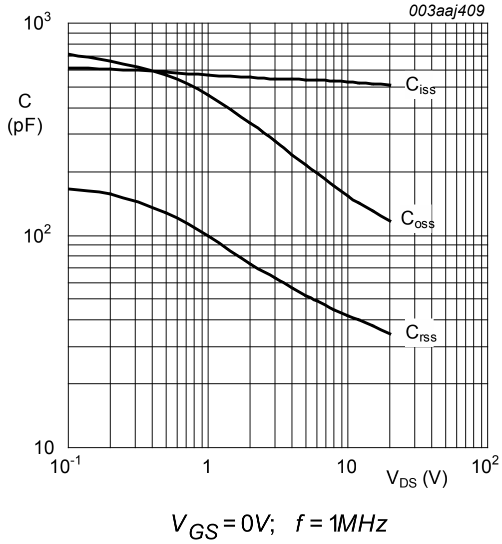


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

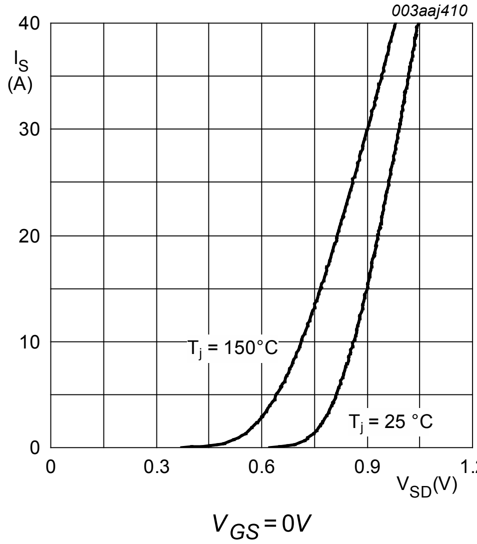


Fig. 15. Source current as a function of source-drain voltage; typical values

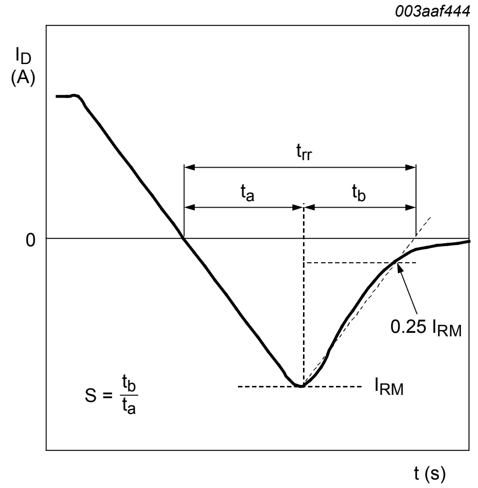
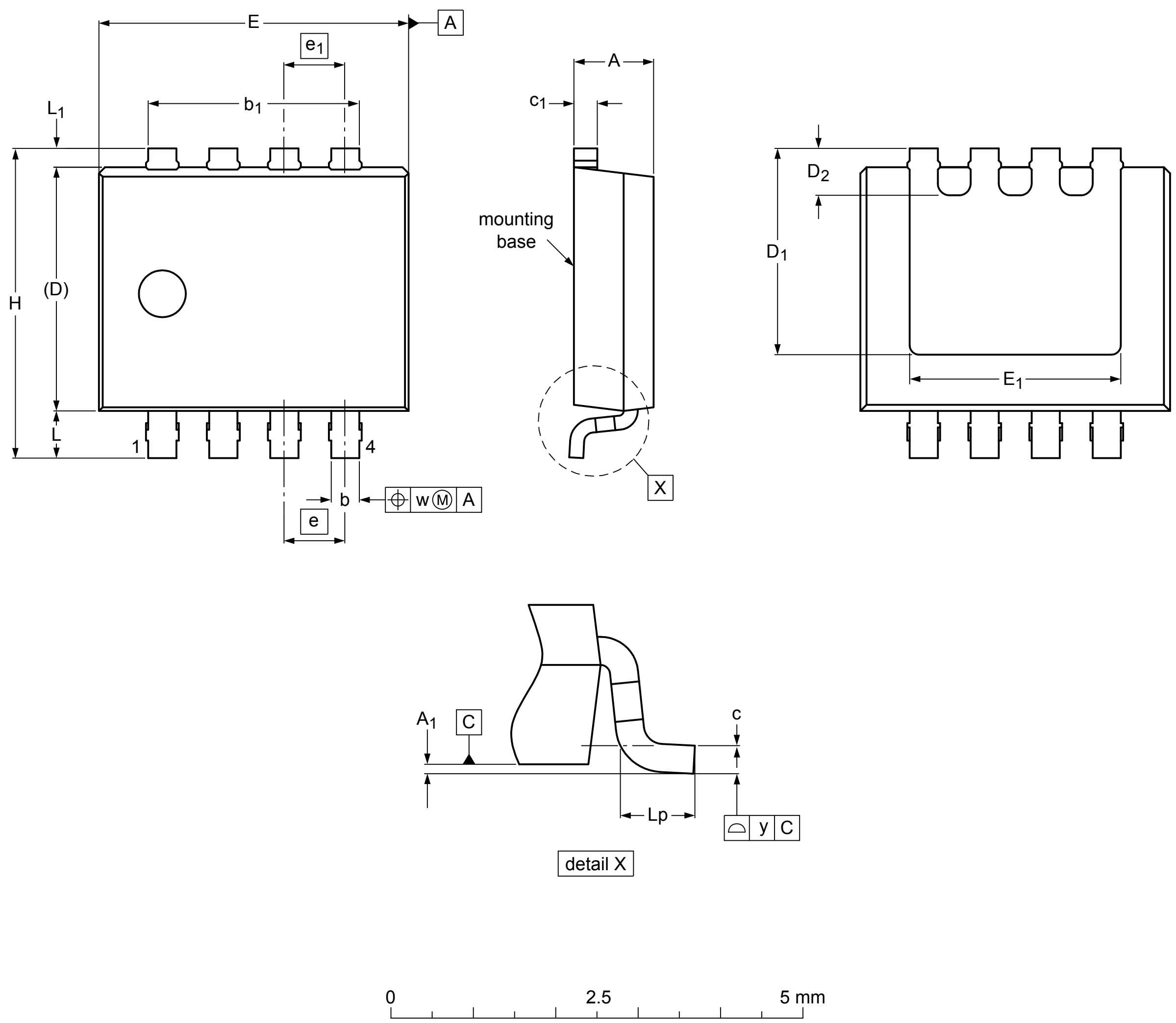


Fig. 16. Reverse recovery timing definition

11. Package outline

Plastic single ended surface mounted package (LFPAK33); 8 leads **SOT1210**



Dimensions

Unit[(1)]		A	A_1	b[(1)]	b_1[(1)]	c	c_1	D ref	D_1	D_2	E[(1)]	E_1	e	e_1	H	L	L_1	L_p	w	y
mm	max	0.90	0.10	0.35	2.4	0.20	0.30		2.35		3.40	2.45			3.40	0.65	0.25	0.50		
	nom							2.60		0.50			0.65	0.65					0.20	0.10
	min	0.80	0.00	0.25	2.2	0.10	0.20		1.90		3.20	2.00			3.20	0.45	0.13	0.30		

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1210_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1210						~~14-04-25~~ 16-08-09

Fig. 17. Package outline LFPAK33 (SOT1210)

12. Soldering

Footprint information for reflow soldering of LFPAK33 package **SOT1210**

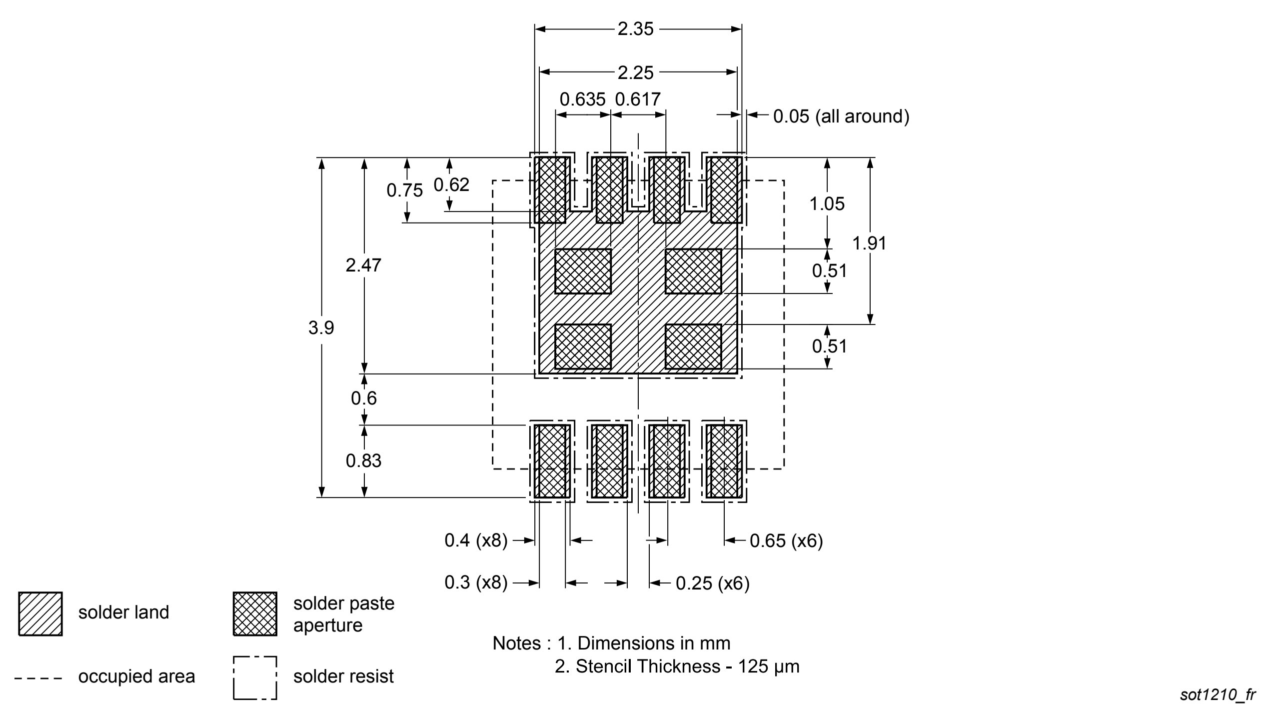


Fig. 18. Reflow soldering footprint for LFPAK33 (SOT1210)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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