



PSMN102-200Y

N-channel TrenchMOS SiliconMAX standard level FET

Rev. 03 — 16 March 2011

Product data sheet

1. Product profile

1.1 General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Higher operating power due to low thermal resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- Class D amplifier
- DC-to-DC converters
- Motion control
- Switched-mode power supplies

1.4 Quick reference data

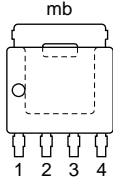
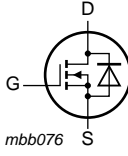
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	200	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; see Figure 3	-	-	21.5	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	113	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 12\text{ A}$; $T_j = 25\text{ °C}$; see Figure 9 ; see Figure 10	-	86	102	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 12\text{ A}$; $V_{DS} = 100\text{ V}$; see Figure 11 ; see Figure 12	-	10.1	-	nC

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2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT669 (LFAK)

3. Ordering information

Table 3. Ordering information

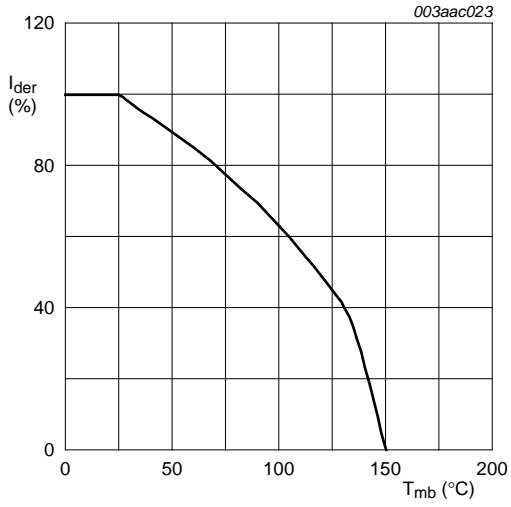
Type number	Package		Version
	Name	Description	
PSMN102-200Y	LFAK	plastic single-ended surface-mounted package (LFAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

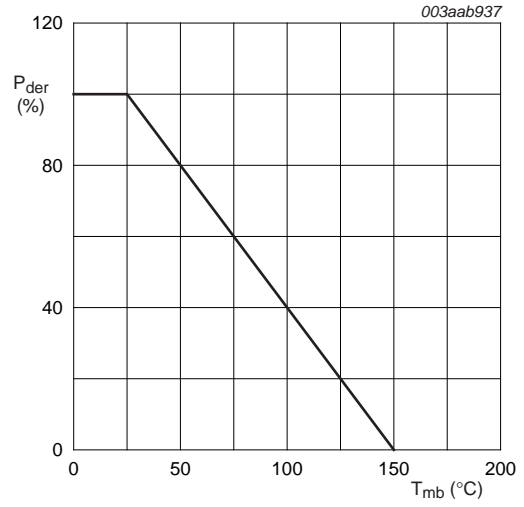
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	200	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	200	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3	-	21.5	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	13.6	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3	-	65	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	113	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	208	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 10.8\text{ A}$; $V_{sup} \leq 200\text{ V}$; unclamped; $t_p = 0.14\text{ ms}$; $R_{GS} = 50\text{ }\Omega$	-	202	mJ



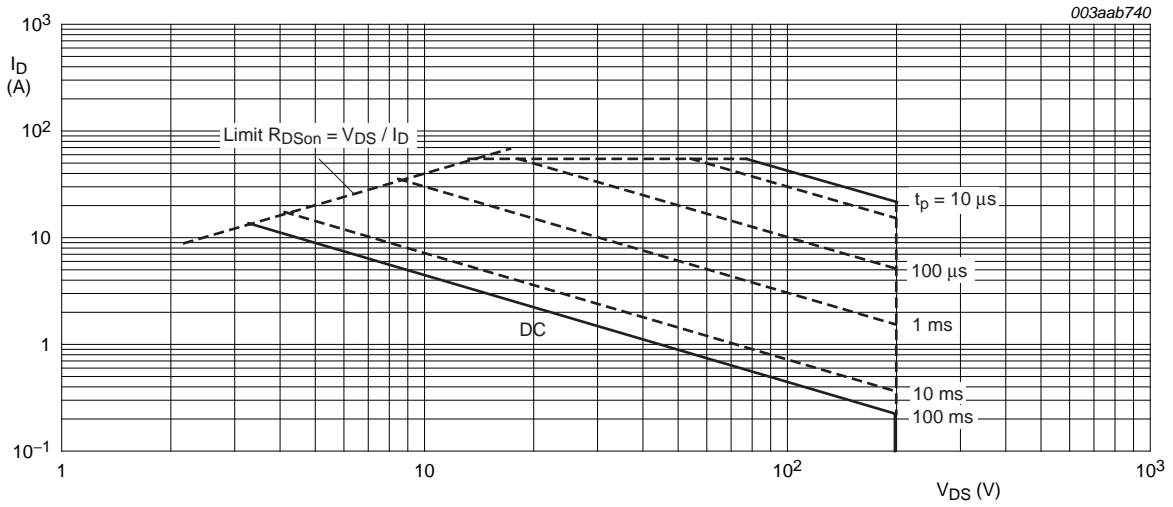
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig. 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig. 2. Normalized total power dissipation as a function of solder point temperature



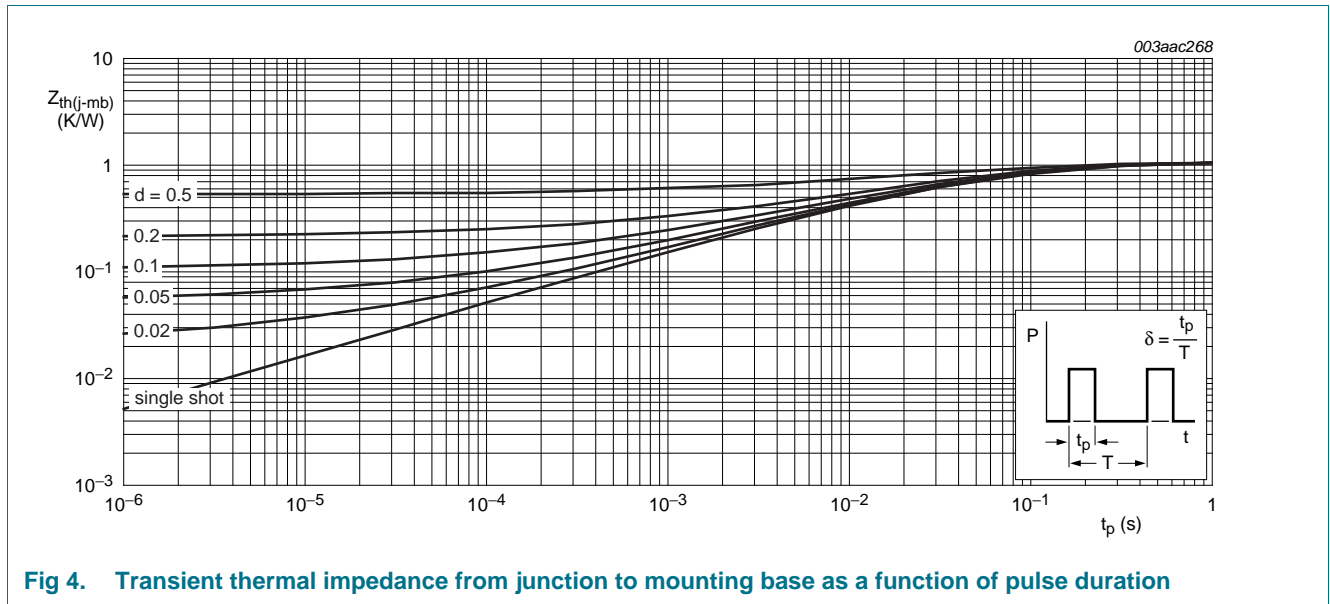
$T_{mb} = 25^\circ\text{C}; I_{DM}$ is single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Mounted on a printed-circuit board; vertical in still air; see Figure 4	-	-	1.1	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	200	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	178	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 7 ; see Figure 8	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 7 ; see Figure 8	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 7 ; see Figure 8	-	-	4.4	V
I_{DSS}	drain leakage current	$V_{DS} = 160 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 160 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 20 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 20 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 12 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 9 ; see Figure 10	-	86	102	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 12 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 9 ; see Figure 10	-	206	245	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}$	-	1.1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 12 \text{ A}; V_{DS} = 100 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 11 ; see Figure 12	-	30.7	-	nC
Q_{GS}	gate-source charge		-	6.3	-	nC
Q_{GD}	gate-drain charge		-	10.1	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 12 \text{ A}; V_{DS} = 100 \text{ V};$ see Figure 11 ; see Figure 12	-	4.6	-	V
C_{iss}	input capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 13	-	1568	-	pF
C_{oss}	output capacitance		-	170	-	pF
C_{rSS}	reverse transfer capacitance		-	55	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 100 \text{ V}; R_L = 5.8 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 5.6 \text{ } \Omega$	-	14.2	-	ns
t_r	rise time		-	29.5	-	ns
$t_{d(off)}$	turn-off delay time		-	33	-	ns
t_f	fall time		-	28	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 12 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 14	-	0.9	1.2	V
t_{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 30 \text{ V}$	-	143	-	ns
Q_r	recovered charge	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}$	-	268	-	nC

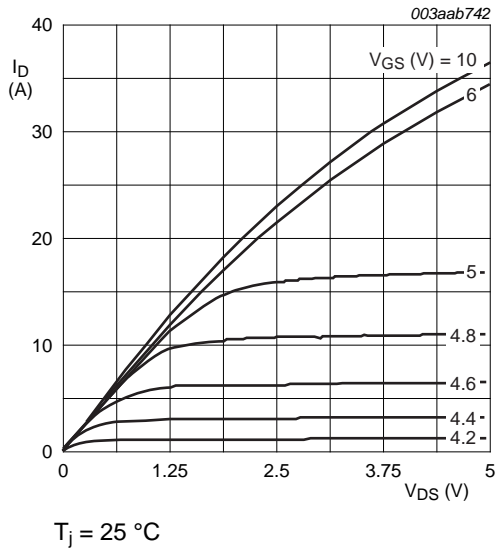


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

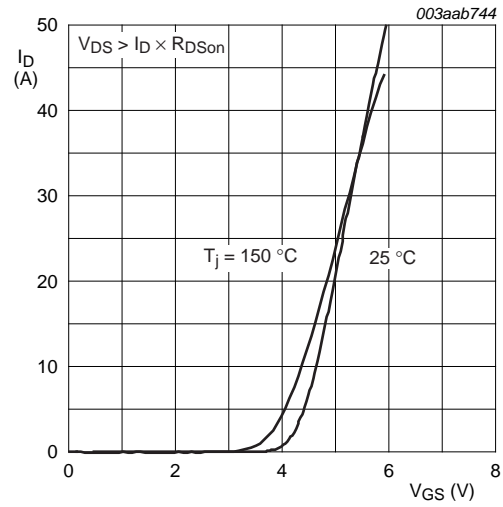


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

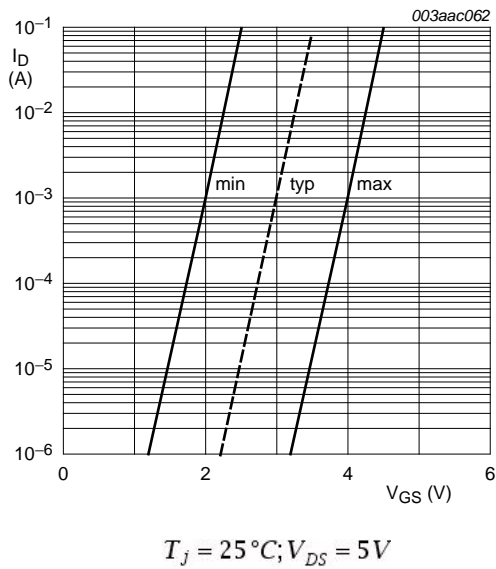


Fig 7. Sub-threshold drain current as a function of gate-source voltage

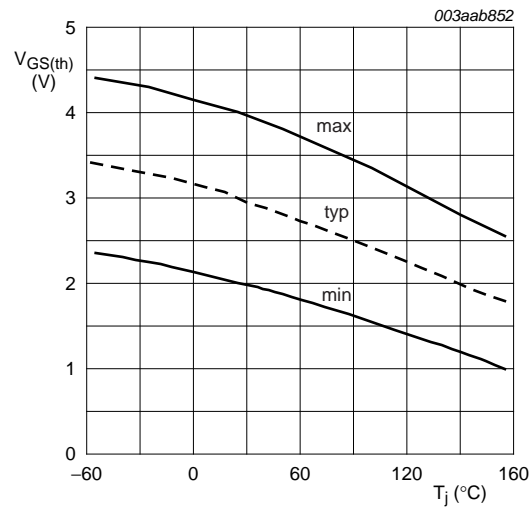
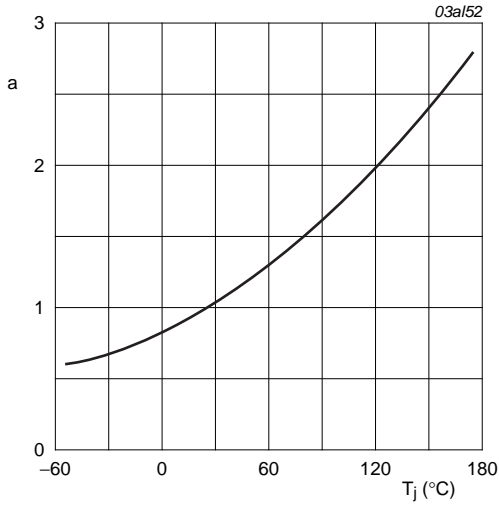
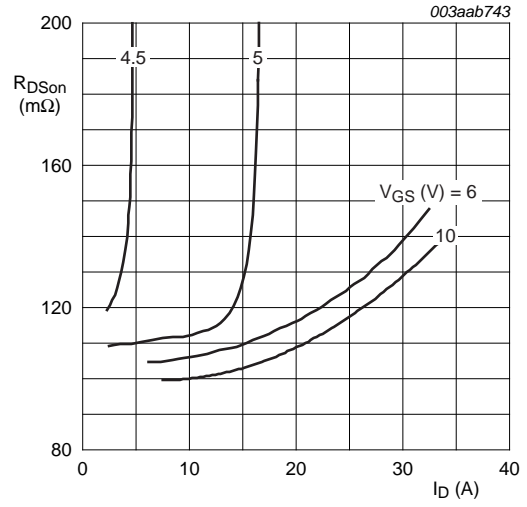


Fig 8. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^{\circ}C$

Fig 10. Drain-source on-state resistance as a function of drain current; typical values

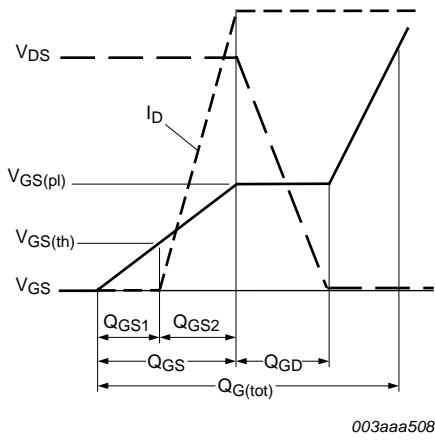
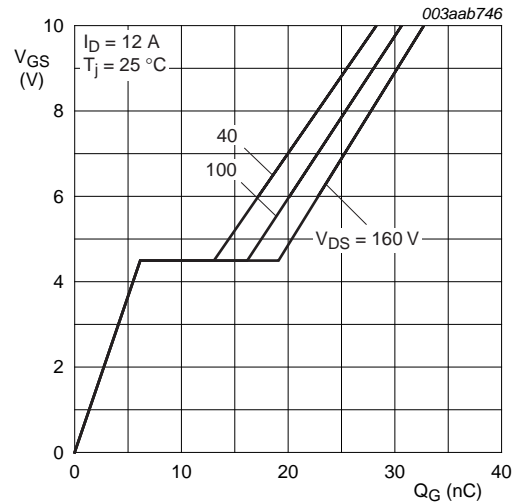
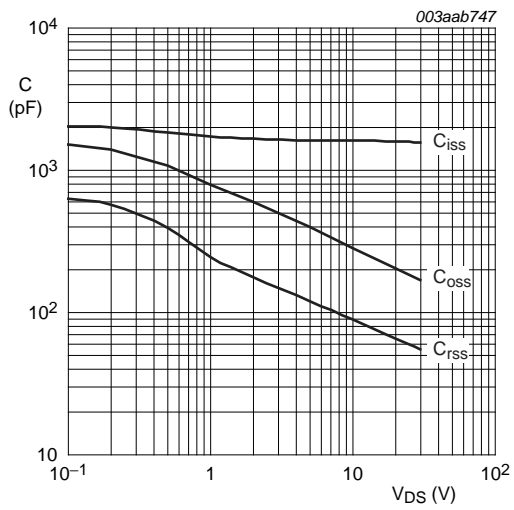


Fig 11. Gate charge waveform definitions



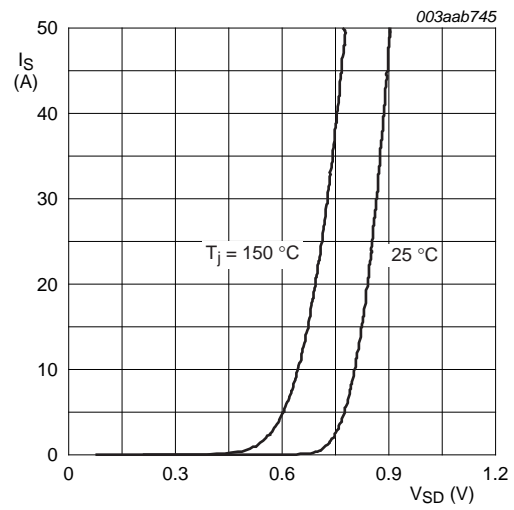
$I_D = 12 A; V_{DS} = 40, 100, \text{ and } 160 V$

Fig 12. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^\circ C \text{ and } 150^\circ C; V_{GS} = 0V$

Fig 14. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads

SOT669

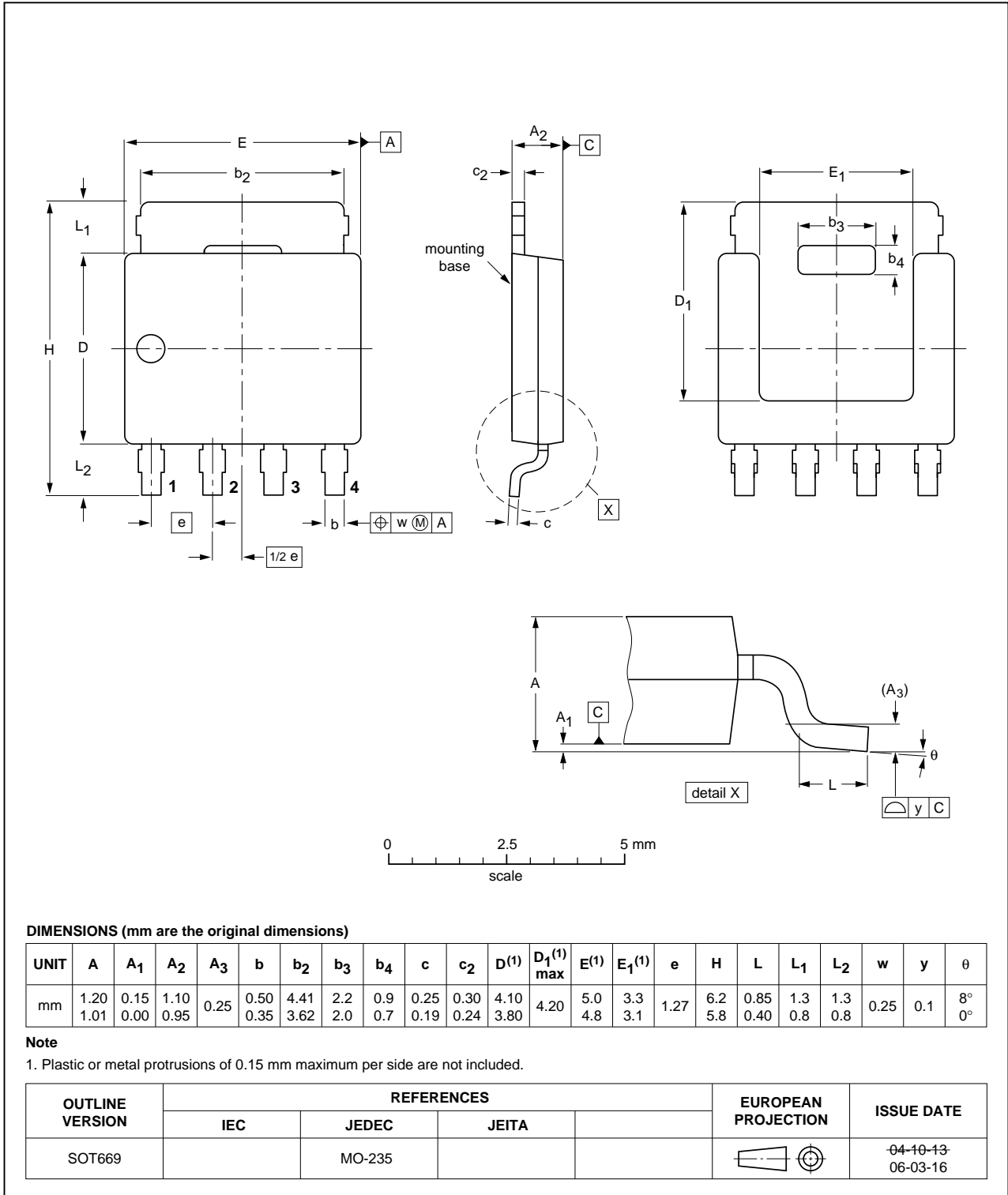


Fig 15. Package outline SOT669 (LFPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN102-200Y v.3	20110316	Product data sheet	-	PSMN102-200Y v.2
Modifications:	• Various changes to content.			
PSMN102-200Y v.2	20101220	Product data sheet	-	PSMN102-200Y v.1

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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