



PSMN1R2-30YLD

N-channel 30 V, 1.2 m Ω , 250 A logic level MOSFET in LPAK56 using NextPowerS3 Technology

21 December 2018

Product data sheet

1. General description

250 A logic level gate drive N-channel enhancement mode MOSFET in LPAK56 package. NextPowerS3 portfolio utilising Nexperia's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

2. Features and benefits

- 250 A capability
- Ultra low Q_G , Q_{GD} and Q_{OSS} for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery; s-factor > 1
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with < 1 μ A leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Wave solderable; exposed leads for optimal visual solder inspection

3. Applications

- On-board DC-to-DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control
- Power OR-ing

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C \leq T_j \leq 175 °C	-	-	30	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 25$ °C; Fig. 2	[1]	-	250	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Fig. 1	-	-	194	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 25$ A; $T_j = 25$ °C; Fig. 10	-	1.2	1.6	m Ω

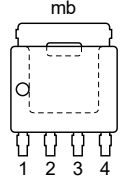
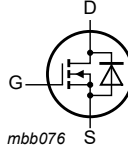
N-channel 30 V, 1.2 mΩ, 250 A logic level MOSFET in LFPAK56 using NextPowerS3 Technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	0.96	1.24	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 15\text{ V}$; $V_{GS} = 4.5\text{ V}$; Fig. 12 ; Fig. 13	-	9.1	-	nC
$Q_{G(tot)}$	total gate charge		-	32	-	nC
Source-drain diode						
S	softness factor	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 15\text{ V}$; Fig. 16	-	0.95	-	

[1] 250A continuous current has been successfully demonstrated during application test. Practically, the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFPAK56; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R2-30YLD	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R2-30YLD	1D230L

8. Limiting values

Table 5. Limiting values

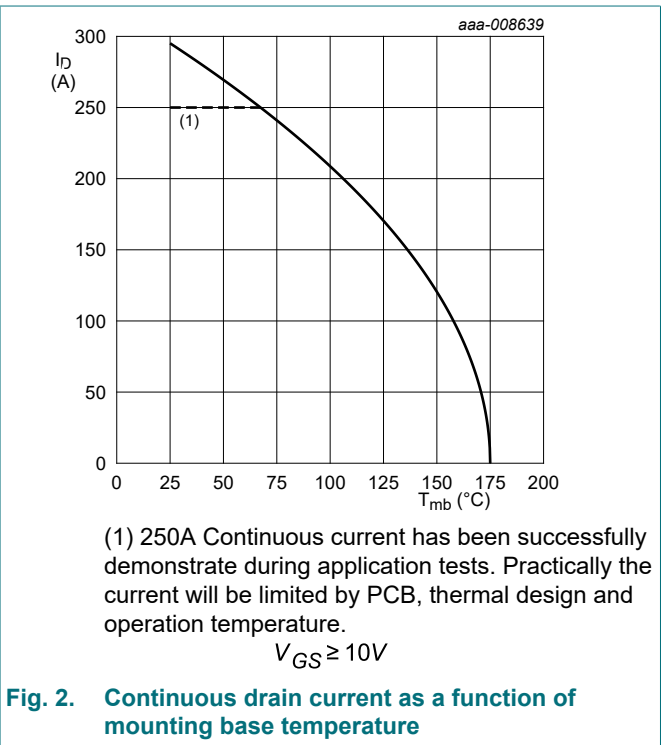
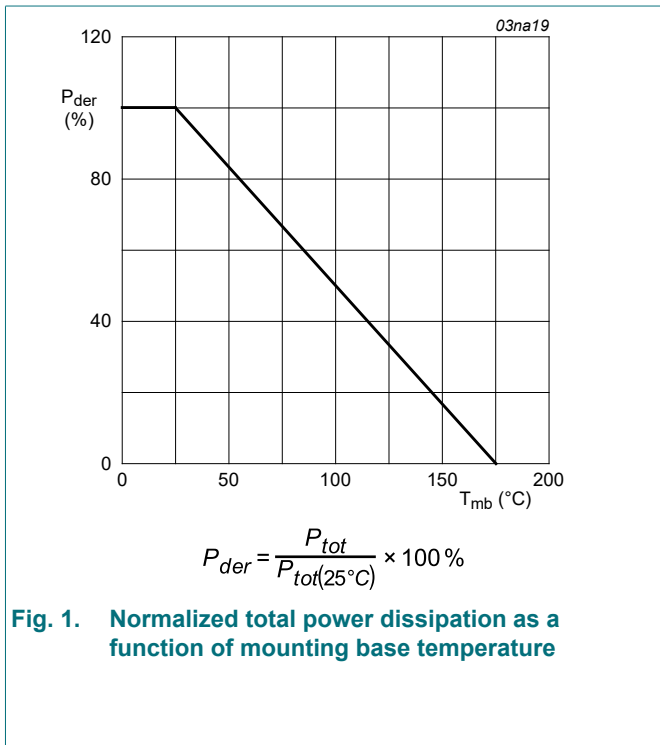
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	194	W

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Symbol	Parameter	Conditions		Min	Max	Unit
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	250	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	209	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	1181	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{slid(M)}	peak soldering temperature			-	260	°C
V _{ESD}	electrostatic discharge voltage	HBM		1500	-	V
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	162	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1181	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 25 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 1.97 ms	[2]	-	961	mJ

- [1] 250A continuous current has been successfully demonstrated during application test. Practically, the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test



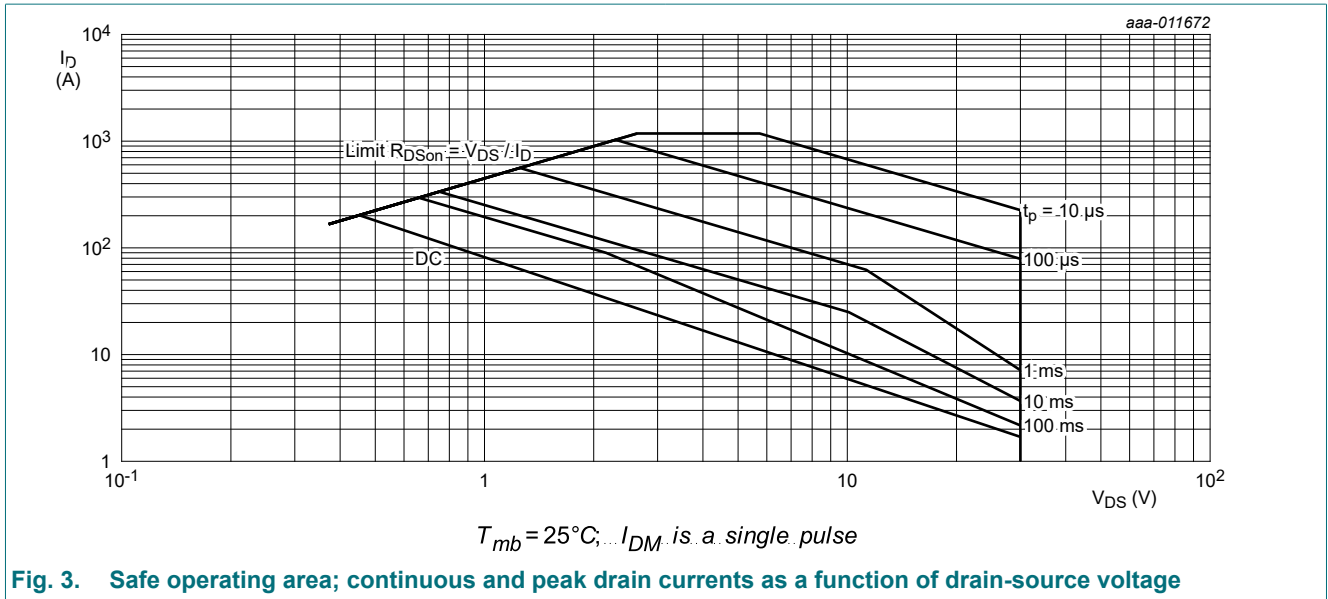


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.69	0.77	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	50	-	K/W
		Fig. 6	-	125	-	K/W

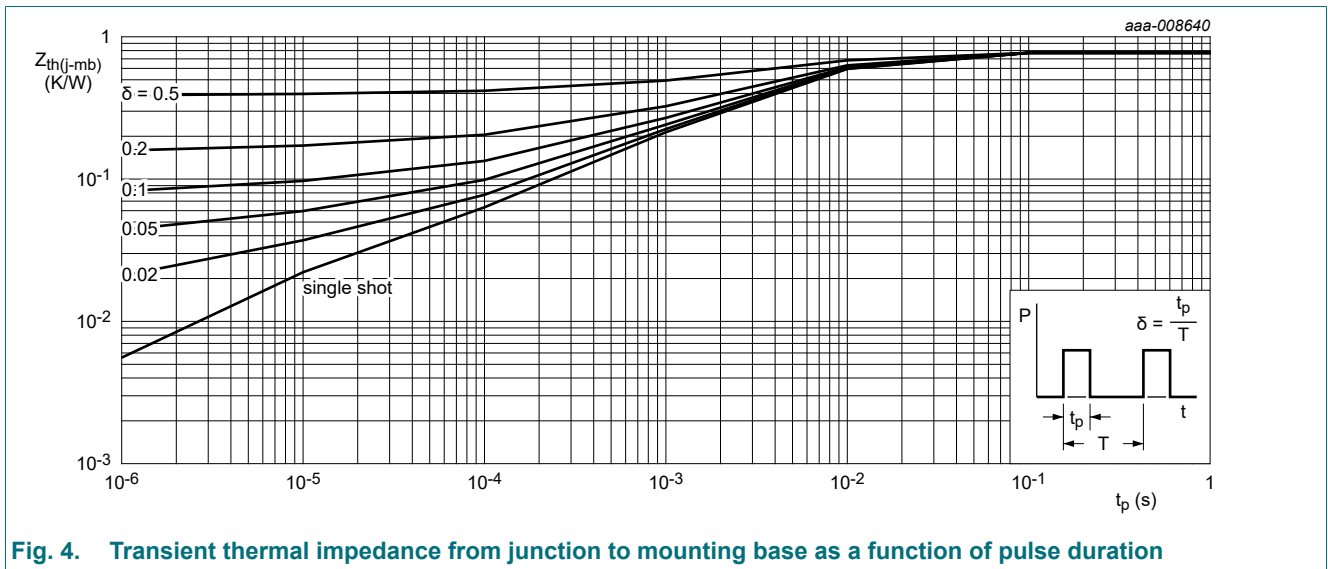
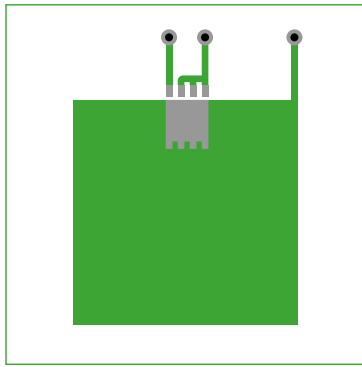
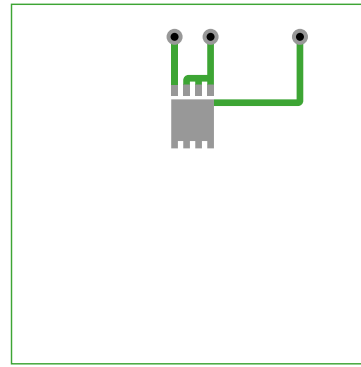


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration



aaa-005750

Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper



aaa-005751

Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint;FR4 board; 2oz copper

10. Characteristics

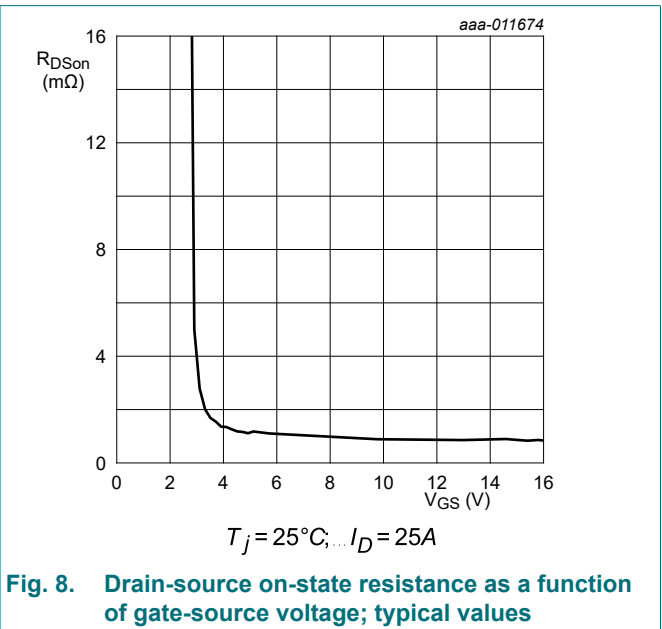
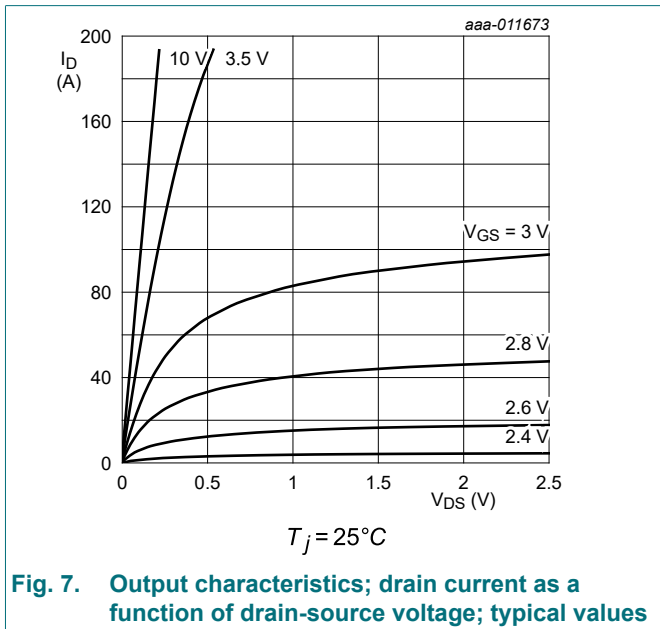
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 2 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	1.7	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-4.7	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	1.9	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 10	-	1.2	1.6	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ Fig. 10; Fig. 11	-	-	2.64	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 10	-	0.96	1.24	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ Fig. 10; Fig. 11	-	-	2.05	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	1.15	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 12; Fig. 13	-	68	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 12; Fig. 13	-	32	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	62	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 12; Fig. 13	-	9.9	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	6.4	-	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3.5	-	nC
Q_{GD}	gate-drain charge		-	9.1	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}$; $V_{DS} = 15\text{ V}$; Fig. 12; Fig. 13	-	2.5	-	V
C_{iss}	input capacitance	$V_{DS} = 15\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$;	-	4616	-	pF
C_{oss}	output capacitance	$T_j = 25\text{ °C}$; Fig. 14	-	2079	-	pF
C_{rss}	reverse transfer capacitance		-	293	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}$; $R_L = 0.6\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$;	-	25.3	-	ns
t_r	rise time	$R_{G(ext)} = 5\text{ }\Omega$	-	31	-	ns
$t_{d(off)}$	turn-off delay time		-	38.7	-	ns
t_f	fall time		-	25.5	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 15\text{ V}$; $f = 1\text{ MHz}$;	-	47.4	-	nC
		$T_j = 25\text{ °C}$				
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; Fig. 15	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	43.2	-	ns
Q_r	recovered charge	$V_{DS} = 15\text{ V}$; Fig. 16	[1]	43	-	nC
t_a	reverse recovery rise time		-	22.2	-	ns
t_b	reverse recovery fall time		-	21	-	ns
S	softness factor		-	0.95	-	

[1] includes capacitive recovery



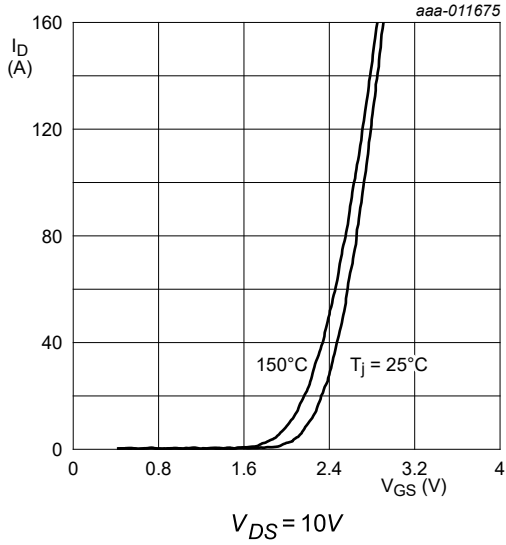


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

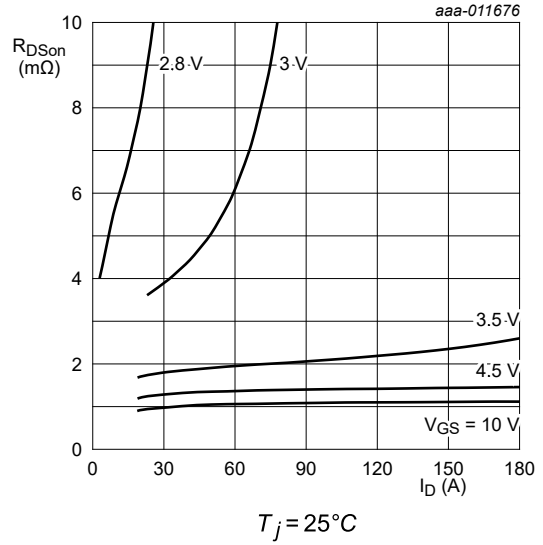


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

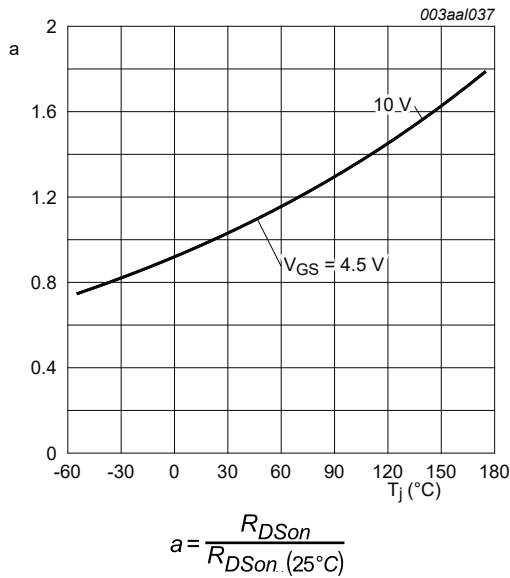


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

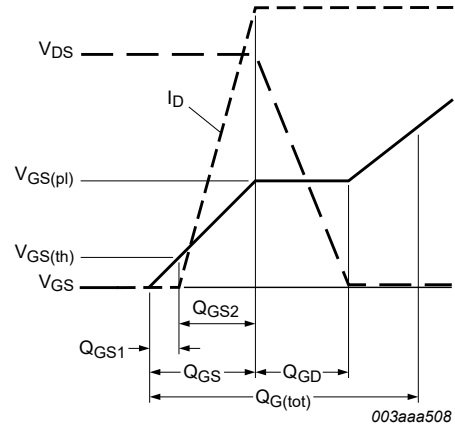


Fig. 12. Gate charge waveform definitions

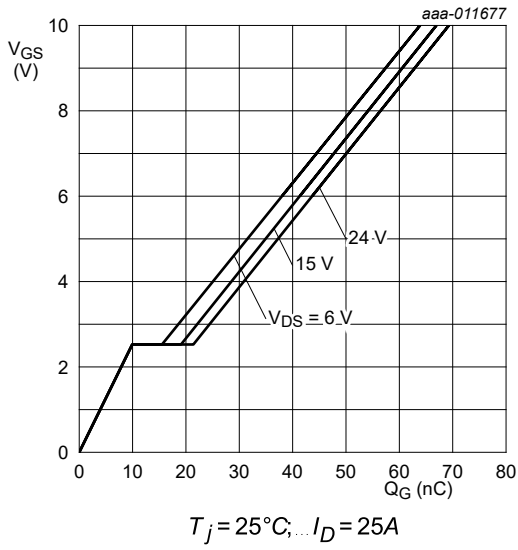


Fig. 13. Gate-source voltage as a function of gate charge; typical values

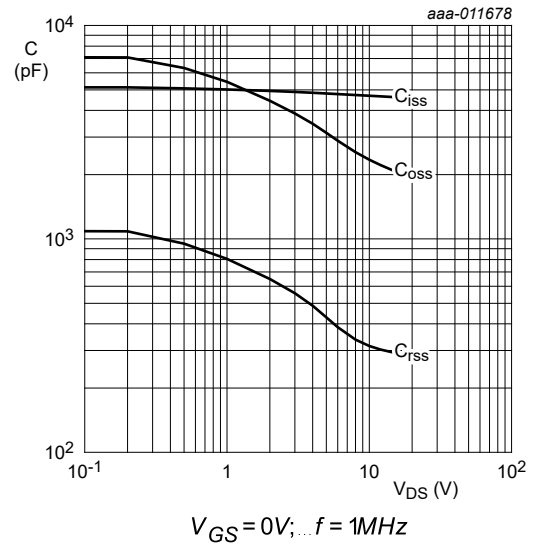


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

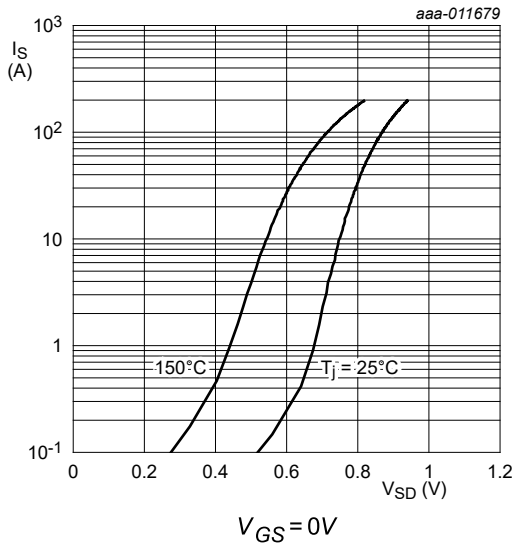


Fig. 15. Source current as a function of source-drain voltage; typical values

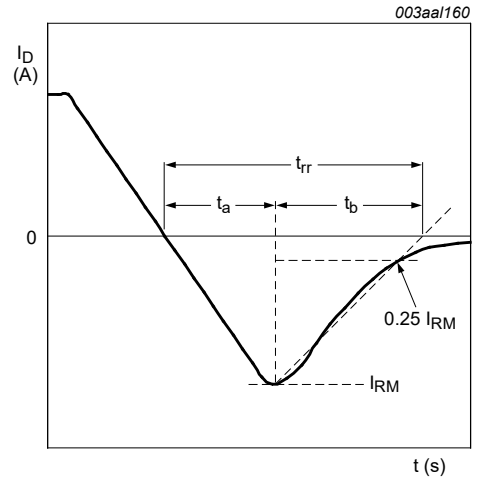


Fig. 16. Reverse recovery timing definition

11. Package outline

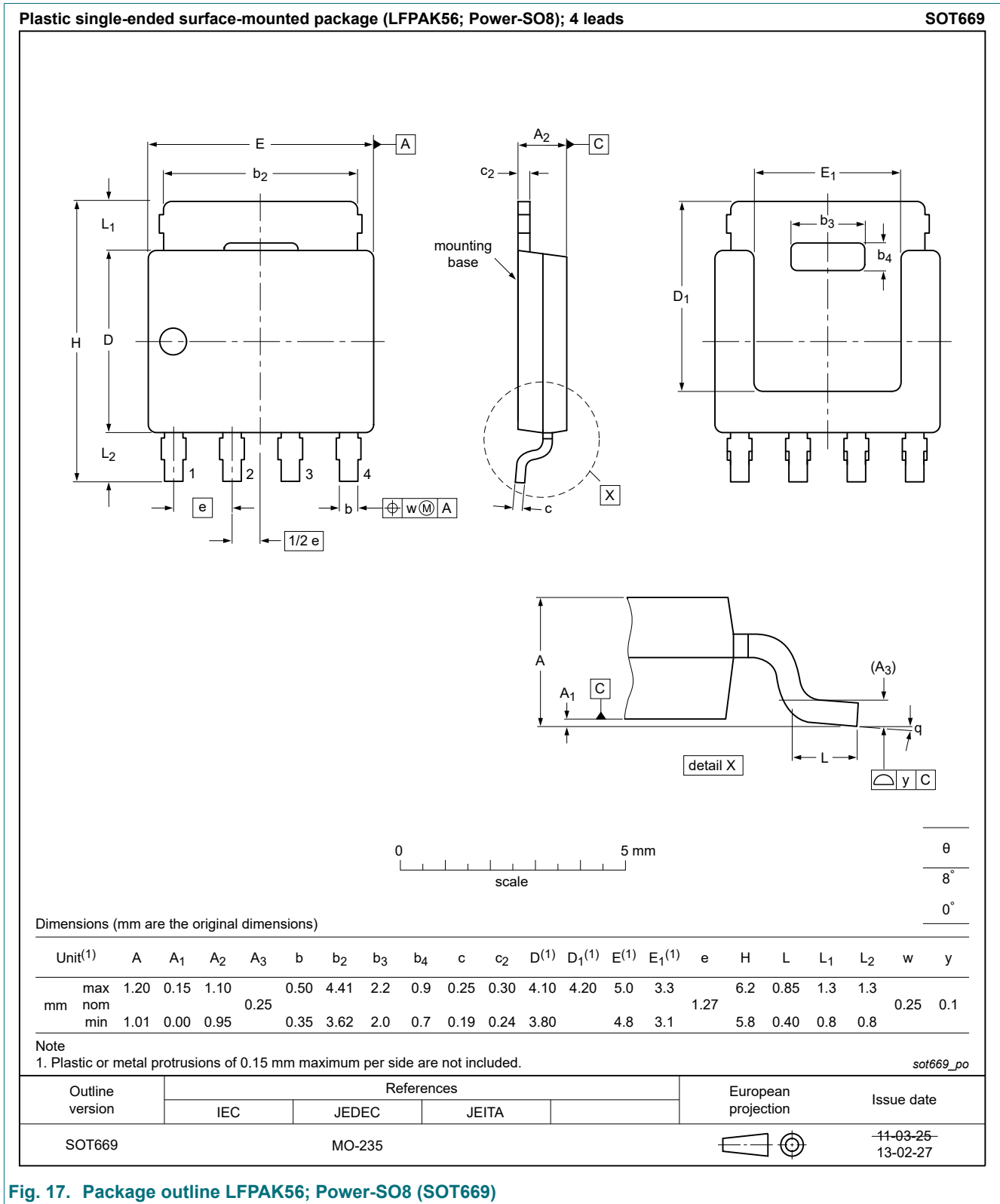


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

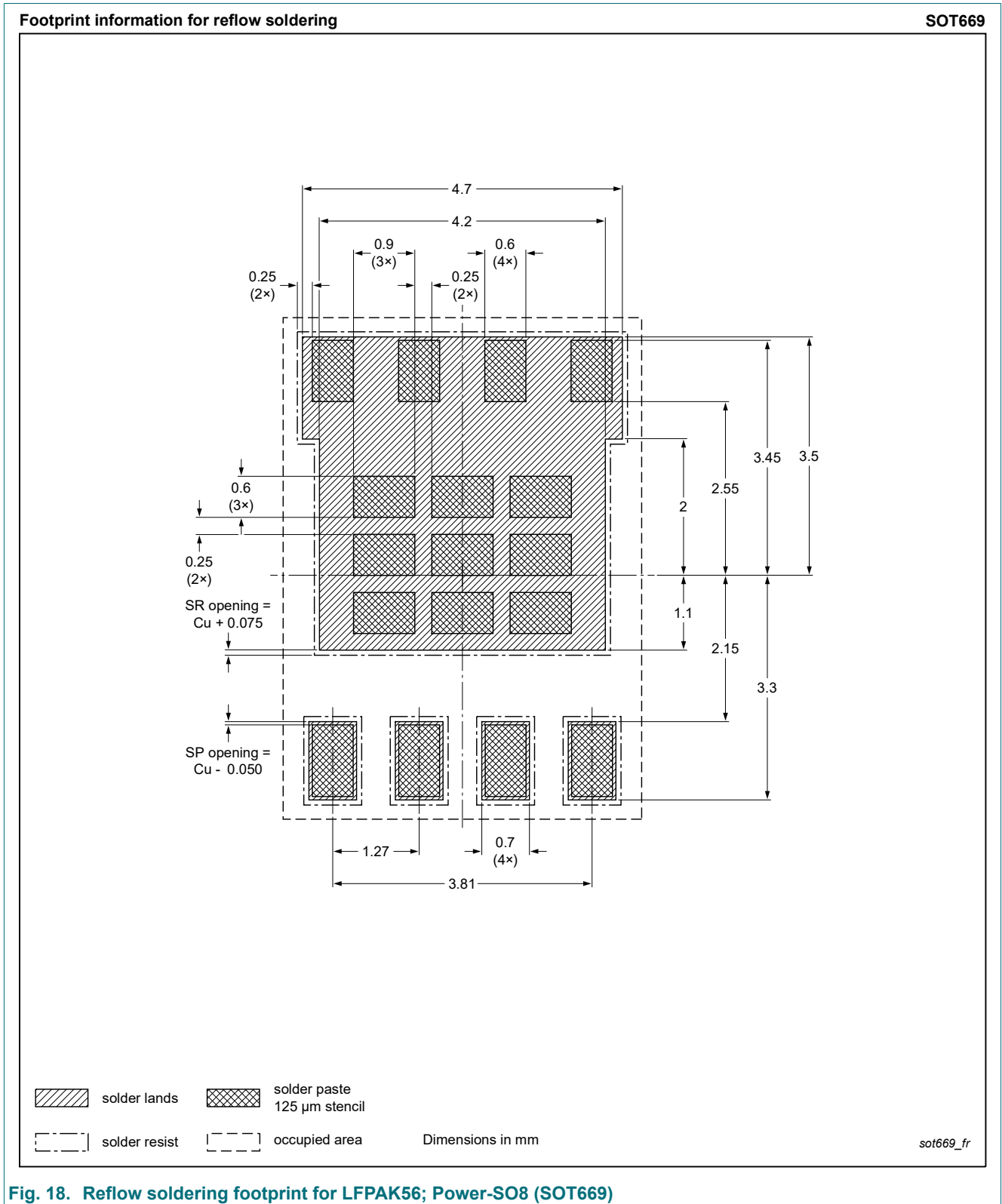
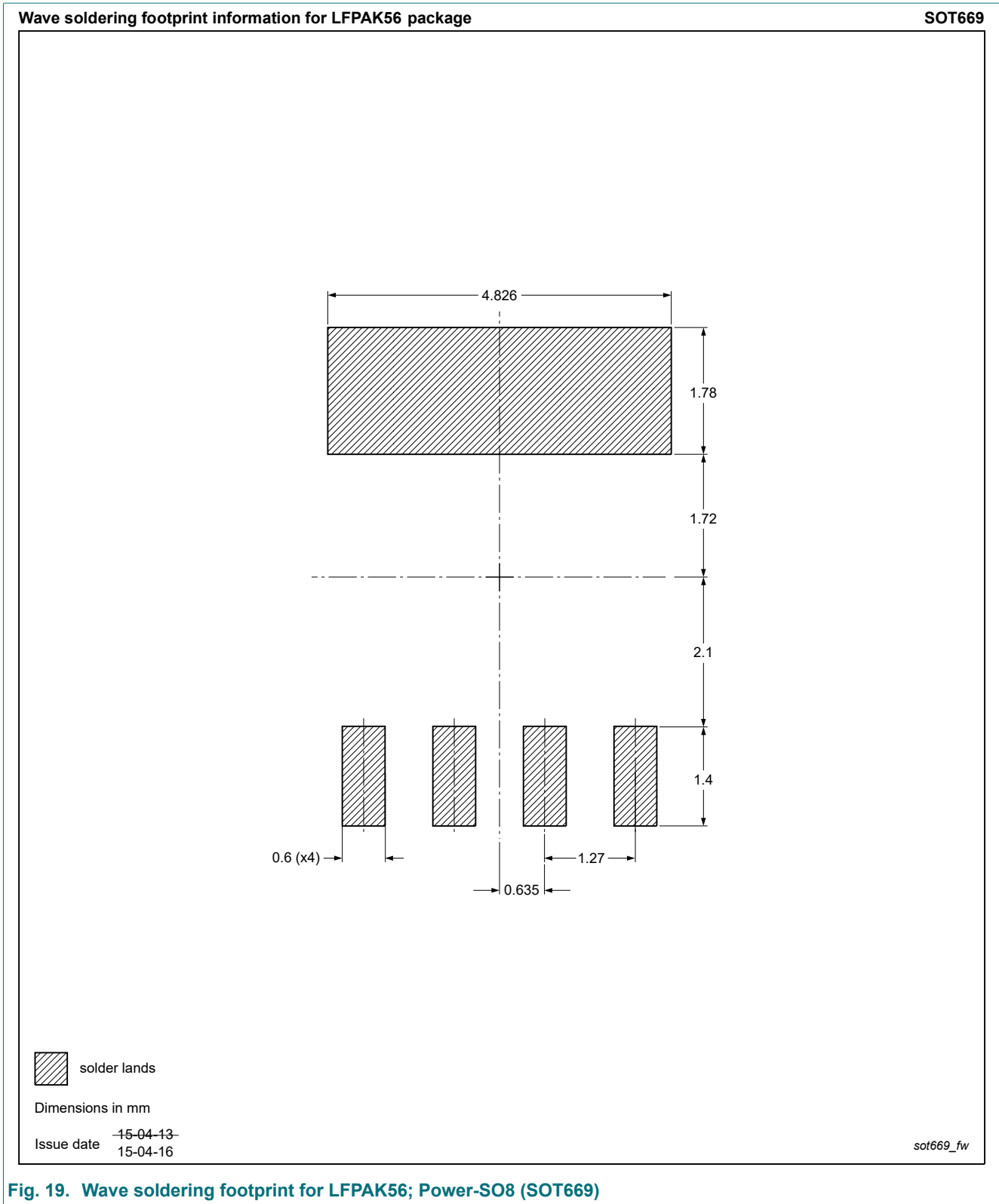


Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)



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Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 21 December 2018

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