



PSMN1R8-30MLH

N-channel 30 V, 2.1 mΩ, 150 A logic level MOSFET in LFAK33 using NextPowerS3 technology

30 September 2019

Product data sheet

1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFAK33 package. NextPowerS3 technology delivers low R_{DSon} , low I_{DSS} leakage and high efficiency. Rated to 150 A and optimized with low gate resistance (R_G) for fast-switching applications.

2. Features and benefits

- Optimized for low R_{DSon} and low gate resistance (R_G)
- Fast switching – reduced switching losses
- Strong linear-mode (SOA) rating
- Low leakage < 1 μ A at 25 °C
- Low spiking and ringing for low EMI designs
- Optimized for 4.5 V gate drive
- 150 A continuous $I_{D(max)}$ rating
- High reliability copper-clip bonded and solder die attach LFAK33 package
- Qualified to 175 °C
- Exposed leads for optimal visual solder inspection

3. Applications

- Synchronous buck regulator
- Synchronous rectifier in AC-DC and DC-DC applications
- BLDC (brushless) motor control
- eFuse and battery protection

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	30	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	150	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	106	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	1.76	2.1	mΩ
		$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	2.4	2.9	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 15\text{ V}$; $V_{GS} = 4.5\text{ V}$; Fig. 12 ; Fig. 13	1	5.6	11.2	nC
$Q_{G(tot)}$	total gate charge		7.7	17	28	nC

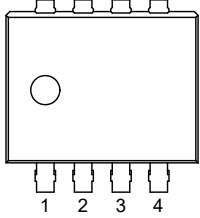
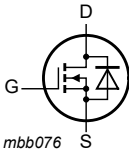
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
S	softness factor	$I_S = 25$ A; $di_S/dt = -100$ A/ μ s; $V_{GS} = 0$ V; $V_{DS} = 15$ V; Fig. 16	-	0.87	-	

[1] 150A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFAK33 (SOT1210)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN1R8-30MLH	LFAK33	Plastic, single ended surface mounted package (LFAK33); 8 leads; 0.65 mm pitch	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R8-30MLH	1H830L

8. Limiting values

Table 5. Limiting values

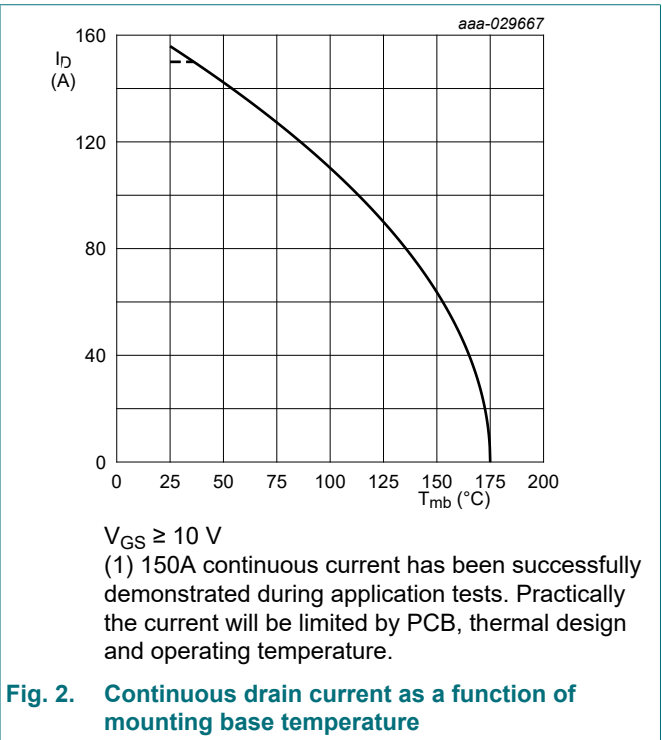
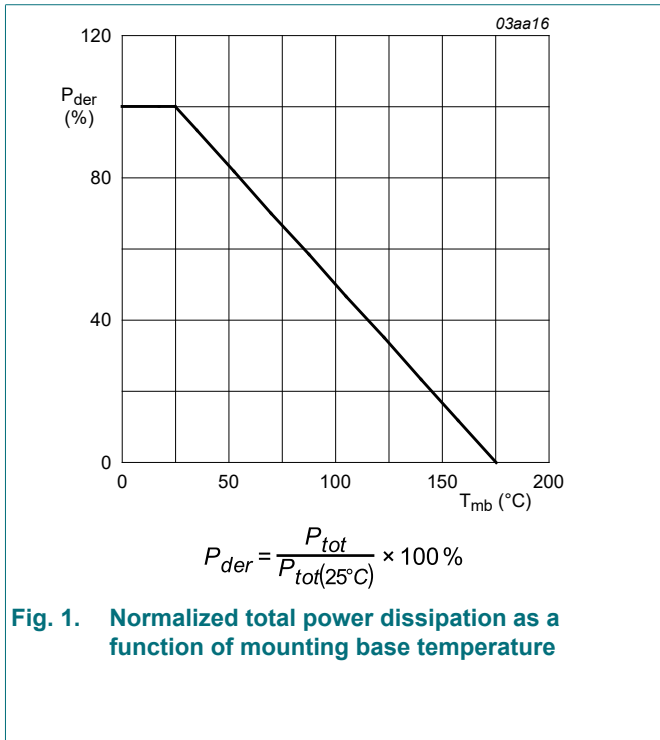
In accordance with the Absolute Maximum Rating System (IEC 60134).

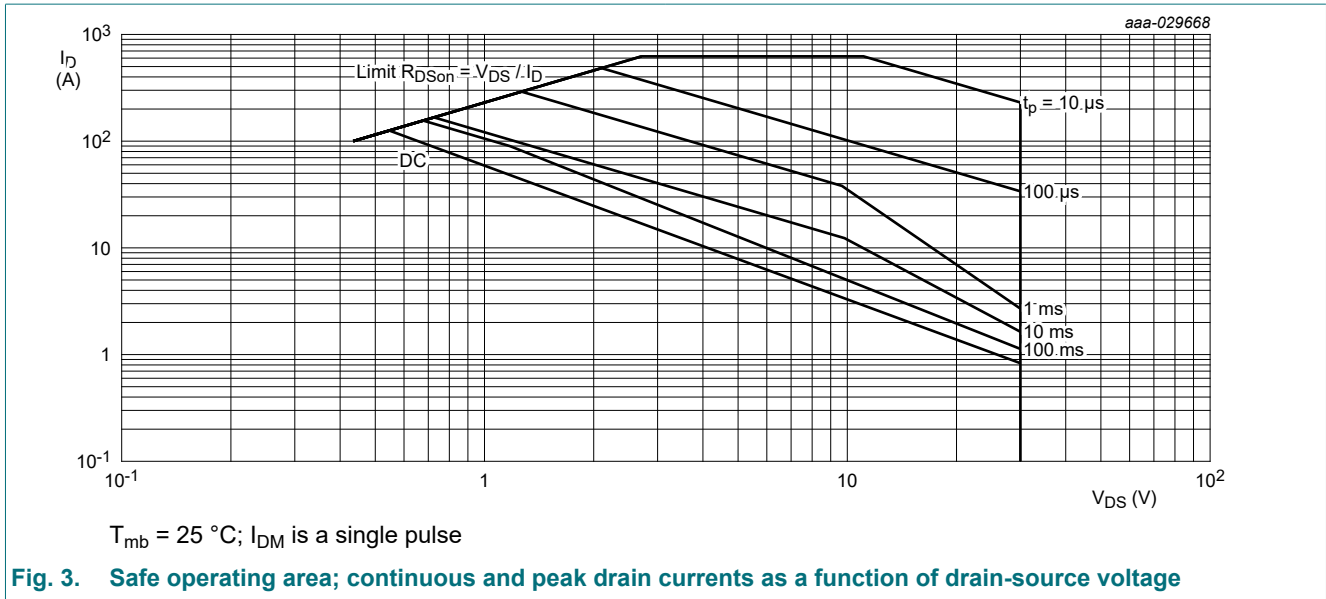
Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	-	30	V	
V_{DGR}	drain-gate voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$; $R_{GS} = 20$ k Ω	-	30	V	
V_{GS}	gate-source voltage		-20	20	V	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 1	-	106	W	
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 2	[1]	-	150	A
		$V_{GS} = 10$ V; $T_{mb} = 100\text{ }^\circ\text{C}$; Fig. 2		-	110	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu$ s; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 3	-	624	A	
T_{stg}	storage temperature		-55	175	$^\circ\text{C}$	

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Symbol	Parameter	Conditions	Min	Max	Unit
T _j	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	106	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	624	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 25 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 546 μs	[2]	-	266 mJ
I _{AS}	non-repetitive avalanche current	V _{sup} = 30 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[2]	-	87 A

- [1] 150A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature
- [2] Protected by 100% test

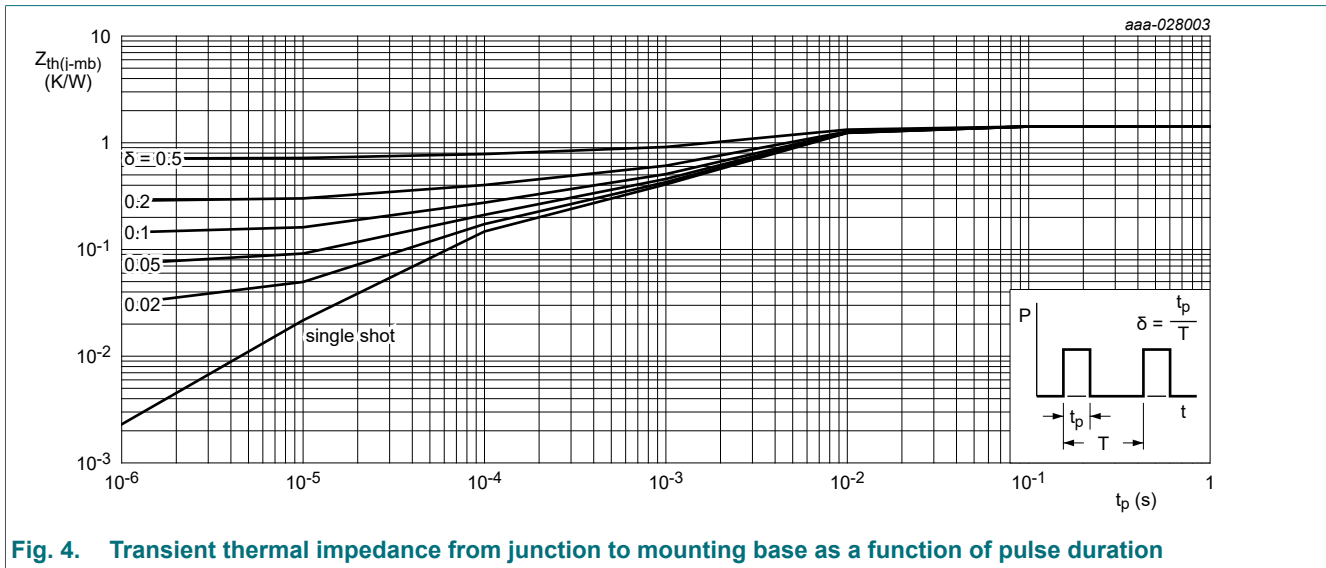


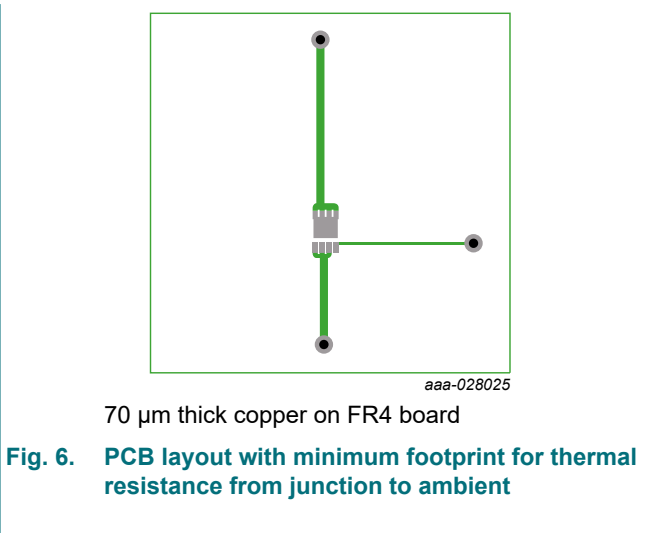
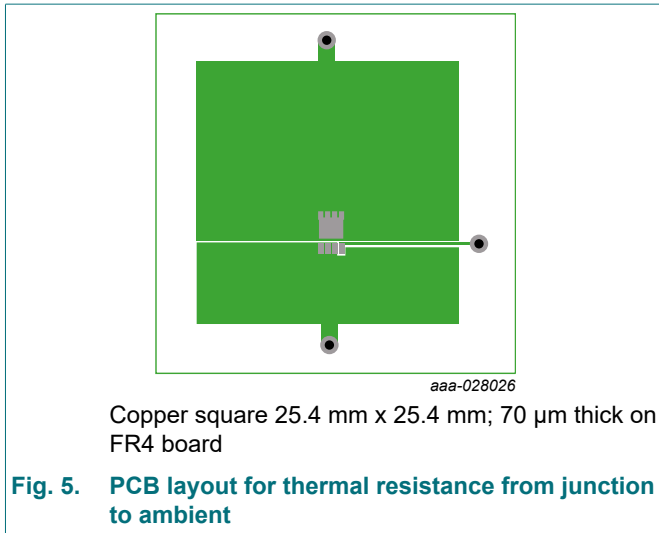


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	1.12	1.42	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	50	-	K/W
		Fig. 6	-	130	-	K/W





10. Characteristics

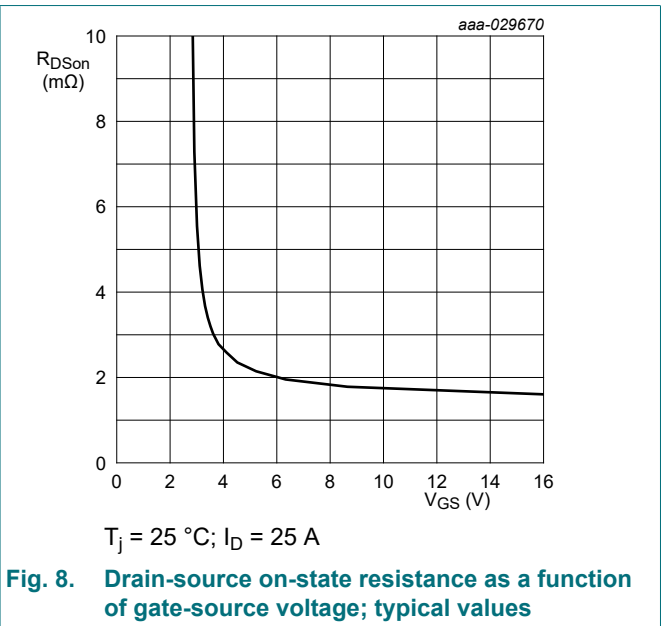
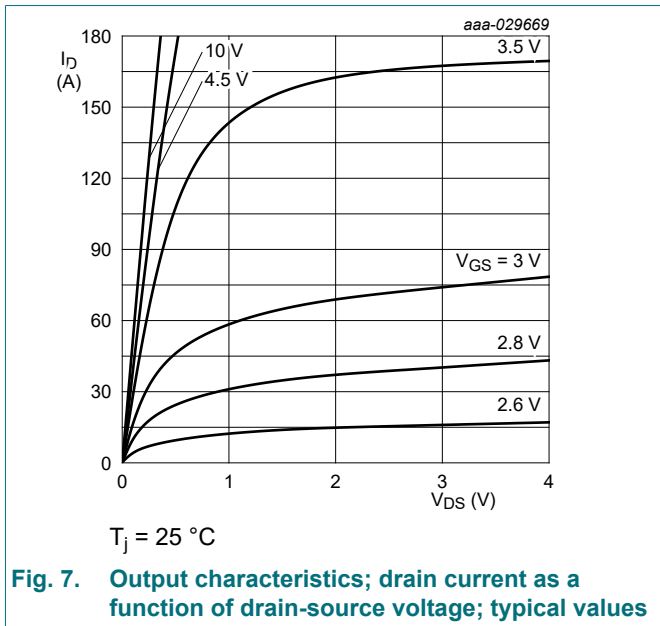
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	1.73	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-4.1	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	1.6	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 10	-	1.76	2.1	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ Fig. 11	-	-	3.9	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 10	-	2.4	2.9	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ Fig. 11	-	-	5.3	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.4	1.1	2.8	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 12; Fig. 13	7.7	17	28	nC
		$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 12; Fig. 13	15.8	35	58	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	19	-	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Q_{GS}	gate-source charge	$I_D = 25\text{ A}; V_{DS} = 15\text{ V}; V_{GS} = 4.5\text{ V};$ Fig. 12 ; Fig. 13	1.4	5.3	10.1	nC	
$Q_{GS(th)}$	pre-threshold gate-source charge		0.86	3.2	6.1	nC	
$Q_{GS(th-pl)}$	post-threshold gate-source charge		0.6	2.2	4.2	nC	
Q_{GD}	gate-drain charge		1	5.6	11.2	nC	
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}; V_{DS} = 15\text{ V};$ Fig. 12 ; Fig. 13	-	2.8	-	V	
C_{iss}	input capacitance	$V_{DS} = 15\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14	1250	2083	3125	pF	
C_{oss}	output capacitance		741	1235	1853	pF	
C_{rss}	reverse transfer capacitance		45	167	401	pF	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}; R_L = 0.6\text{ }\Omega; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega$	-	14	-	ns	
t_r	rise time		-	23	-	ns	
$t_{d(off)}$	turn-off delay time		-	20	-	ns	
t_f	fall time		-	14	-	ns	
Q_{oss}	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C}$	-	26	-	nC	
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 15	-	0.79	1	V	
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 15\text{ V};$ Fig. 16	-	30	-	ns	
Q_r	recovered charge		[1]	-	23	-	nC
t_a	reverse recovery rise time		-	16	-	ns	
t_b	reverse recovery fall time		-	14	-	ns	
S	softness factor		-	0.87	-		

[1] includes capacitive recovery



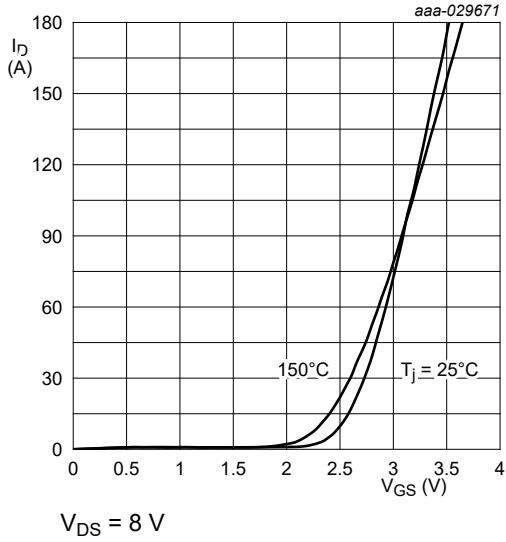


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

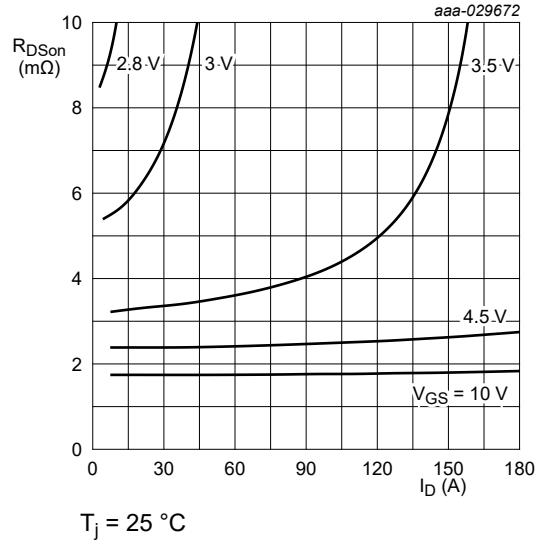


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

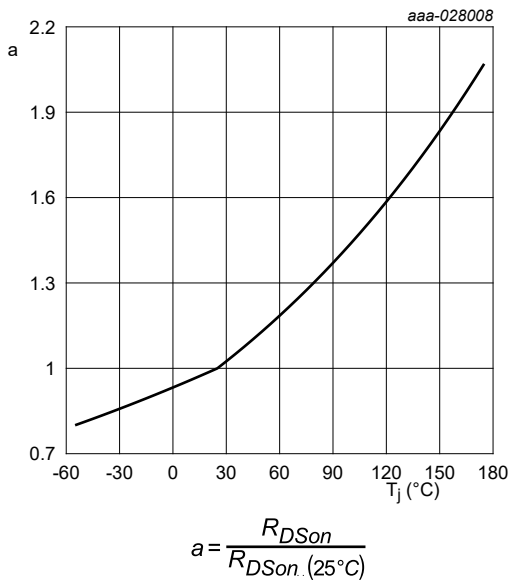


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

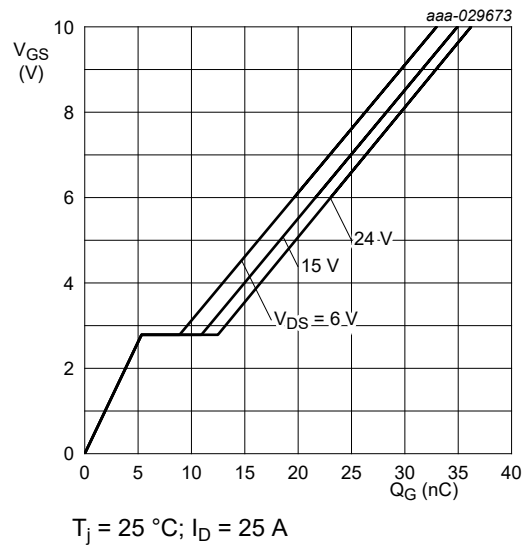


Fig. 12. Gate-source voltage as a function of gate charge; typical values



Fig. 13. Gate charge waveform definitions

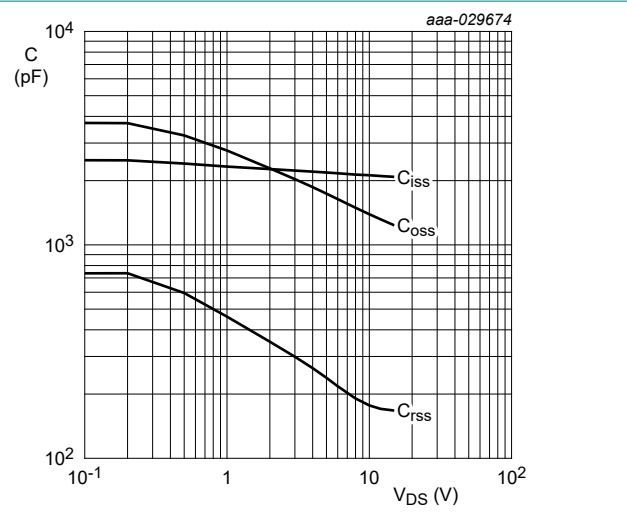


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values
 $V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

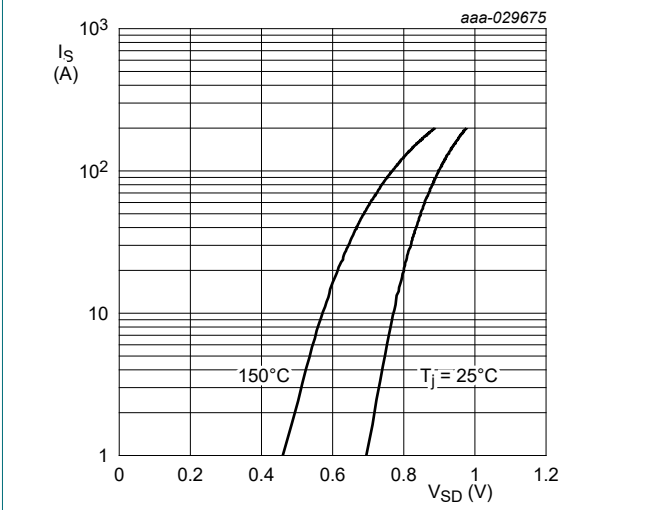


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values
 $V_{GS} = 0 \text{ V}$

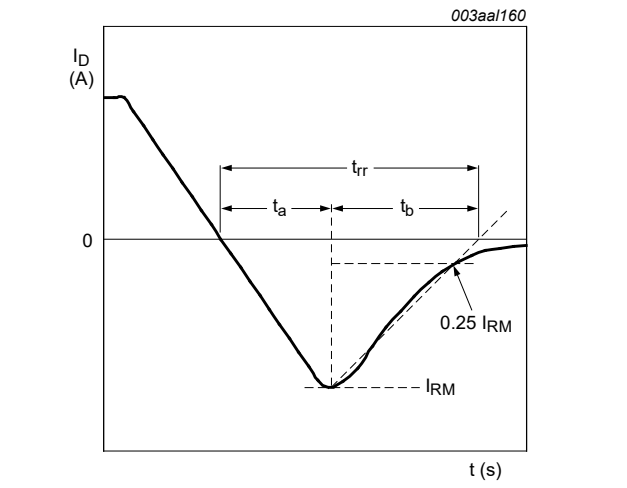


Fig. 16. Reverse recovery timing definition

11. Package outline

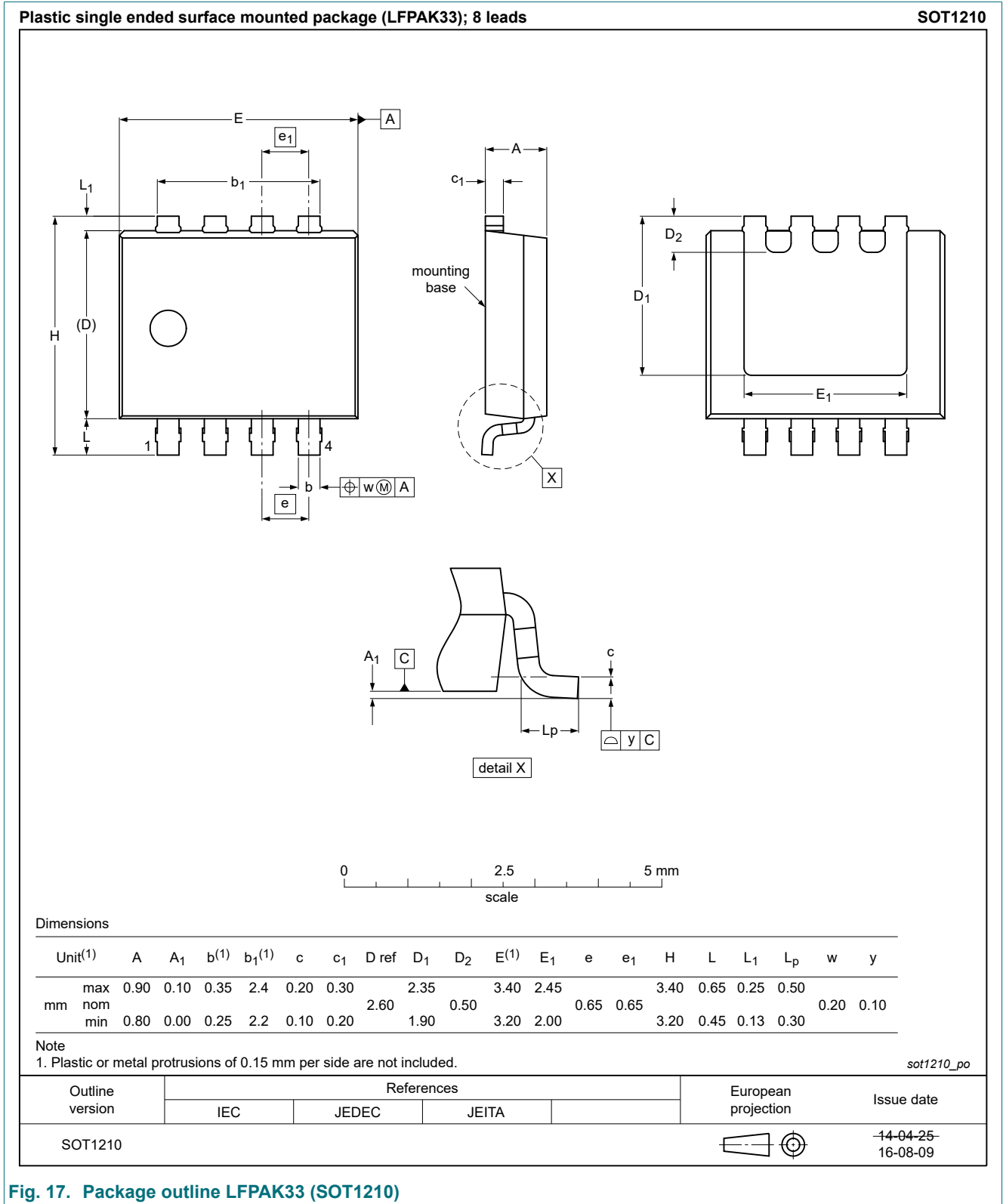


Fig. 17. Package outline LPAK33 (SOT1210)

12. Soldering

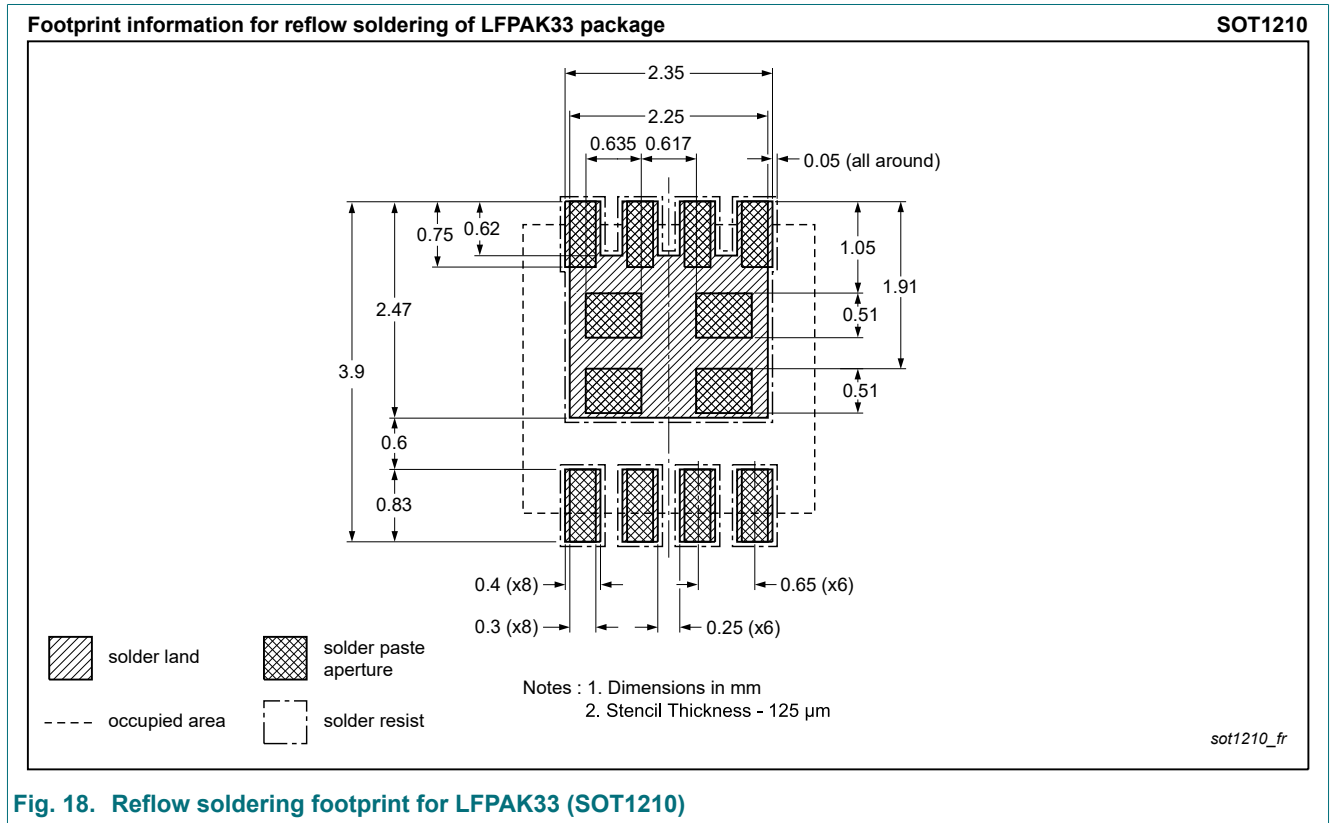


Fig. 18. Reflow soldering footprint for LPAK33 (SOT1210)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 30 September 2019

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