



# PSMN1R8-40YLC

N-channel 40 V 1.8 mΩ logic level MOSFET in LFPAK using NextPower technology

22 August 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads
- Ultra low R<sub>ds(on)</sub> and low parasitic inductance

### 1.3 Applications

- DC-to-DC converters
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	-	40	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; <a href="#">Fig. 1</a>	[1]	-	100	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	-	-	272	W
T <sub>j</sub>	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 12</a>	-	1.8	2.1	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 12</a>	-	1.5	1.8	mΩ
<b>Dynamic characteristics</b>						
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>	-	10.9	-	nC

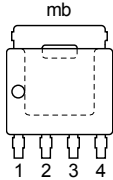
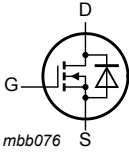
### N-channel 40 V 1.8 mΩ logic level MOSFET in LPAK using NextPower technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(\text{tot})}$	total gate charge	$V_{GS} = 4.5 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $V_{DS} = 20 \text{ V}$ ; <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>	-	45	-	nC

[1] Continuous current is limited by package.

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R8-40YLC	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

## 4. Limiting values

Table 4. Limiting values

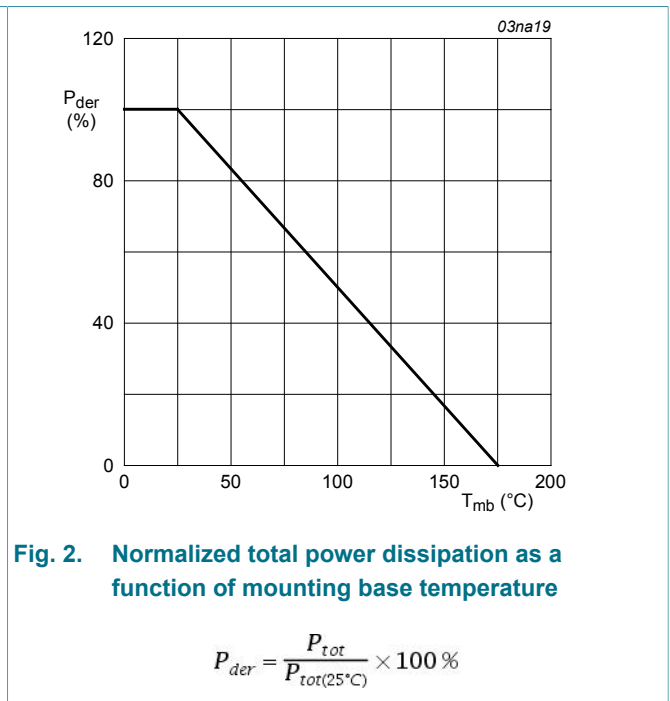
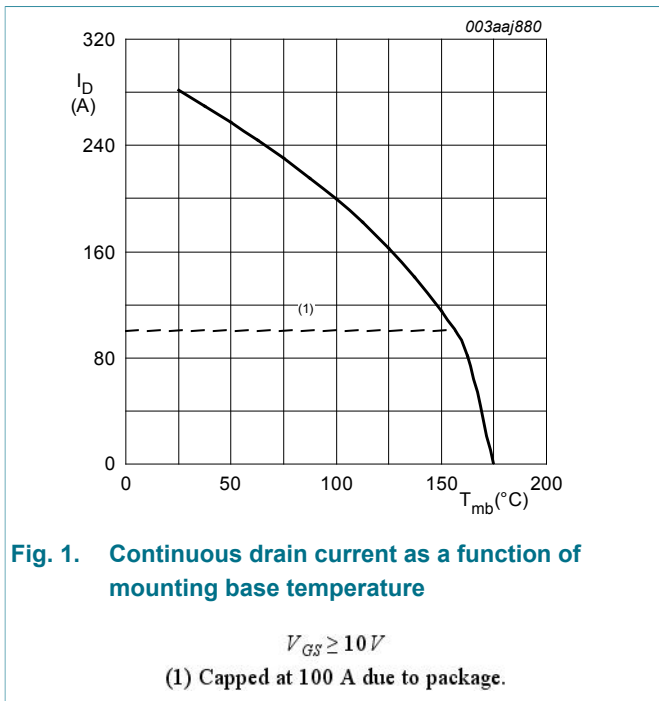
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$25 \text{ °C} \leq T_j \leq 175 \text{ °C}$	-	40	V	
$V_{DGR}$	drain-gate voltage	$25 \text{ °C} \leq T_j \leq 175 \text{ °C}$ ; $R_{GS} = 20 \text{ k}\Omega$	-	40	V	
$V_{GS}$	gate-source voltage		-20	20	V	
$I_D$	drain current	$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 25 \text{ °C}$ ; <a href="#">Fig. 1</a>	[1]	-	100	A
		$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 100 \text{ °C}$ ; <a href="#">Fig. 1</a>	[1]	-	100	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10 \text{ }\mu\text{s}$ ; $T_{mb} = 25 \text{ °C}$ ; <a href="#">Fig. 4</a>	-	1128	A	
$P_{\text{tot}}$	total power dissipation	$T_{mb} = 25 \text{ °C}$ ; <a href="#">Fig. 2</a>	-	272	W	
$T_{\text{stg}}$	storage temperature		-55	175	°C	
$T_j$	junction temperature		-55	175	°C	
$T_{\text{slid(M)}}$	peak soldering temperature		-	260	°C	

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Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>ESD</sub>	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	890	-	V
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	100	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	1128	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>J(init)</sub> = 25 °C; I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; unclamped; Fig. 3	-	248	mJ

[1] Continuous current is limited by package.



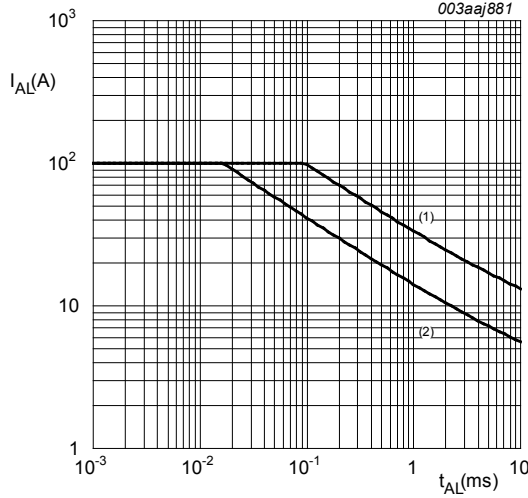


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j (init)} = 25^{\circ}C$ ; (2)  $T_{j (init)} = 100^{\circ}C$

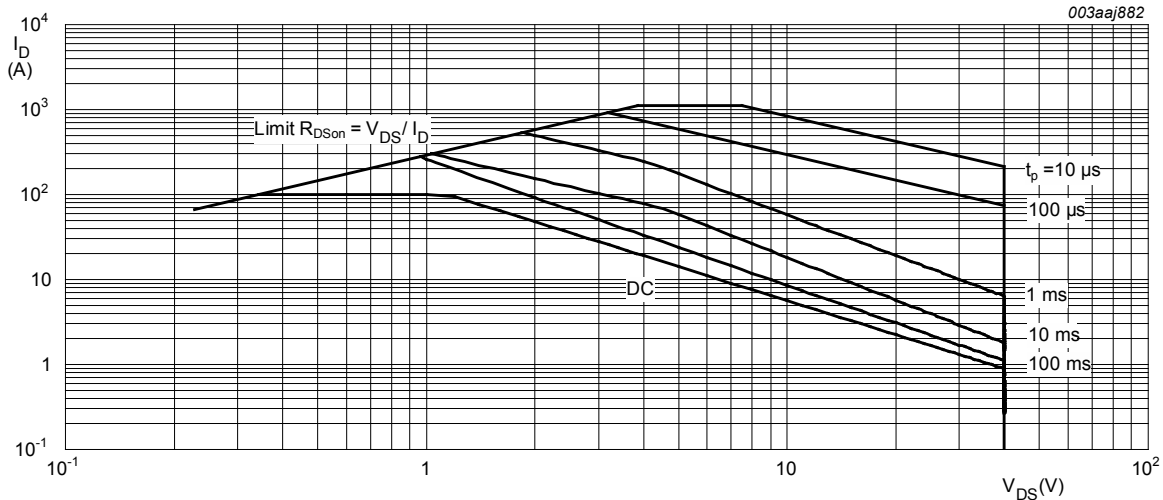


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.45	0.55	K/W

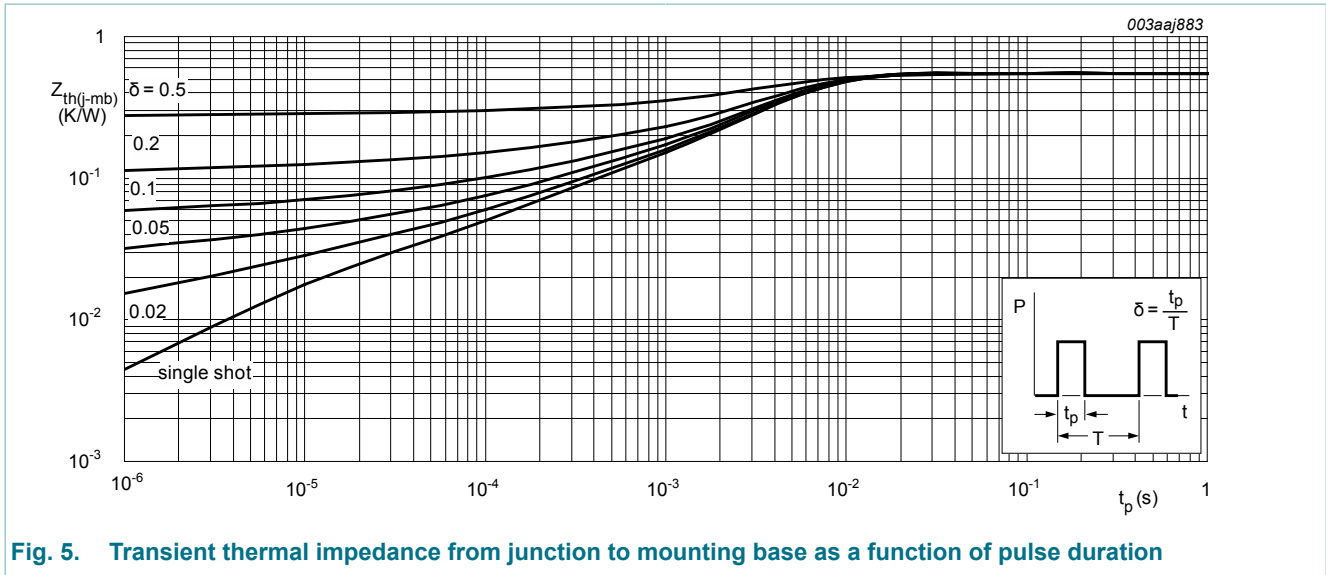


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	1.05	1.45	1.95	V
		$I_D = 10 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	-	2.25	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ C$	-	-	100	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	1.8	2.1	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 13</a>	-	-	3.6	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	1.5	1.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 13</a>	-	-	3.25	mΩ

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>G</sub>	gate resistance	f = 1 MHz	0.5	1	2	Ω
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	96	-	nC
		I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>	-	45	-	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V	-	88	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>	-	15.5	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge		-	8.4	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	7.1	-	nC
Q <sub>GD</sub>	gate-drain charge		-	10.9	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>	-	2.7	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>J</sub> = 25 °C; <a href="#">Fig. 16</a>	-	6680	-	pF
C <sub>oss</sub>	output capacitance		-	825	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	310	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 20 V; R <sub>L</sub> = 0.8 Ω; V <sub>GS</sub> = 4.5 V; R <sub>G(ext)</sub> = 5 Ω	-	32.2	-	ns
t <sub>r</sub>	rise time		-	37	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	62.5	-	ns
t <sub>f</sub>	fall time		-	31.7	-	ns
Q <sub>oss</sub>	output charge	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; f = 1 MHz; T <sub>J</sub> = 25 °C	-	30	-	nC
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 17</a>	-	0.77	1.1	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 25 A; di <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V	-	37	-	ns
Q <sub>r</sub>	recovered charge		-	43	-	nC
t <sub>a</sub>	reverse recovery rise time	V <sub>GS</sub> = 0 V; I <sub>S</sub> = 25 A; di <sub>S</sub> /dt = -100 A/μs; V <sub>DS</sub> = 20 V; <a href="#">Fig. 18</a>	-	21	-	ns
t <sub>b</sub>	reverse recovery fall time		-	16	-	ns

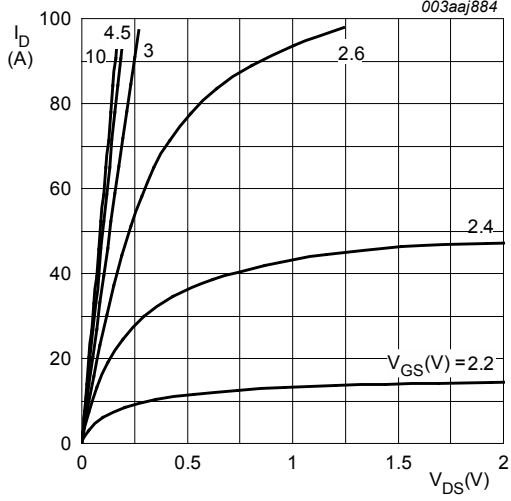


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ\text{C}$

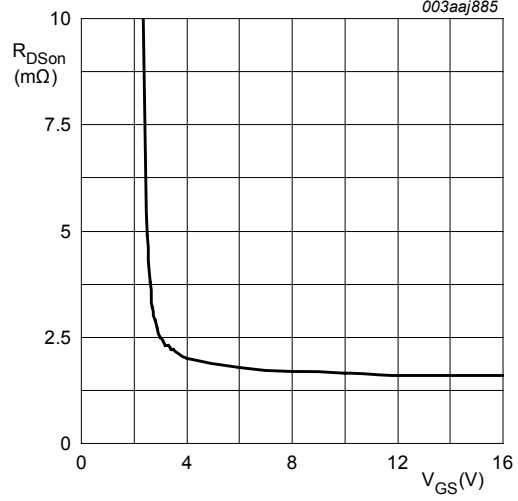


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

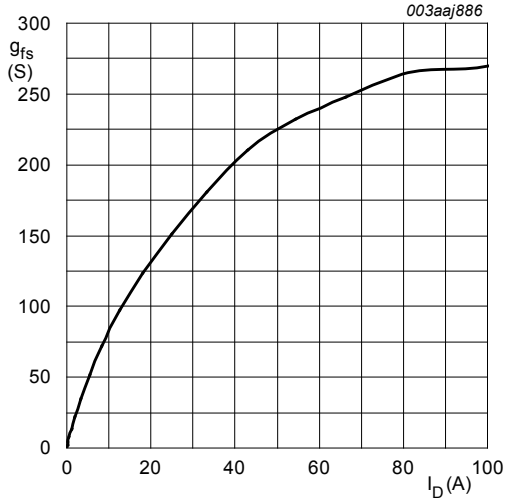


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$

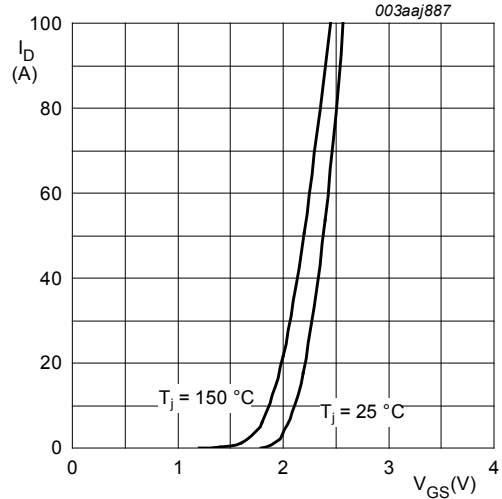


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

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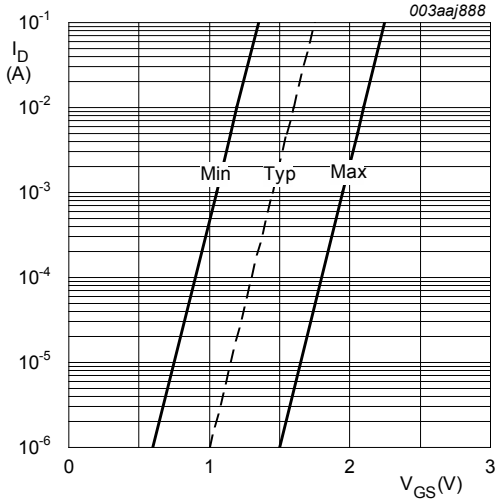


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

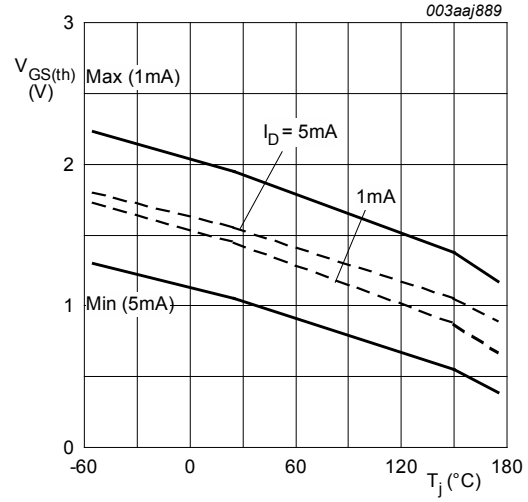


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$V_{DS} = V_{GS}$$

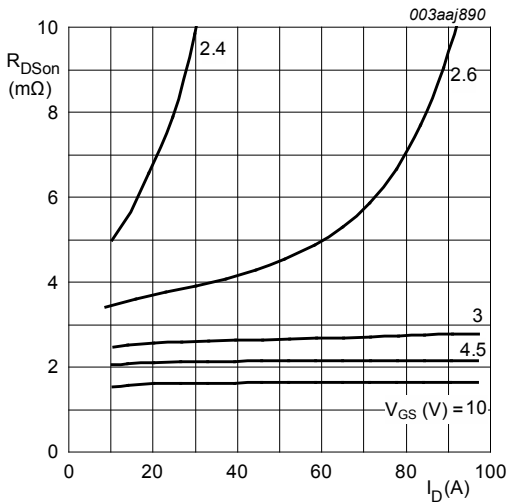


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

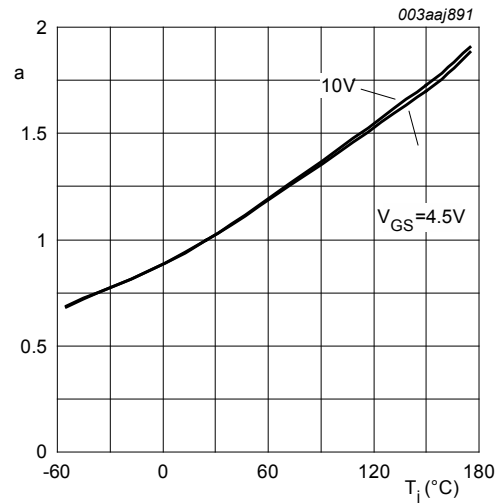


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$



N-channel 40 V 1.8 mΩ logic level MOSFET in LPAK using NextPower technology

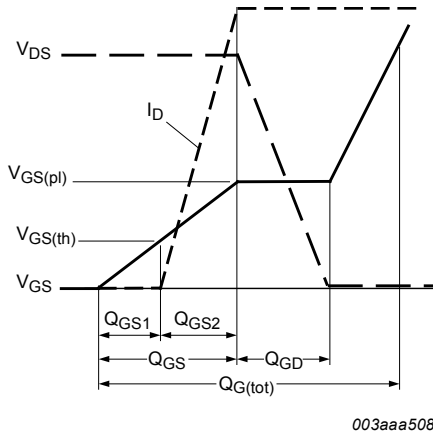


Fig. 14. Gate charge waveform definitions

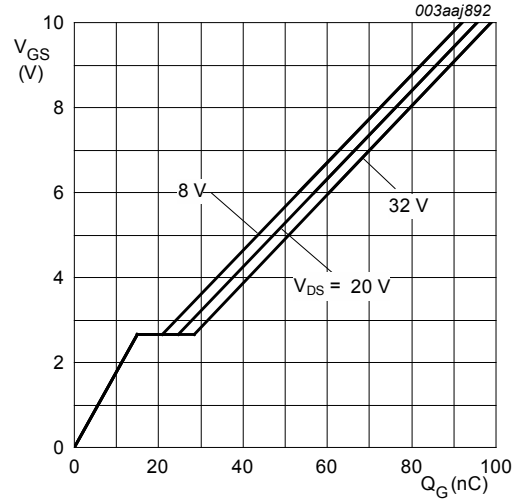


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

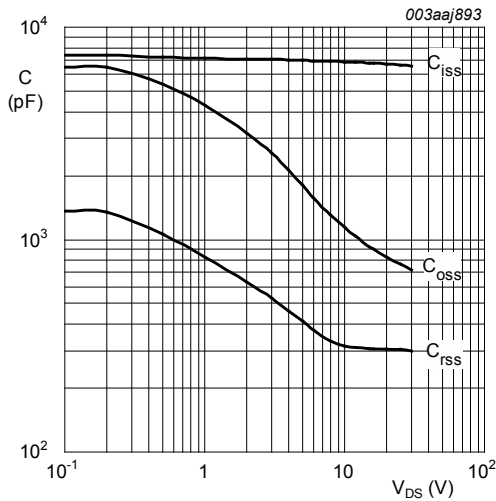


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{V}; f = 1\text{MHz}$

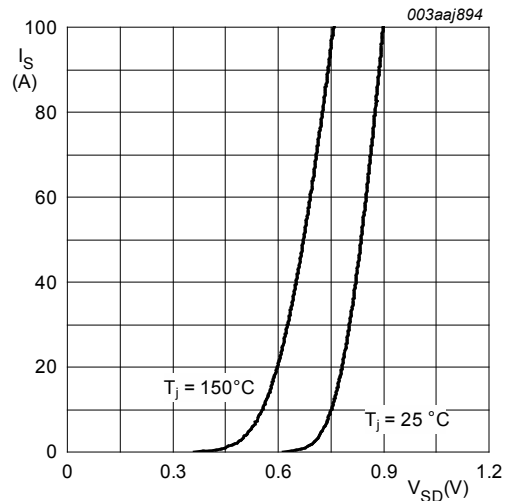


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\text{V}$

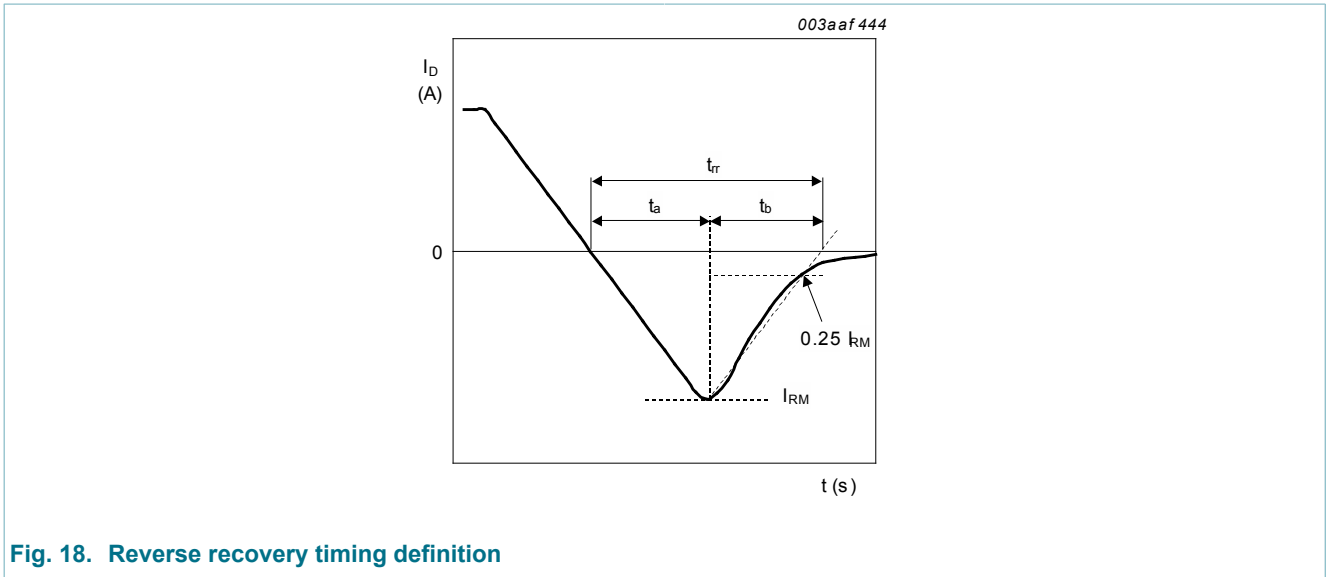


Fig. 18. Reverse recovery timing definition

### 7. Package outline

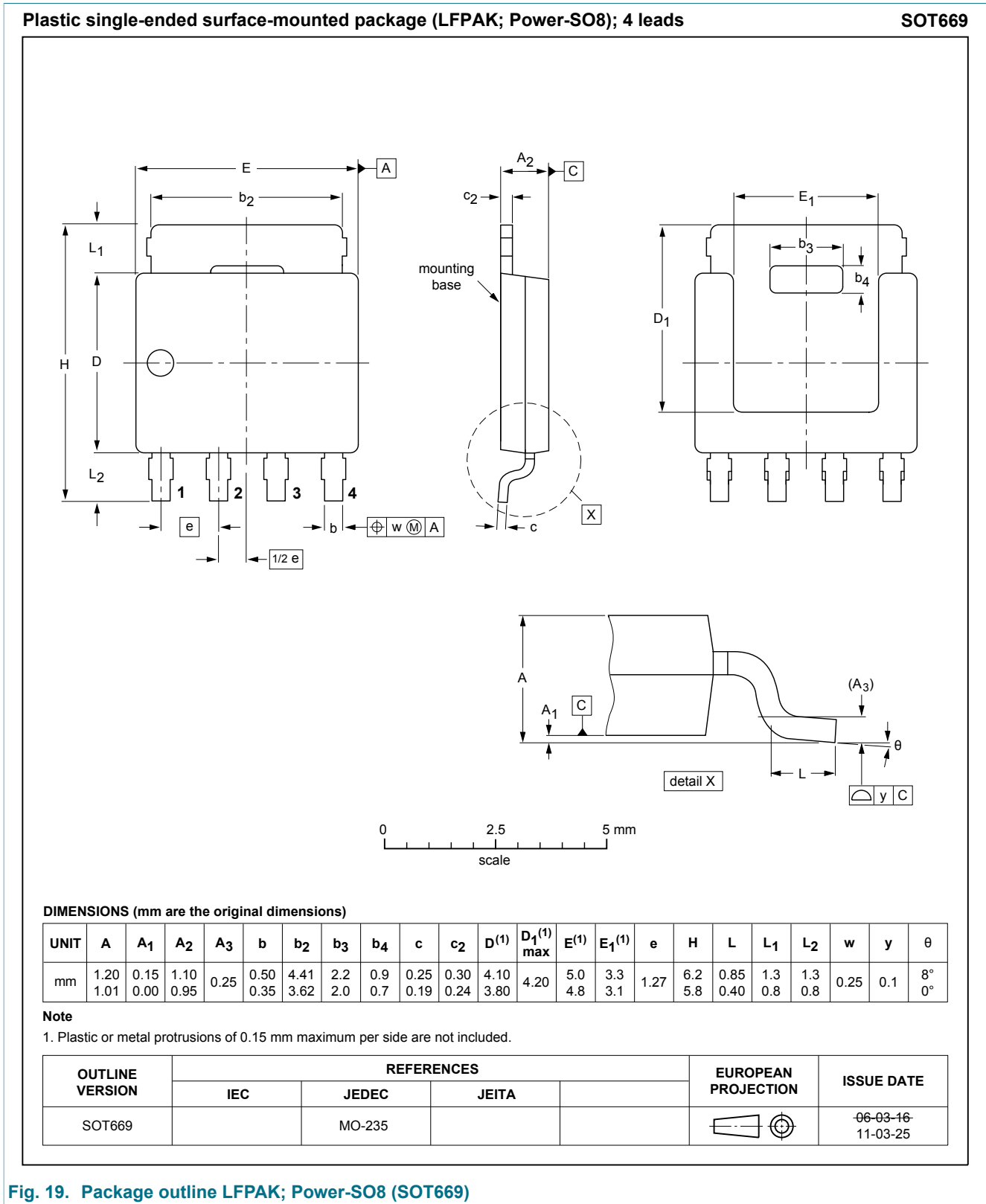


Fig. 19. Package outline LPAK; Power-SO8 (SOT669)

## 8. Legal information

### 8.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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