



PSMN2R0-25YLD

N-channel 25 V, 2.09 mΩ, 140 A logic level MOSFET in LFPAK56 using NextPowerS3 Technology

19 April 2016

Product data sheet

1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFPAK56 package. NextPowerS3 portfolio utilising Nexperia's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETS with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

2. Features and benefits

- 100% Avalanche tested at $I_{(AS)} = 100$ A
- Ultra low Q_G , Q_{GD} and Q_{OSS} for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with < 1 μ A leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Wave solderable; exposed leads for optimal visual solder inspection

3. Applications

- On-board DC:DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------|-------------------------|---|-----|-----|-----|-----|------|
| V_{DS} | drain-source voltage | $25\text{ °C} \leq T_j \leq 175\text{ °C}$ | | - | - | 25 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2 | [1] | - | - | 100 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 1 | | - | - | 115 | W |

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N-channel 25 V, 2.09 mΩ, 140 A logic level MOSFET in LFAK56 using NextPowerS3 Technology

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---|-----|------|------|------|
| T_j | junction temperature | | -55 | - | 175 | °C |
| Static characteristics | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ Fig. 10 | - | 2.41 | 2.91 | mΩ |
| | | $V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ Fig. 10 | - | 1.82 | 2.09 | mΩ |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 25\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 10\text{ V};$ Fig. 12; Fig. 13 | - | 34.1 | - | nC |
| | | $I_D = 25\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 4.5\text{ V};$ Fig. 12; Fig. 13 | - | 15.7 | - | nC |
| | | $I_D = 0\text{ A}; V_{DS} = 0\text{ V}; V_{GS} = 10\text{ V}$ | - | 15.2 | - | nC |
| Q_{GD} | gate-drain charge | $I_D = 25\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 4.5\text{ V};$ Fig. 12; Fig. 13 | - | 3.6 | - | nC |
| Source-drain diode | | | | | | |
| S | softness factor | $I_S = 25\text{ A}; di_S/dt = -100\text{ A/s}; V_{GS} = 0\text{ V};$ $V_{DS} = 12\text{ V};$ Fig. 16 | - | 1 | - | |

[1] Continuous current is limited by package

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|-----------------------------------|----------------|
| 1 | S | source | <p>LFAK56; Power-SO8 (SOT669)</p> | <p>mbb076</p> |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|---------------|----------------------|---|---------|
| | Name | Description | Version |
| PSMN2R0-25YLD | LFAK56; Power-SO8 | Plastic single-ended surface-mounted package (LFAK56; Power-SO8); 4 leads | SOT669 |

N-channel 25 V, 2.09 mΩ, 140 A logic level MOSFET in LPAK56 using
NextPowerS3 Technology

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|---------------|--------------|
| PSMN2R0-25YLD | 2D025L |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-----------------------------|--|---|-----|-----|-----|------|
| V_{DS} | drain-source voltage | $25\text{ °C} \leq T_j \leq 175\text{ °C}$ | | - | 25 | V |
| V_{DGR} | drain-gate voltage | $25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$ | | - | 25 | V |
| V_{GS} | gate-source voltage | | | -20 | 20 | V |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 1 | | - | 115 | W |
| I_D | drain current | $V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2 | [1] | - | 100 | A |
| | | $V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2 | [1] | - | 100 | A |
| I_{DM} | peak drain current | pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3 | | - | 722 | A |
| T_{stg} | storage temperature | | | -55 | 175 | °C |
| T_j | junction temperature | | | -55 | 175 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |
| V_{ESD} | electrostatic discharge voltage | HBM (JEDEC) | | 600 | - | V |
| Source-drain diode | | | | | | |
| I_S | source current | $T_{mb} = 25\text{ °C}$ | | - | 95 | A |
| I_{SM} | peak source current | pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$ | | - | 722 | A |
| Avalanche ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 25\text{ A}$; $V_{sup} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; unclamped; $t_p = 1.01\text{ ms}$ | [2] | - | 410 | mJ |

[1] Continuous current is limited by package

[2] Protected by 100% test

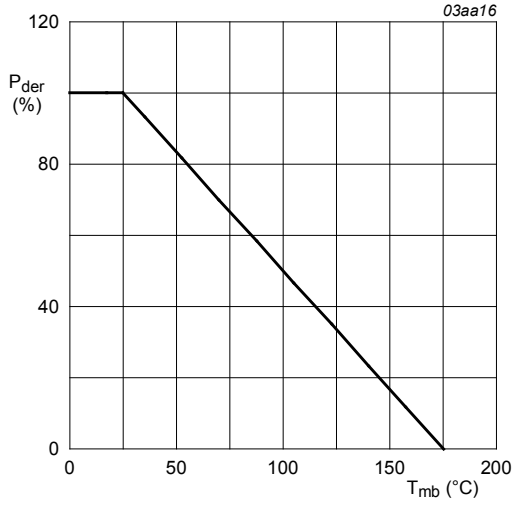
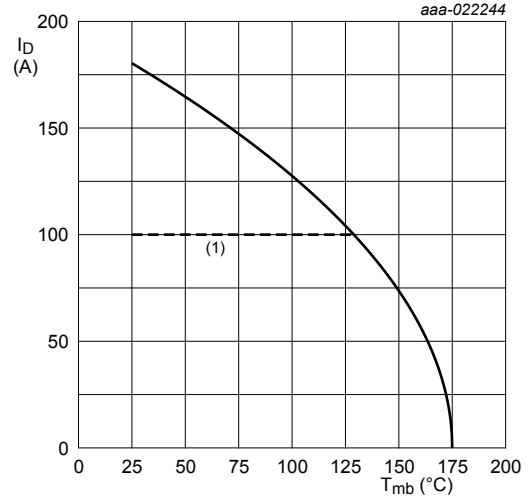


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

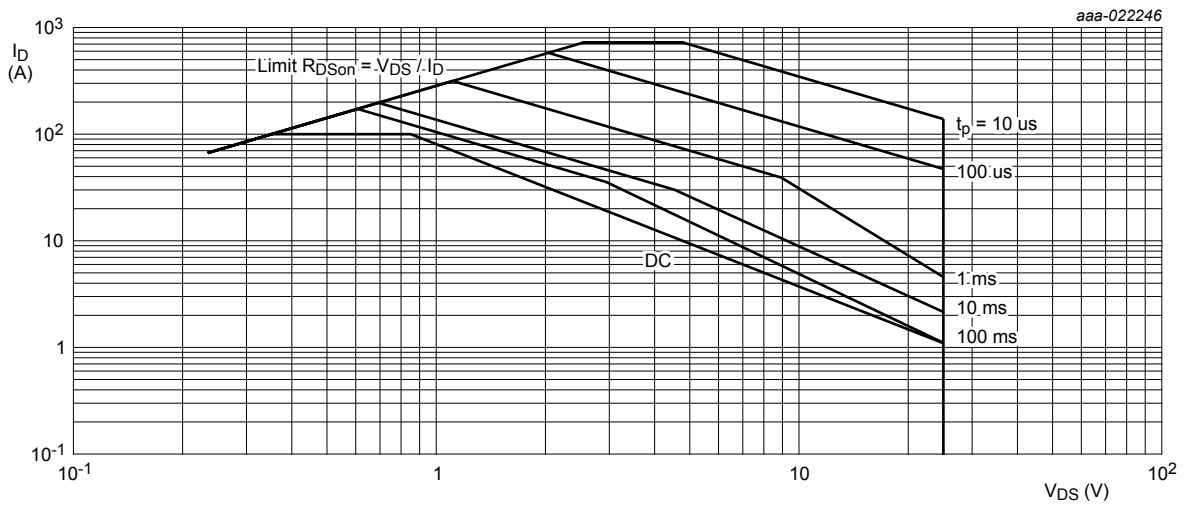


$V_{GS} \geq 10\text{ V}$

(1) Capped at 100A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

$$I_D = 180A \times \sqrt{\frac{175^{\circ}C - T_{mb}}{150^{\circ}C}} \text{ for } T_{mb} \geq 25^{\circ}C$$



$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------------------|-----|------|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 4 | - | 1.09 | 1.31 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Fig. 5 | - | 50 | - | K/W |
| | | Fig. 6 | - | 125 | - | K/W |

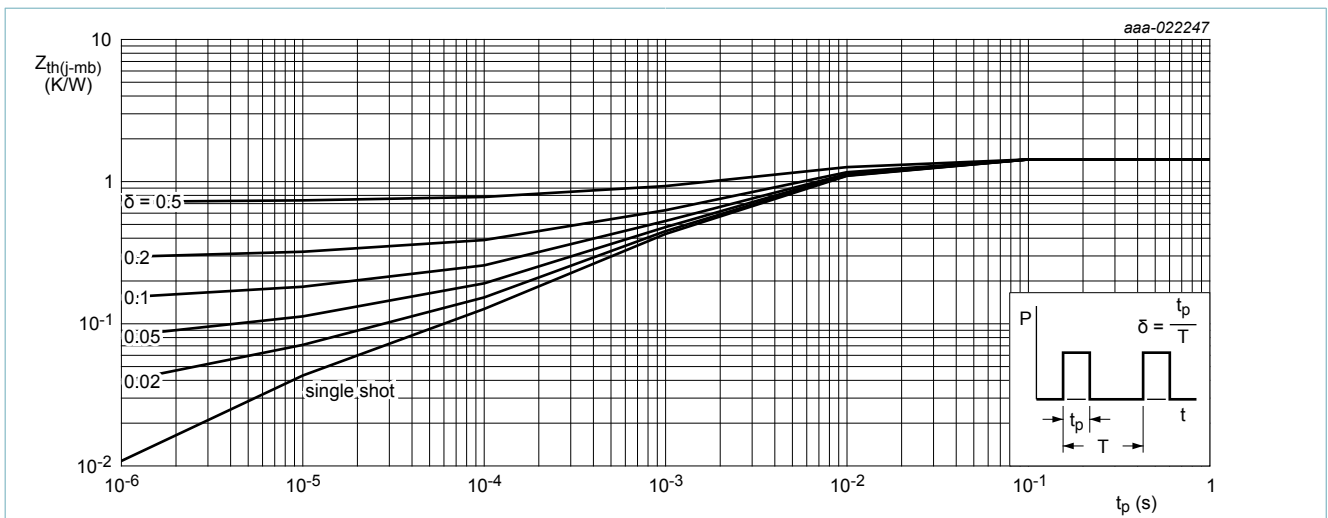


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

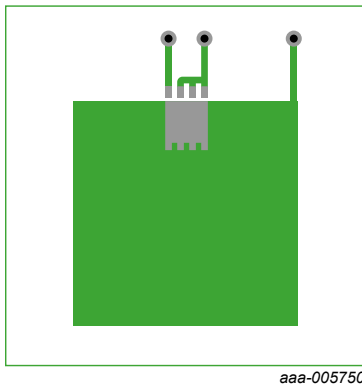


Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

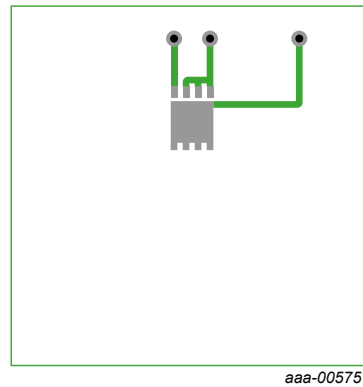


Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

10. Characteristics

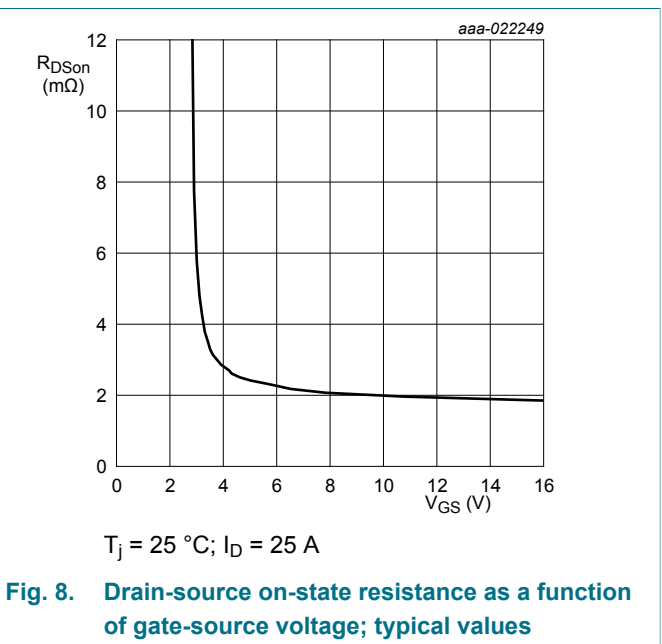
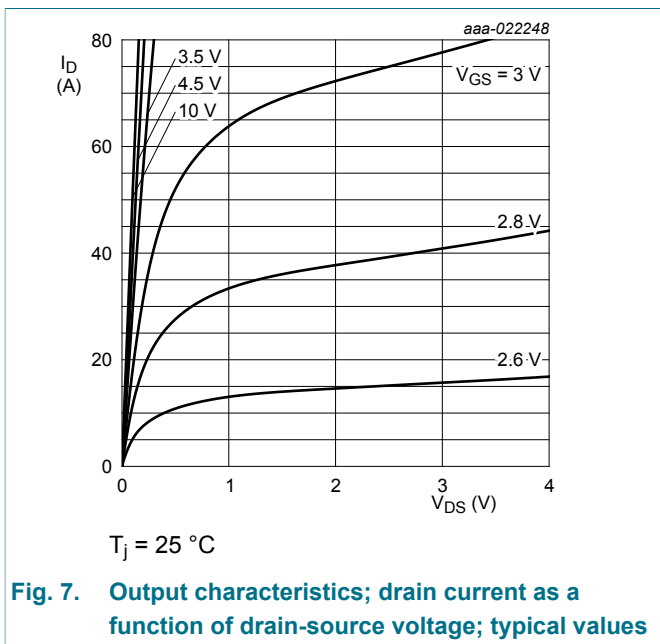
Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--|---|------|-------|------|---------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | 25 | - | - | V |
| | | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$ | 22.5 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$ | 1.2 | 1.68 | 2.2 | V |
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | $25 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C}$ | - | -4.5 | - | mV/K |
| I_{DSS} | drain leakage current | $V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | - | 1 | μA |
| | | $V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$ | - | 3.9 | - | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | - | 100 | nA |
| | | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | - | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 10 | - | 2.41 | 2.91 | mΩ |
| | | $V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 10; Fig. 11 | - | - | 4.95 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 10 | - | 1.82 | 2.09 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 10; Fig. 11 | - | - | 3.52 | mΩ |
| R_G | gate resistance | $f = 1 \text{ MHz}$ | - | 0.849 | - | Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 12; Fig. 13 | - | 34.1 | - | nC |
| | | $I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 12; Fig. 13 | - | 15.7 | - | nC |
| | | $I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$ | - | 15.2 | - | nC |
| Q_{GS} | gate-source charge | $I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 12; Fig. 13 | - | 6.4 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | - | 3.8 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | - | 2.6 | - | nC |
| Q_{GD} | gate-drain charge | | - | 3.6 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D = 25 \text{ A}; V_{DS} = 12 \text{ V};$ Fig. 12; Fig. 13 | - | 2.8 | - | V |

N-channel 25 V, 2.09 mΩ, 140 A logic level MOSFET in LFPAK56 using NextPowerS3 Technology

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|------------------------------|--|-----|------|-----|------|
| C_{iss} | input capacitance | $V_{DS} = 12\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ Fig. 14 | - | 2485 | - | pF |
| C_{oss} | output capacitance | | - | 1142 | - | pF |
| C_{rss} | reverse transfer capacitance | | - | 152 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 12\text{ V}; R_L = 0.6\text{ }\Omega; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 5\text{ }\Omega$ | - | 15.7 | - | ns |
| t_r | rise time | | - | 18.7 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 18.7 | - | ns |
| t_f | fall time | | - | 12.4 | - | ns |
| Q_{oss} | output charge | $V_{GS} = 0\text{ V}; V_{DS} = 12\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}$ | - | 23 | - | nC |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 20\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 15 | - | 0.8 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 25\text{ A}; di_S/dt = -100\text{ A/s}; V_{GS} = 0\text{ V}; V_{DS} = 12\text{ V};$ Fig. 16 | - | 26 | - | ns |
| Q_r | recovered charge | | [1] | 16.8 | - | nC |
| t_a | reverse recovery rise time | | - | 13 | - | ns |
| t_b | reverse recovery fall time | | - | 13 | - | ns |
| S | softness factor | | - | 1 | - | |

[1] Includes capacitive recovery



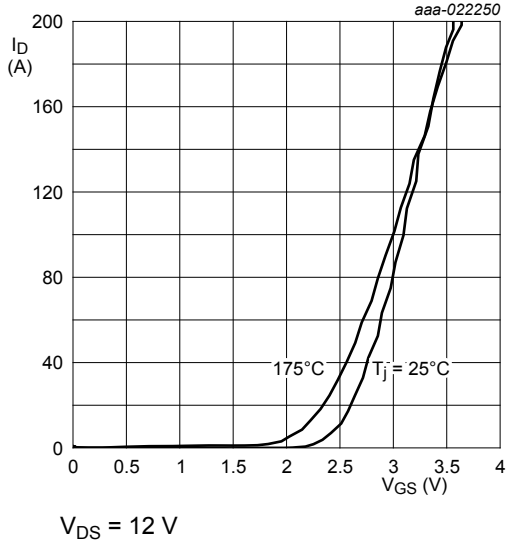


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

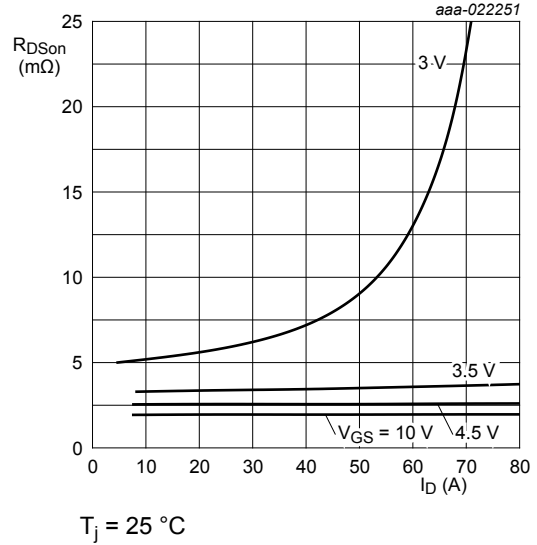


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

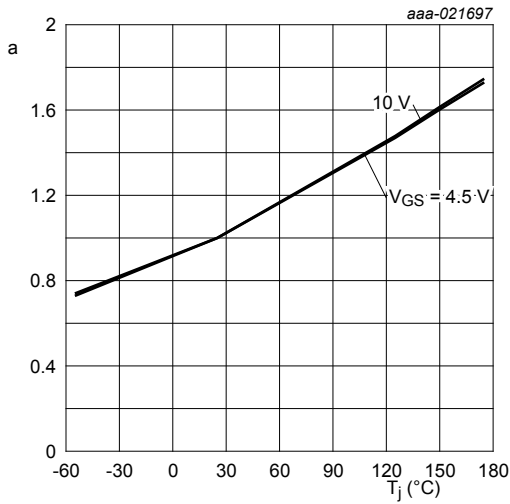


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

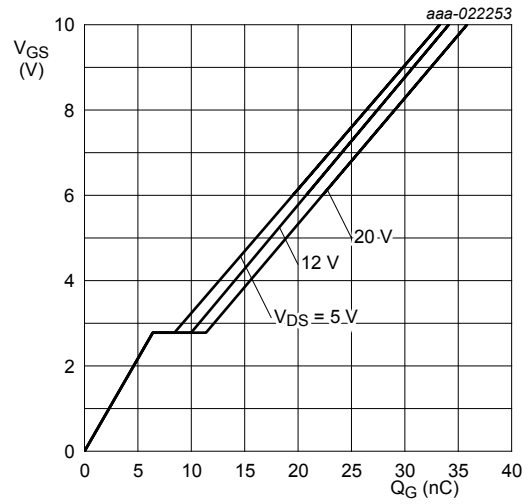


Fig. 12. Gate-source voltage as a function of gate charge; typical values

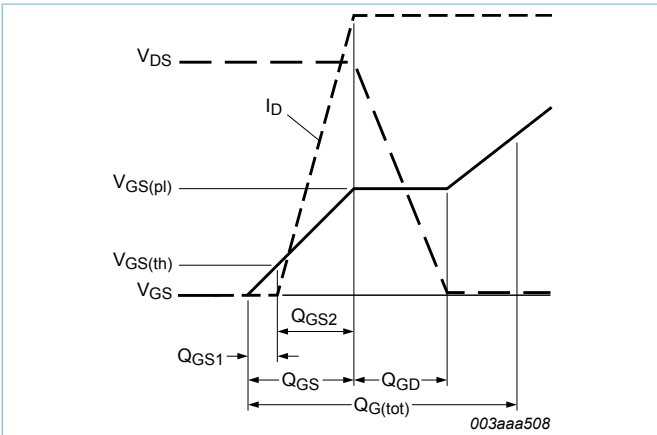
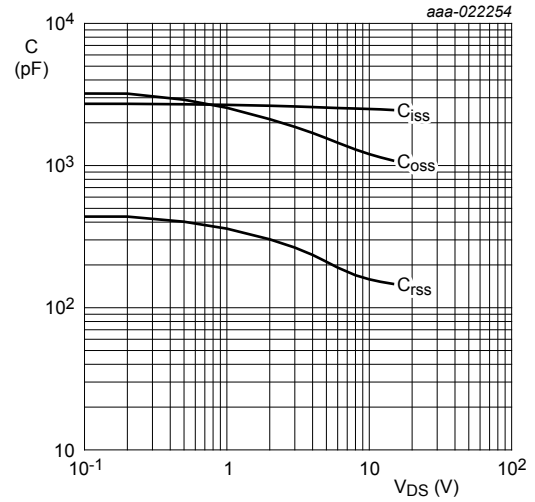
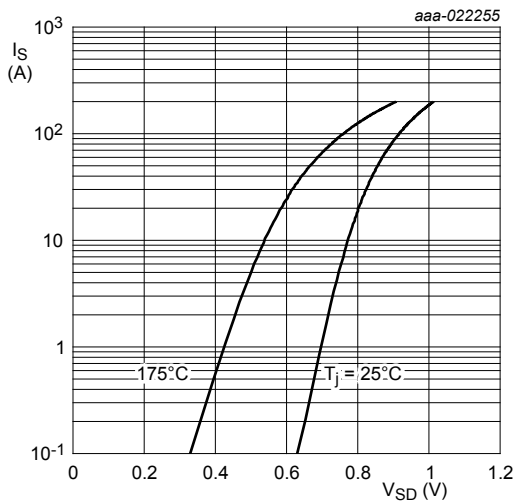


Fig. 13. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0 \text{ V}$

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

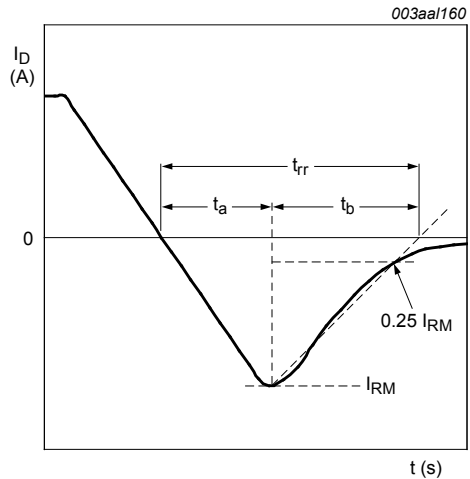
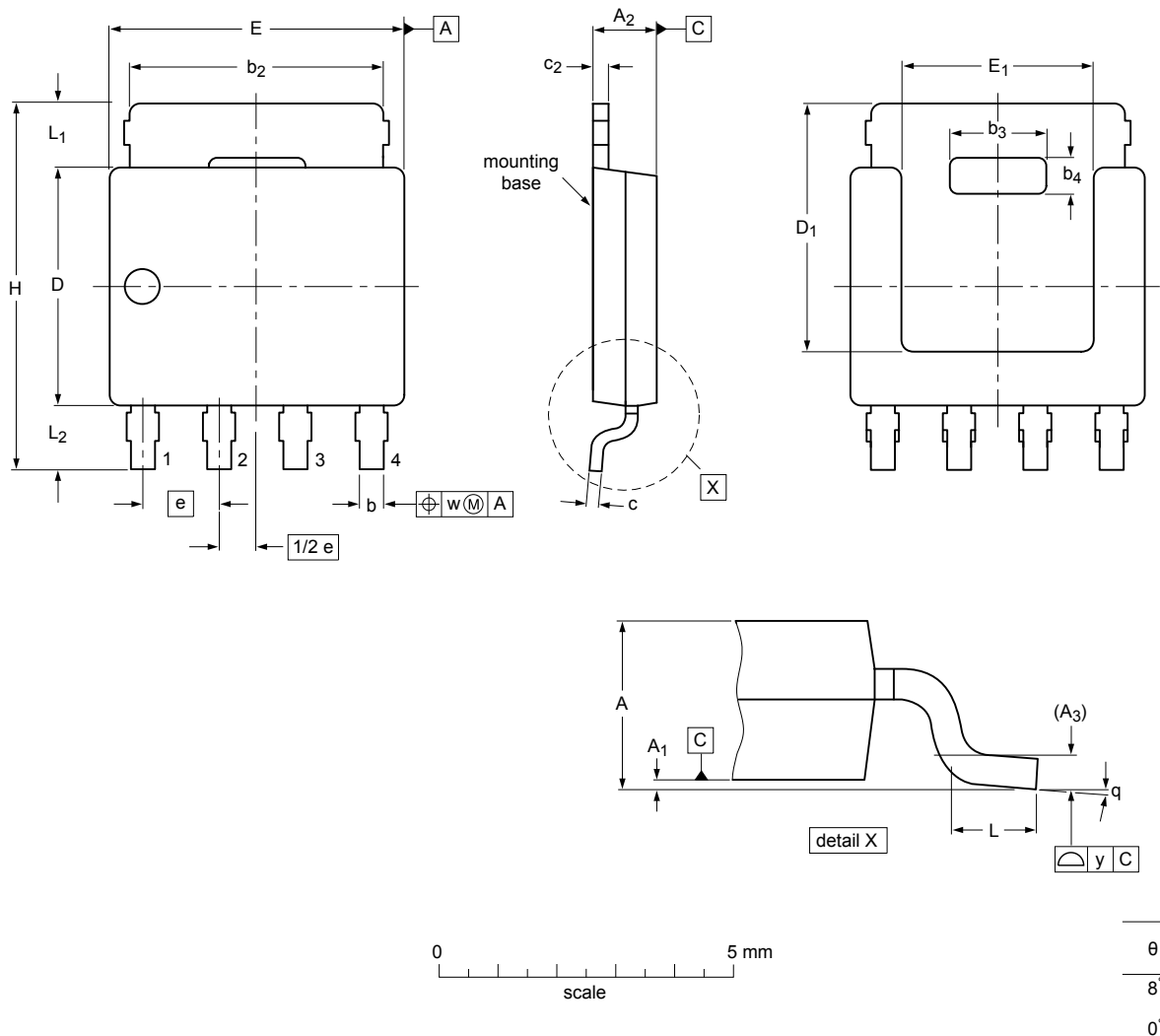


Fig. 16. Reverse recovery timing definition

11. Package outline

Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

| Unit ⁽¹⁾ | A | A ₁ | A ₂ | A ₃ | b | b ₂ | b ₃ | b ₄ | c | c ₂ | D ⁽¹⁾ | D ₁ ⁽¹⁾ | E ⁽¹⁾ | E ₁ ⁽¹⁾ | e | H | L | L ₁ | L ₂ | w | y |
|---------------------|------|----------------|----------------|----------------|------|----------------|----------------|----------------|------|----------------|------------------|-------------------------------|------------------|-------------------------------|------|-----|------|----------------|----------------|------|-----|
| max | 1.20 | 0.15 | 1.10 | | 0.50 | 4.41 | 2.2 | 0.9 | 0.25 | 0.30 | 4.10 | 4.20 | 5.0 | 3.3 | | 6.2 | 0.85 | 1.3 | 1.3 | | |
| nom | | | | 0.25 | | | | | | | | | | | 1.27 | | | | | 0.25 | 0.1 |
| min | 1.01 | 0.00 | 0.95 | | 0.35 | 3.62 | 2.0 | 0.7 | 0.19 | 0.24 | 3.80 | | 4.8 | 3.1 | | 5.8 | 0.40 | 0.8 | 0.8 | | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

| Outline version | References | | | | European projection | Issue date |
|-----------------|------------|--------|-------|--|---------------------|------------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT669 | | MO-235 | | | | -11-03-25- 13-02-27 |

Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

12.1 Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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