

# PSMN5R2-60YL

N-channel 60 V, 5.2 mΩ logic level MOSFET in LFPAK56

3 June 2016

Product data sheet

## 1. General description

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product is designed and qualified for use in a wide range of power supply & motor control equipment.

#### 2. Features and benefits

- Advanced TrenchMOS provides low R<sub>DSon</sub> and low gate charge
- · Logic level gate operation
- Avalanche rated, 100% tested
- LFPAK provides maximum power density in a Power SO8 package

## 3. Applications

- · Synchronous rectifier in LLC topology
- Chargers & adaptors with V<sub>out</sub> < 10 V</li>
- Fast charge & USB-PD applications
- Battery powered motor control
- LED lighting & TV backlight

#### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	60	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	[1]	-	-	100	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	195	W
Static characte	eristics						
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}; Fig. 11$		-	4.6	6	mΩ
Dynamic characteristics							
$Q_{GD}$	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 5 V; Fig. 13; Fig. 14		-	11.1	-	nC

<sup>[1]</sup> Continuous current is limited by package.



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## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D I
2	S	source		
3	S	source	[q]j	G 4
4	G	gate	وققق	mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

## 6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PSMN5R2-60YL	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669		

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	60	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$		-	60	V
$V_{GS}$	gate-source voltage			-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	195	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	[1]	-	100	Α
		V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 100 °C; <u>Fig. 2</u>		-	85	Α
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$ ; Fig. 3		-	479	Α
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
Source-drain diode						
Is	source current	T <sub>mb</sub> = 25 °C	[1]	-	100	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	479	Α

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### N-channel 60 V, 5.2 mΩ logic level MOSFET in LFPAK56

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche rug	gedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 100 A; $V_{sup} \le$ 60 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[2][3]	-	127	mJ

- [1]
- Continuous current is limited by package. Single-pulse avalanche rating limited by maximum junction temperature of 175  $^{\circ}\text{C}.$
- Refer to application note AN10273 for further information.

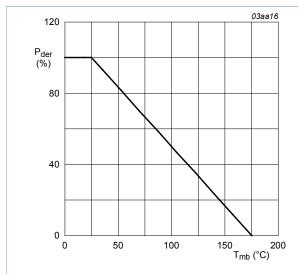
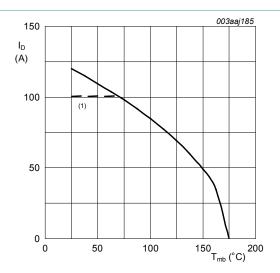


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

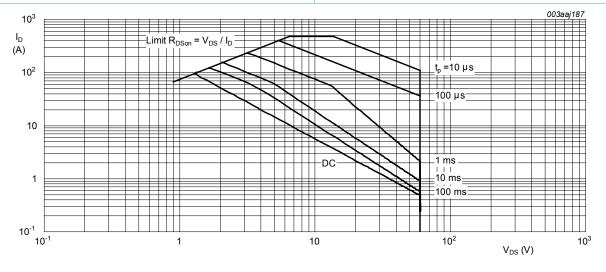
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$



(1) Capped at 100A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 5V$$



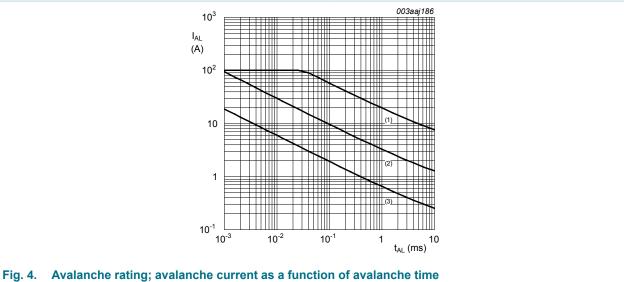
Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb}$  = 25°C;  $I_{DM}$  is a single pulse

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#### rig. 4. Avaianche fathig, avaianche current as a function of avaianche time

(1) 
$$T_{j(init)} = 25$$
°C; (2)  $T_{j(init)} = 150$ °C; (3) Repetitive Avalanche

#### 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 5	-	-	0.77	K/W

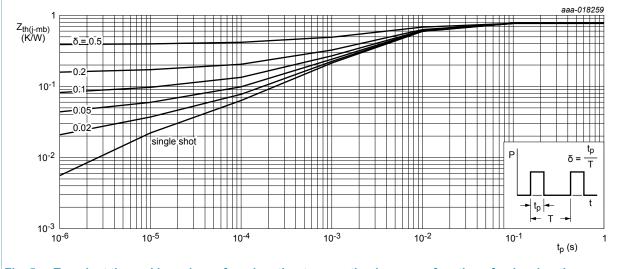


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

## 9. Characteristics

Table 6. Characteristics

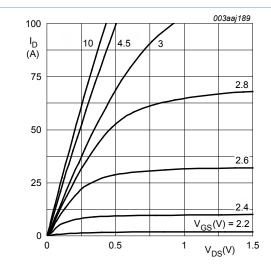
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		'			
V <sub>(BR)DSS</sub>	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	60	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^{\circ}C$	54	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}; Fig. 9;$ Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}; Fig. 9$	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C}; Fig. 9$	0.5	-	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 60 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μA
		V <sub>DS</sub> = 60 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.07	10	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 11$	-	4.6	6	mΩ
resistance	resistance	$V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 11	-	4	5.2	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; Fig. 11; Fig. 12	-	-	13.6	mΩ
Dynamic cl	naracteristics					
Q <sub>G(tot)</sub> to	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 5 V; Fig. 13; Fig. 14	-	39.4	-	nC
		I <sub>D</sub> = 25 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 10 V; Fig. 13; Fig. 14	-	78.4	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 5 V;	-	12.3	-	nC
$Q_{GD}$	gate-drain charge	Fig. 13; Fig. 14	-	11.1	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz;	-	4739	6319	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 15</u>	-	391	469	pF
C <sub>rss</sub>	reverse transfer capacitance		-	202	277	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = 45 V; $R_L$ = 1.8 $\Omega$ ; $V_{GS}$ = 5 V;	-	24	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega$	-	44	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	60	-	ns
t <sub>f</sub>	fall time		-	37	-	ns
Source-dra	in diode		1	-	-	
$V_{SD}$	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <u>Fig. 16</u>	-	0.8	1.2	V

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t <sub>rr</sub>	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	_	26	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 25 V	-	23	-	nC



 $T_i = 25 \, ^{\circ}\text{C}; t_p = 300 \, \mu\text{s}$ 

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

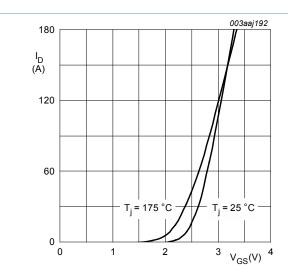


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



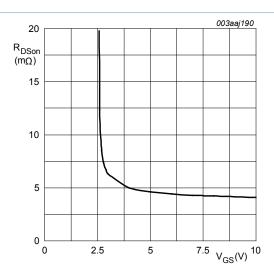


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_i = 25^{\circ}C; I_D = 25A$$

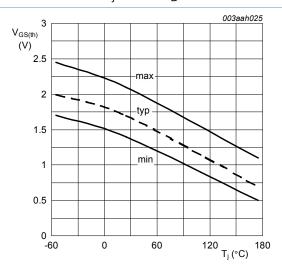


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D$$
 = 1 mA;  $V_{DS}$  =  $V_{GS}$ 

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### N-channel 60 V, 5.2 m $\Omega$ logic level MOSFET in LFPAK56

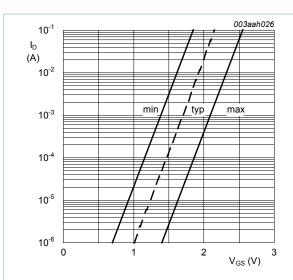


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_i = 25$$
°C;  $V_{DS} = 5V$ 

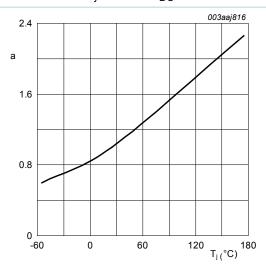
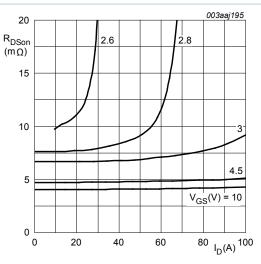


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}C)}$$



 $T_j = 25 \, ^{\circ}C; t_p = 300 \, \mu s$ 

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

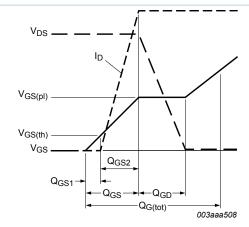


Fig. 13. Gate charge waveform definitions

### N-channel 60 V, 5.2 m $\Omega$ logic level MOSFET in LFPAK56

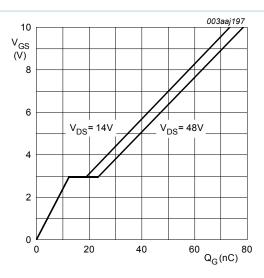


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_i = 25^{\circ}C; I_D = 25A$$

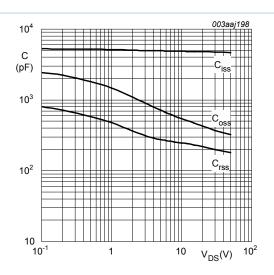


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V$$
;  $f = 1MHz$ 

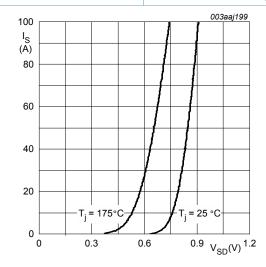


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

## 10. Package outline

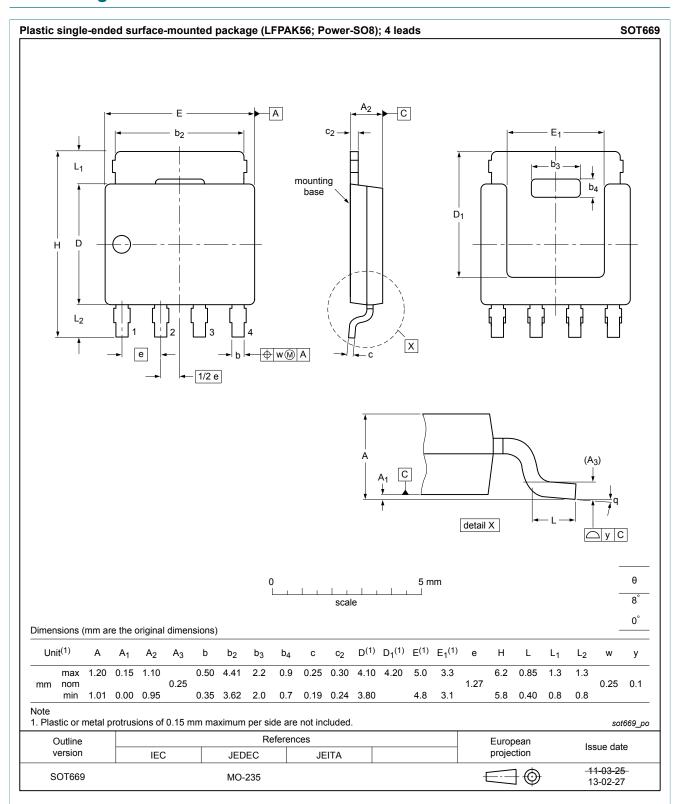


Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)

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