



PSMNR60-25YLH

N-channel 25 V, 0.7 mΩ, 300 A logic level MOSFET in LFPAK56 using NextPowerS3 technology

30 September 2019

Product data sheet

1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFPAK56 package optimized for low R_{DSon} . Low I_{DSS} leakage even when hot, high efficiency and high current. Rated to 300 A, optimized for DC load switch and hot-swap applications.

2. Features and benefits

- 100% avalanche tested at $I_{(AS)} = 190$ A
- Optimized for low R_{DSon}
- Low leakage $< 1 \mu A$ at 25 °C
- Low spiking and ringing for low EMI designs
- Optimized for 4.5 V gate drive
- Copper-clip for low parasitic inductance and resistance
- High reliability LFPAK package, qualified to 175 °C
- Wave solderable; exposed leads for optimal solder coverage and visual solder inspection

3. Applications

- Hot swap
- e-Fuse
- Power OR-ing
- DC switch / Load switch
- Battery protection
- Brushed and BLDC (brushless) motor control
- Synchronous rectification in AC-DC and DC-DC applications

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25 \text{ °C} \leq T_j \leq 175 \text{ °C}$	-	-	25	V
I_D	drain current	$V_{GS} = 10 \text{ V}$; $T_{mb} = 25 \text{ °C}$; Fig. 2	[1]	-	300	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ °C}$; Fig. 1	-	-	268	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 25 \text{ °C}$; Fig. 10	-	0.59	0.7	mΩ
		$V_{GS} = 4.5 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 25 \text{ °C}$; Fig. 10	-	0.82	1.02	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25 \text{ A}$; $V_{DS} = 12 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; Fig. 12 ; Fig. 13	2.7	15	30	nC
$Q_{G(tot)}$	total gate charge		19	43	71	nC

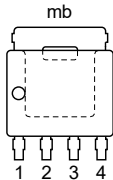
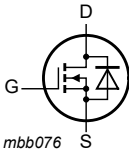
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
S	softness factor	$I_S = 25$ A; $di_S/dt = -100$ A/ μ s; $V_{GS} = 0$ V; $V_{DS} = 12$ V; Fig. 16	-	1	-	

[1] 300A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR60-25YLH	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR60-25YLH	H6025L

8. Limiting values

Table 5. Limiting values

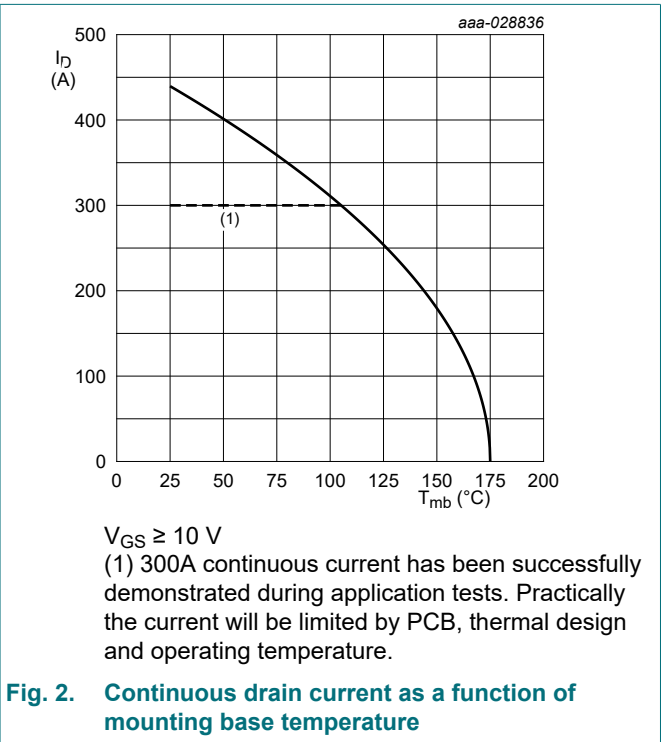
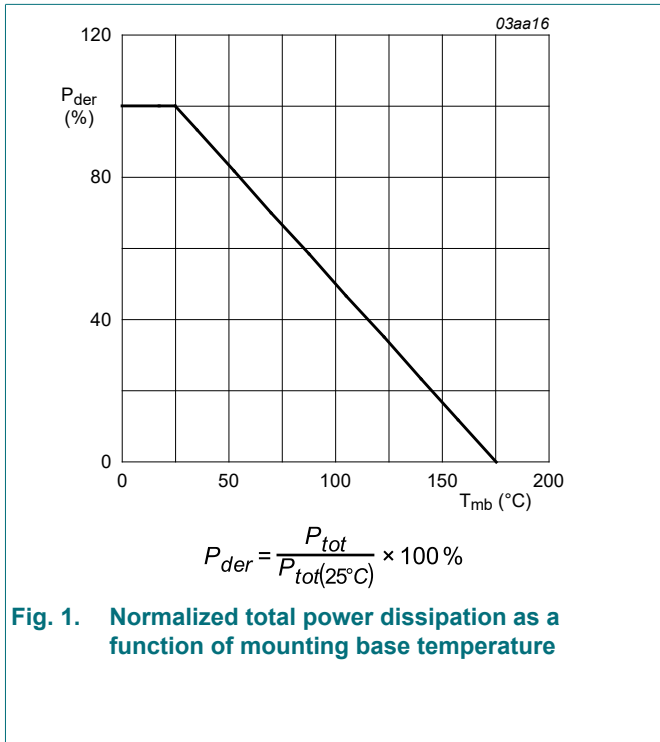
In accordance with the Absolute Maximum Rating System (IEC 60134).

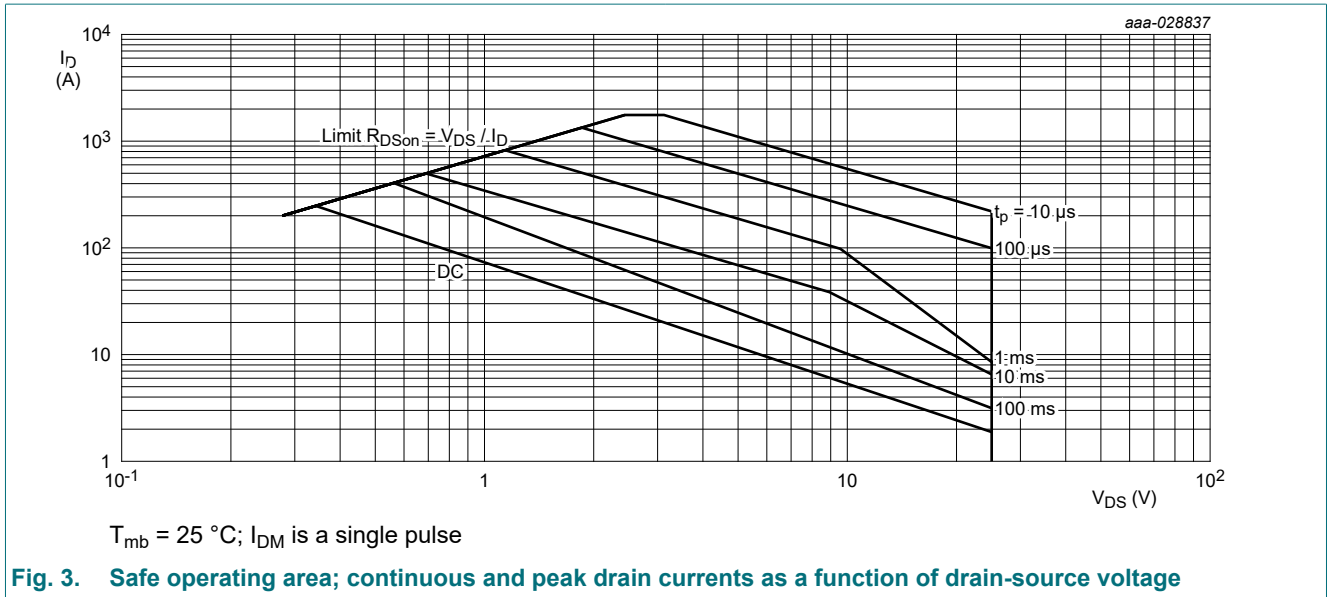
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	-	25	V
V_{DGR}	drain-gate voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 1	-	268	W
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 2	[1]	300	A
		$V_{GS} = 10$ V; $T_{mb} = 100\text{ }^\circ\text{C}$; Fig. 2		300	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 3	-	1758	A
T_{stg}	storage temperature		-55	175	$^\circ\text{C}$
T_j	junction temperature		-55	175	$^\circ\text{C}$

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Symbol	Parameter	Conditions	Min	Max	Unit
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	268	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	1758	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 25 A; V _{sup} ≤ 25 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 8.09 ms	[2]	-	3.2 J
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 25 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[2]	-	190 A

- [1] 300A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test

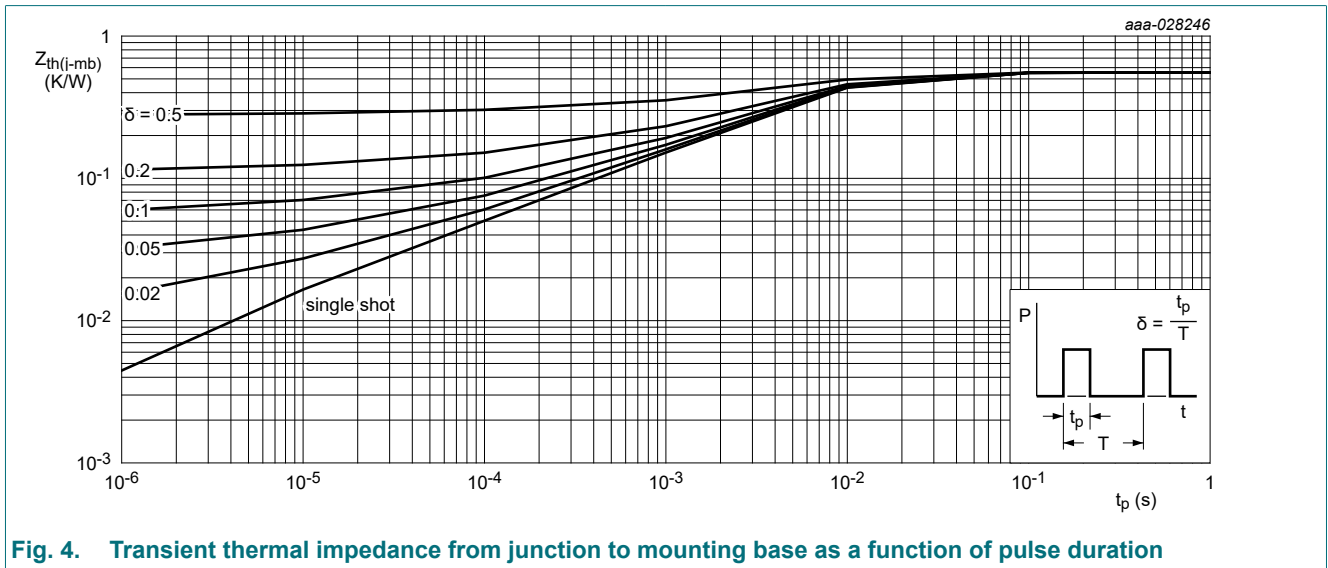




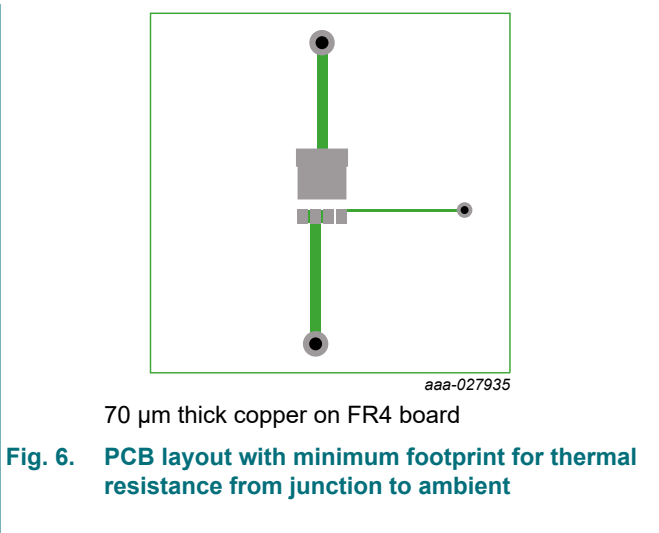
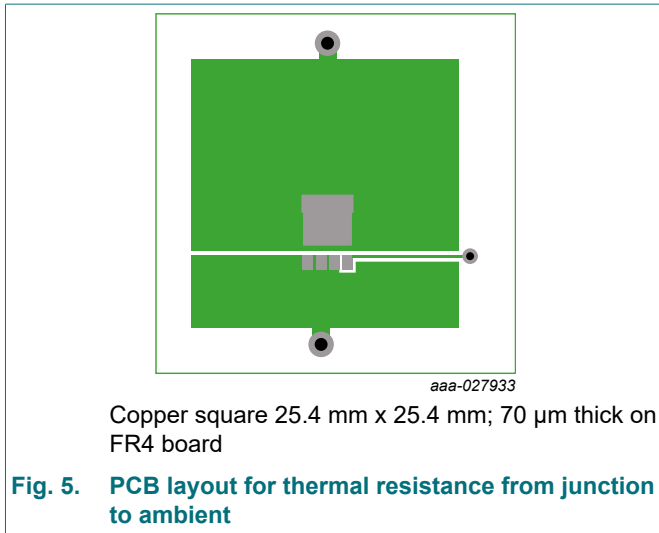
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.48	0.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5 Fig. 6	-	42 85	-	K/W



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10. Characteristics

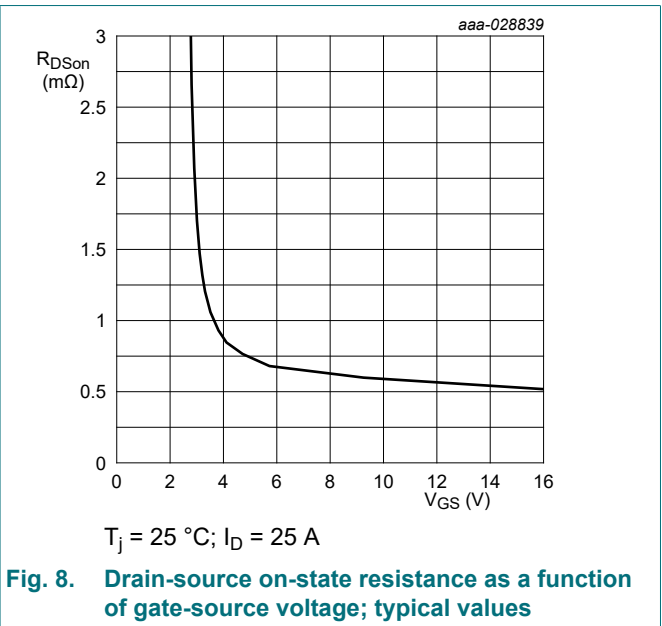
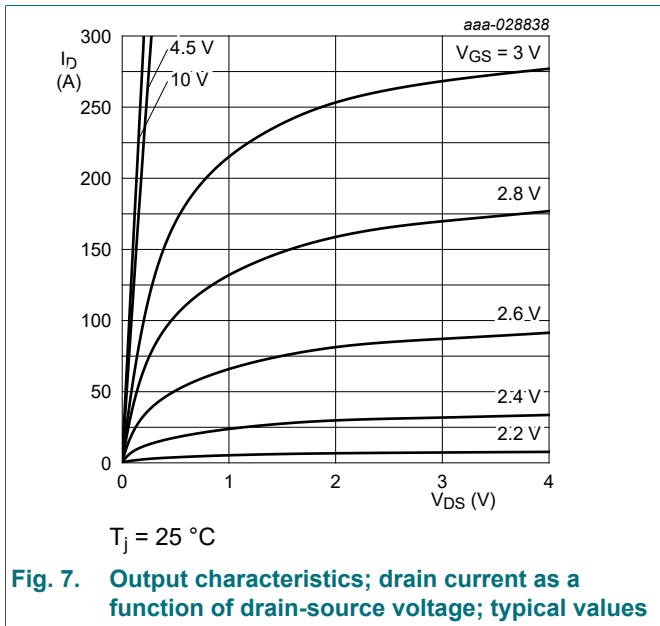
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	25	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 2 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	1.64	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-4.7	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	5.4	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 10	-	0.59	0.7	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ Fig. 11	-	-	1.25	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 10	-	0.82	1.02	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ Fig. 11	-	-	1.82	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.56	1.4	3.5	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 12; Fig. 13	19	43	71	nC
		$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 12; Fig. 13	40	89	147	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	45	-	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Q_{GS}	gate-source charge	$I_D = 25\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 4.5\text{ V};$ Fig. 12 ; Fig. 13	3.2	12	23	nC	
$Q_{GS(th)}$	pre-threshold gate-source charge		2.1	8	15	nC	
$Q_{GS(th-pl)}$	post-threshold gate-source charge		1.1	4.1	7.8	nC	
Q_{GD}	gate-drain charge		2.7	15	30	nC	
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}; V_{DS} = 12\text{ V};$ Fig. 12 ; Fig. 13	-	2.5	-	V	
C_{iss}	input capacitance	$V_{DS} = 12\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14	3247	5411	8117	pF	
C_{oss}	output capacitance		2047	3412	5118	pF	
C_{rss}	reverse transfer capacitance		166	616	1478	pF	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}; R_L = 0.4\text{ }\Omega; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega$	-	32	-	ns	
t_r	rise time		-	61	-	ns	
$t_{d(off)}$	turn-off delay time		-	50	-	ns	
t_f	fall time		-	44	-	ns	
Q_{oss}	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 12\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C}$	-	53	-	nC	
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 15	-	0.76	1	V	
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 12\text{ V};$ Fig. 16	-	42	-	ns	
Q_r	recovered charge		[1]	-	41	-	nC
t_a	reverse recovery rise time		-	-	21	-	ns
t_b	reverse recovery fall time		-	-	21	-	ns
S	softness factor		-	-	1	-	

[1] includes capacitive recovery



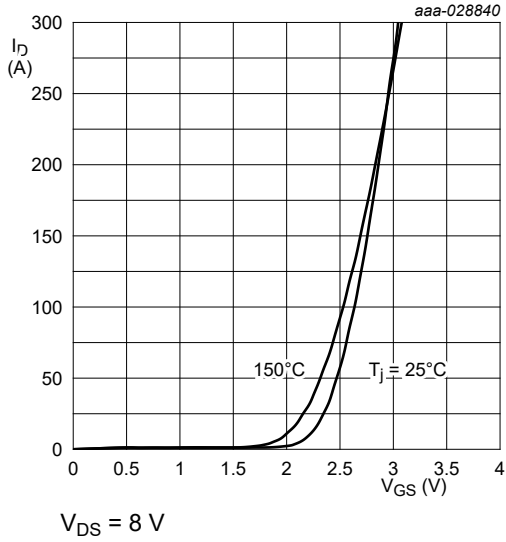


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

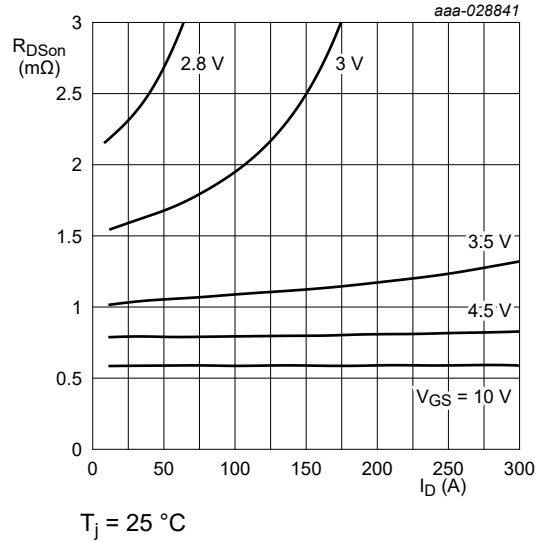
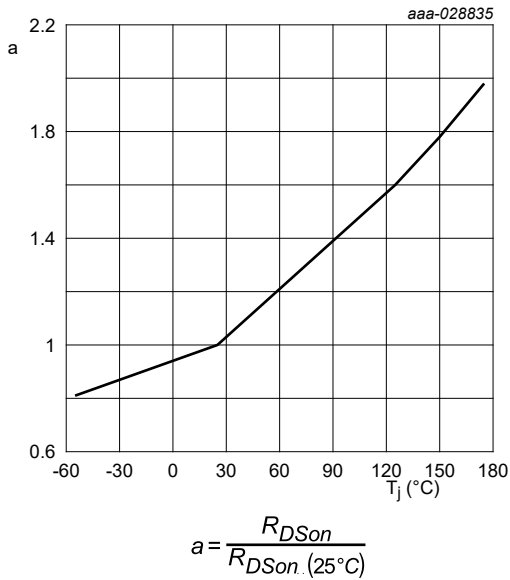


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

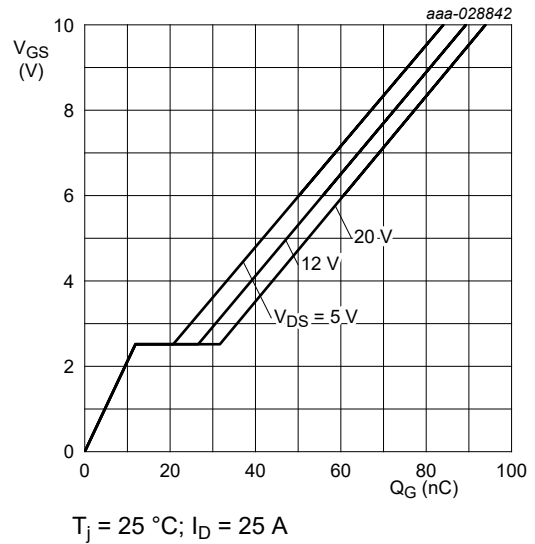


Fig. 12. Gate-source voltage as a function of gate charge; typical values



Fig. 13. Gate charge waveform definitions

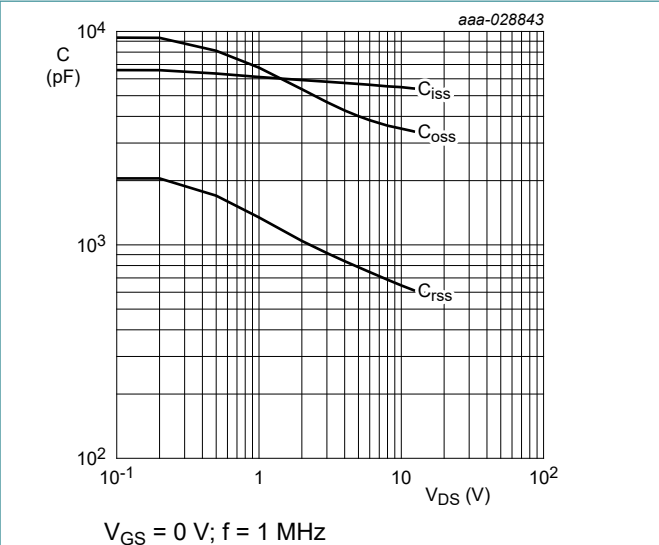


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

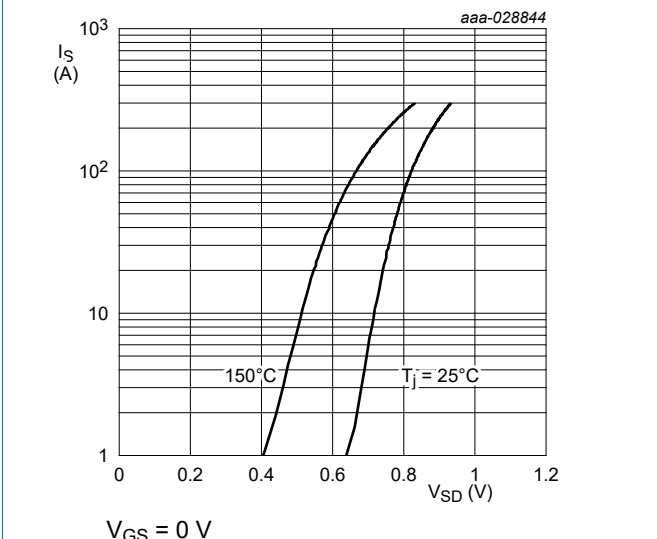


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

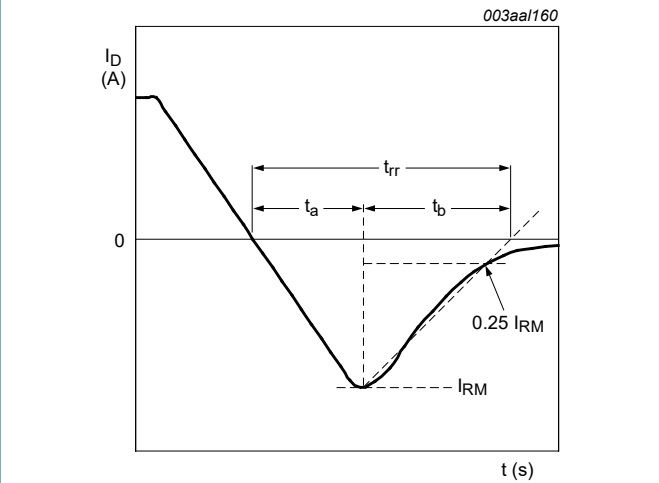


Fig. 16. Reverse recovery timing definition

11. Package outline

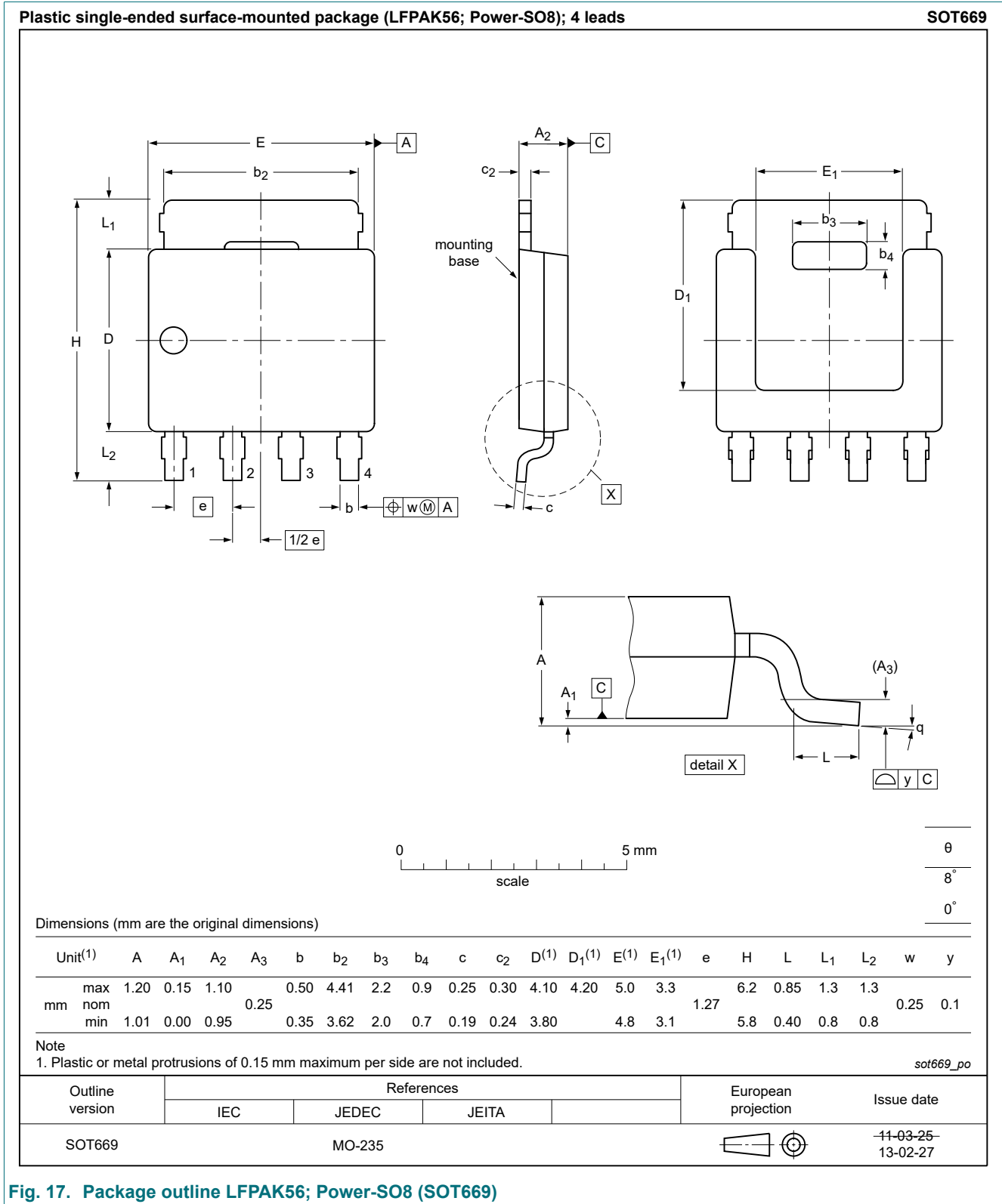


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

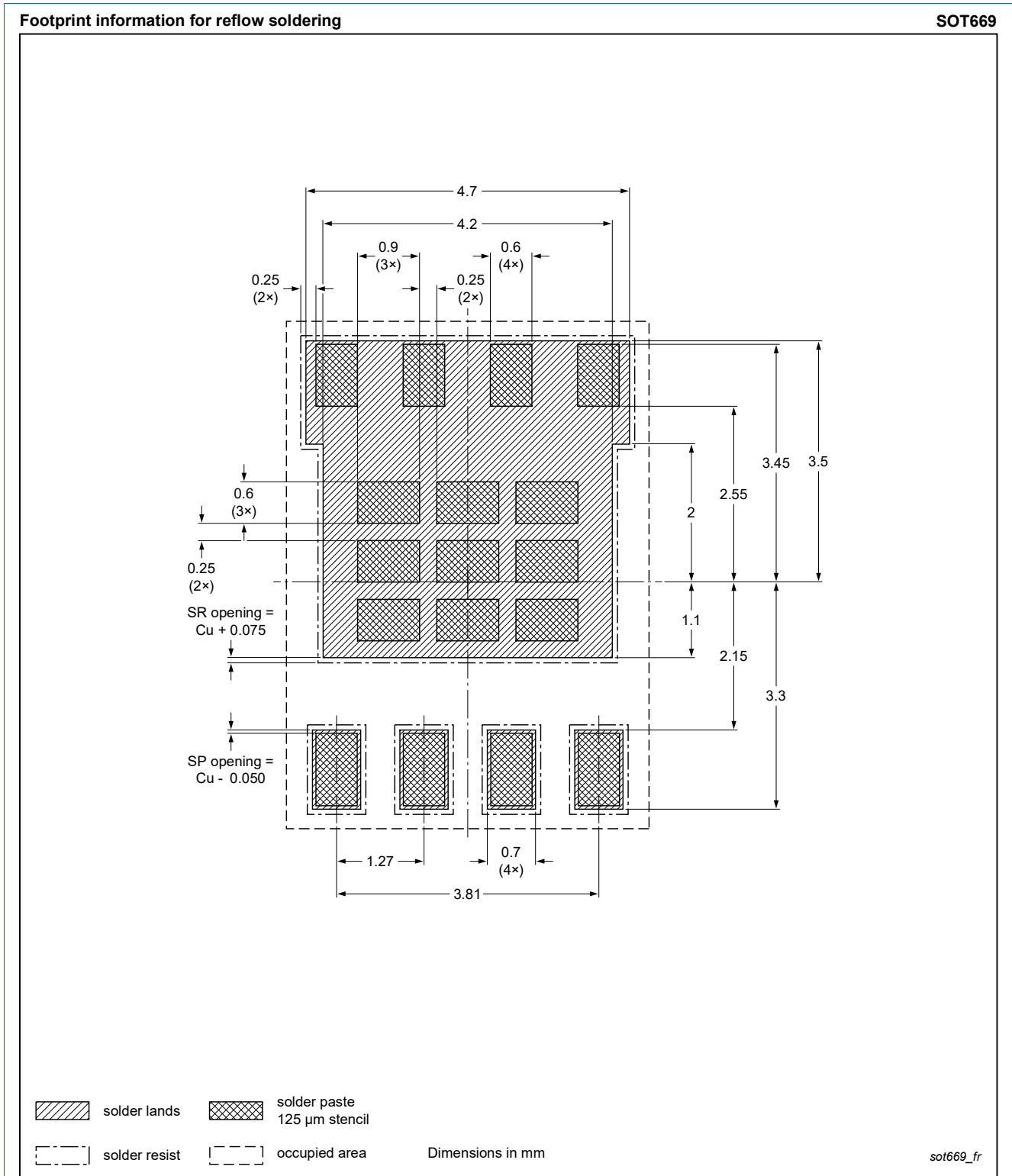
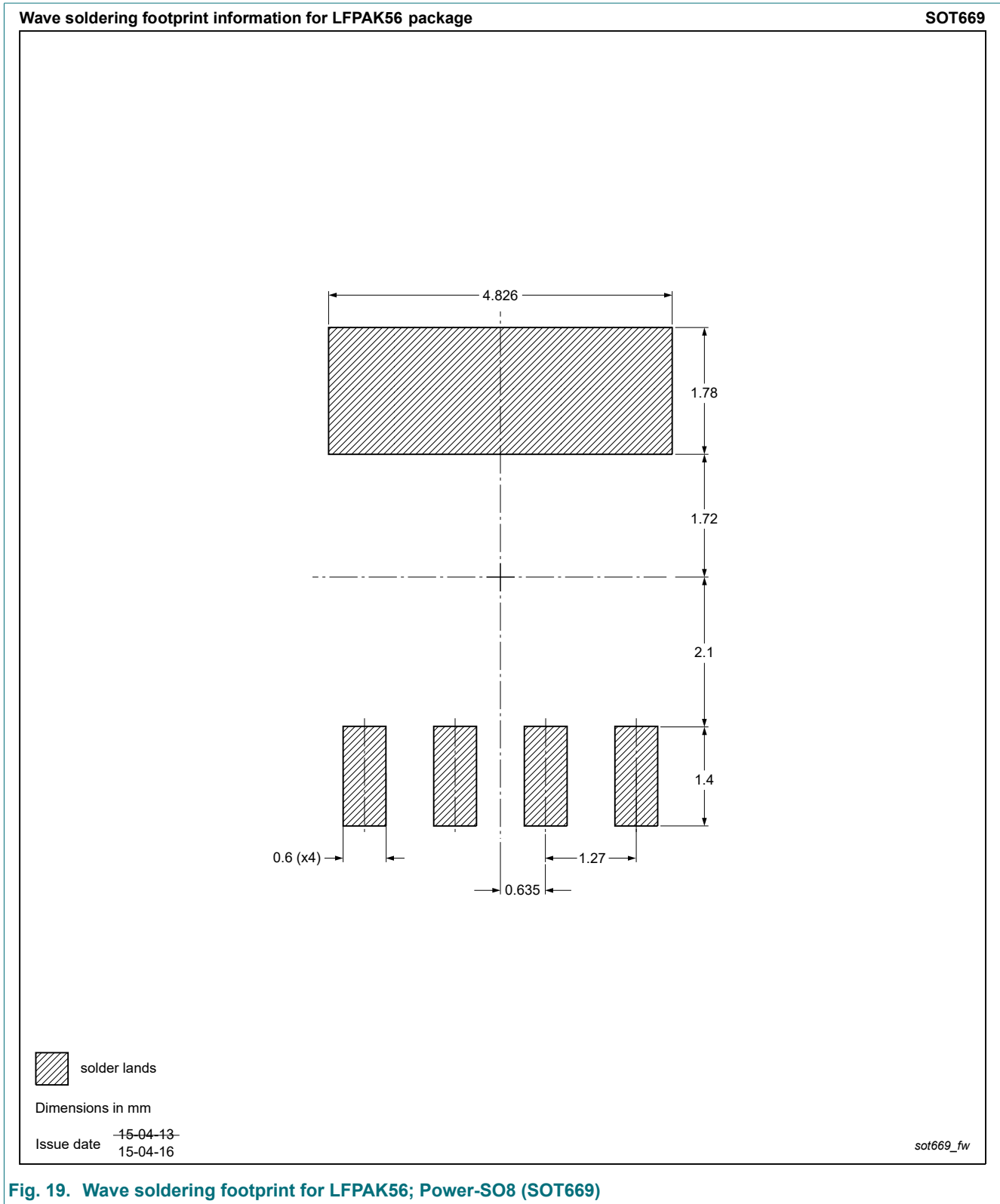


Fig. 18. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)



13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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