



PTVS3V3D1BAL

Ultra compact Transient Voltage Suppressor

26 January 2018

Product data sheet

1. General description

Transient voltage suppressor in a DFN1006-2 (SOD882) ultra small and leadless Surface-Mounted Device (SMD) package designed to protect one line against high surge currents and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- Very high surge robustness; $I_{PP} = 38.3$ A for 8/20 μ s pulse (average measured)
- Very low clamping voltage: $V_{CL} = 10.3$ V typ. for 34 A, 8/20 μ s pulse
- ESD protection up to 30 kV
- Very low dynamical resistance $R_{dyn} = 0.1$ Ω (TLP)
- AEC-Q101 qualified

3. Applications

Surge protection for:

- supply and battery lines
- audio interfaces

in portable communication, consumer and computing devices.

4. Quick reference data

Table 1. Quick reference data


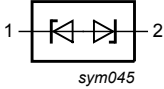
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------|--------------------------|---|-----|-----|------|------|------|
| I_{PPM} | rated peak pulse current | $t_p = 8/20$ μ s | [1] | - | - | 34 | A |
| V_{CL} | clamping voltage | $I_{PPM} = 34$ A; $t_p = 8/20$ μ s; $T_{amb} = 25$ °C | [1] | - | 10.3 | 13.2 | V |
| V_{RWM} | reverse standoff voltage | $T_{amb} = 25$ °C | | - | - | 3.3 | V |

[1] In accordance with IEC 61000-4-5 (8/20 μ s current waveform).

nexperia

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------------|--|---|
| 1 | K1 | cathode (diode 1) |  <p>Transparent top view</p> <p>DFN1006-2 (SOD882)</p> |  <p>sym045</p> |
| 2 | K2 | cathode (diode 2) | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|--------------|-----------|---|---------|
| | Name | Description | Version |
| PTVS3V3D1BAL | DFN1006-2 | plastic, leadless ultra small package; 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.48 mm body | SOD882 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|--------------|--------------|
| PTVS3V3D1BAL | J5 |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|----------------------------|---------------------------------|----------------------------------|-----|-----|-----|------|
| I_{PPM} | rated peak pulse current | $t_p = 8/20 \mu s$ | [1] | - | 34 | A |
| T_j | junction temperature | | | - | 150 | °C |
| T_{amb} | ambient temperature | | | -55 | 150 | °C |
| T_{stg} | storage temperature | | | -65 | 150 | °C |
| ESD maximum ratings | | | | | | |
| V_{ESD} | electrostatic discharge voltage | IEC 61000-4-2; contact discharge | [2] | - | 30 | kV |
| | | IEC 61000-4-2; air discharge | [2] | - | 30 | kV |

[1] In accordance with IEC 61000-4-5 (8/20 μs current waveform).

[2] Device stressed with ten non-repetitive ESD pulses.

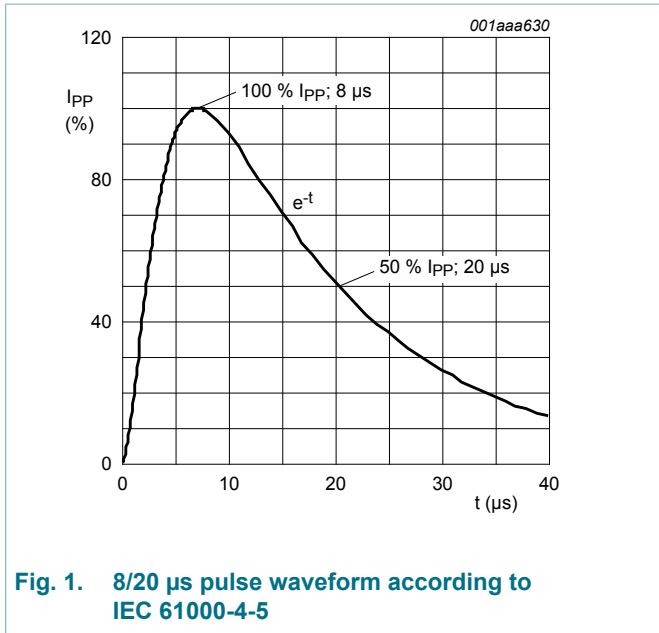


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

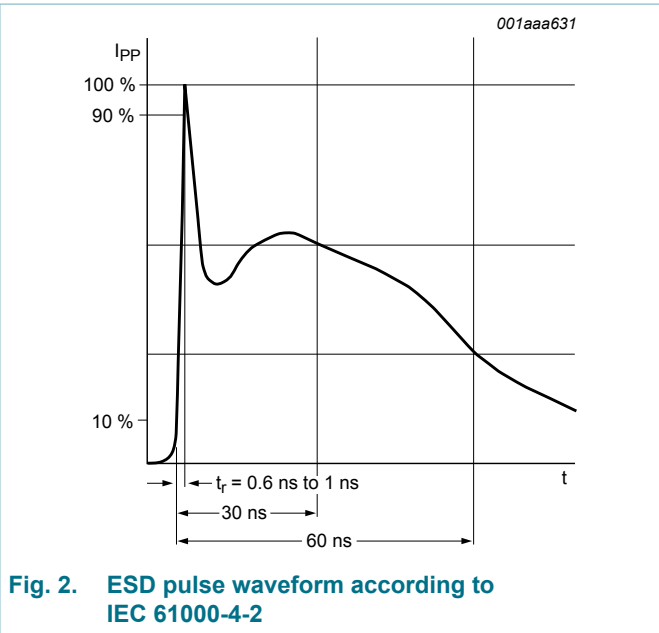


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|--------------------------|---|-----|------|------|------|
| V _{RWM} | reverse standoff voltage | T _{amb} = 25 °C | - | - | 3.3 | V |
| V _{BR} | breakdown voltage | I _R = 1 mA; T _{amb} = 25 °C | 4.5 | - | - | V |
| I _{RM} | reverse leakage current | V _R = 3.3 V; T _{amb} = 25 °C | - | 0.1 | 50 | nA |
| C _d | diode capacitance | f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C | - | 65 | 78 | pF |
| V _{CL} | clamping voltage | I _{PP} = 1 A; t _p = 8/20 μs; T _{amb} = 25 °C | [1] | 5.8 | 9.2 | V |
| | | I _{PPM} = 34 A; t _p = 8/20 μs; T _{amb} = 25 °C | [1] | 10.3 | 13.2 | V |
| | | I _{PP} = 16 A; t _p = TLP; T _{amb} = 25 °C | | 7.5 | - | V |
| R _{dyn} | dynamic resistance | I _R = 10 A; T _{amb} = 25 °C | [2] | 0.1 | - | Ω |

[1] In accordance with IEC 61000-4-5 (8/20 μs current waveform).

[2] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI/ESD STM5.5.1-2008

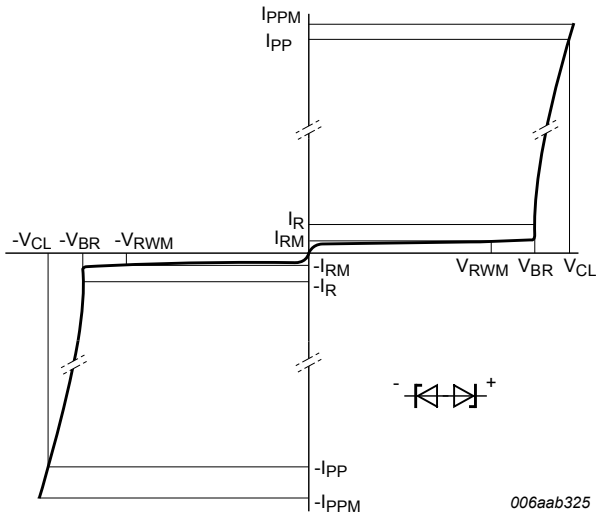


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

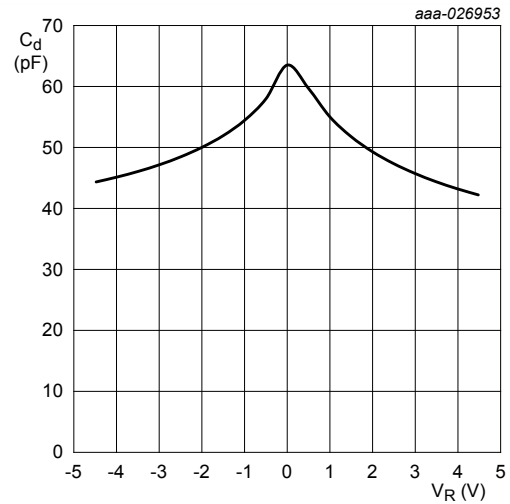


Fig. 4. Diode capacitance as a function of reverse voltage; typical values

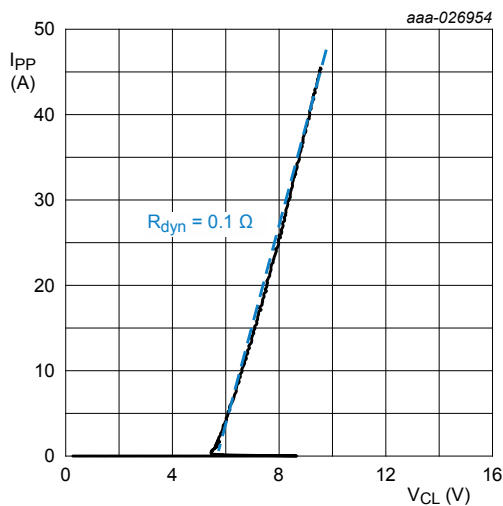


Fig. 5. Positive clamping voltage (TLP); typical values

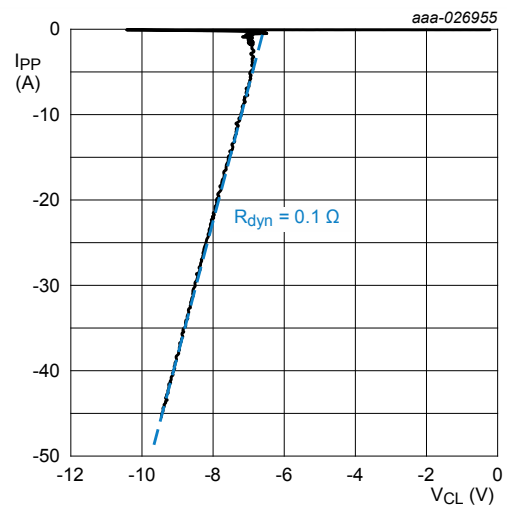


Fig. 6. Negative clamping voltage (TLP); typical values

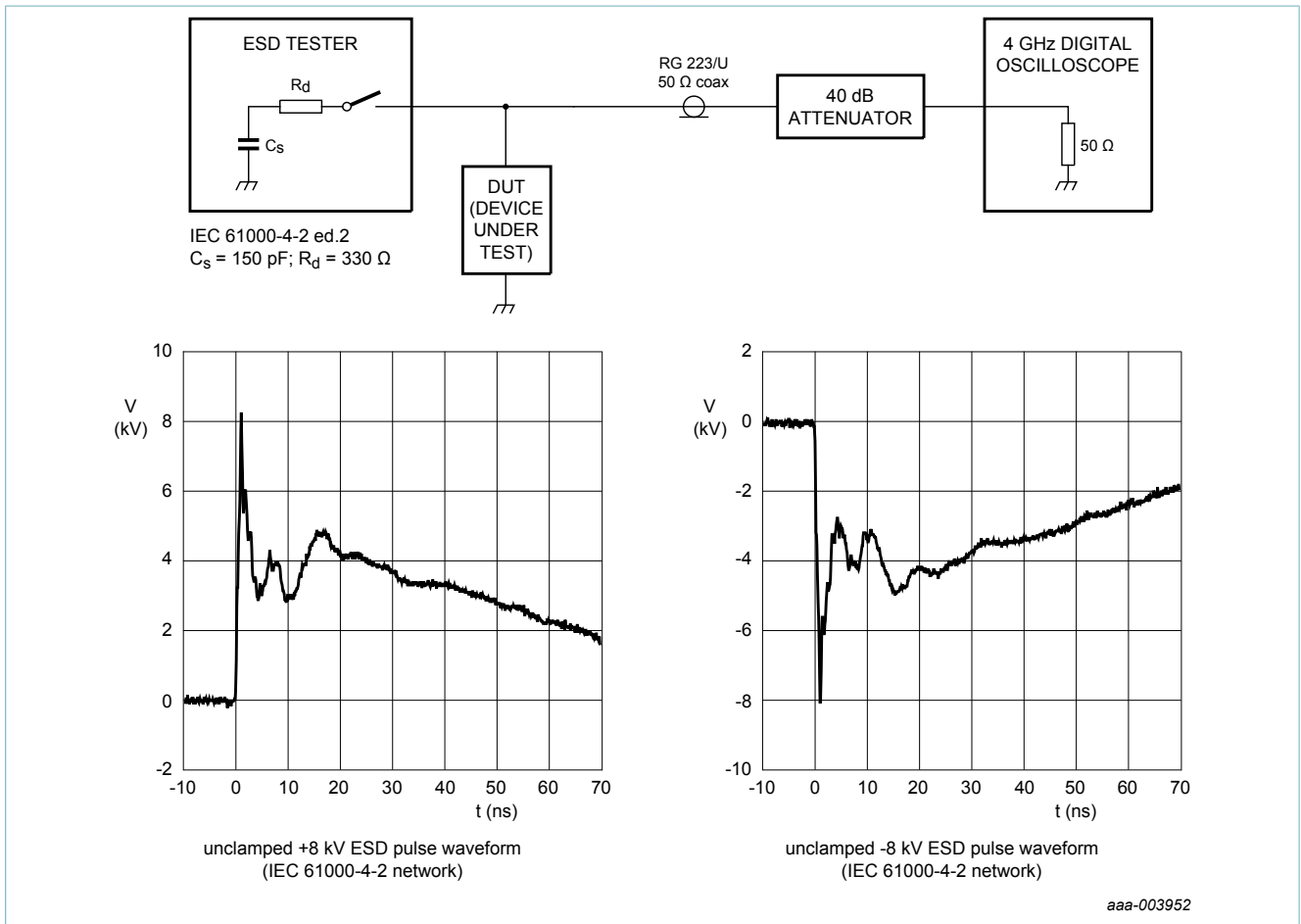
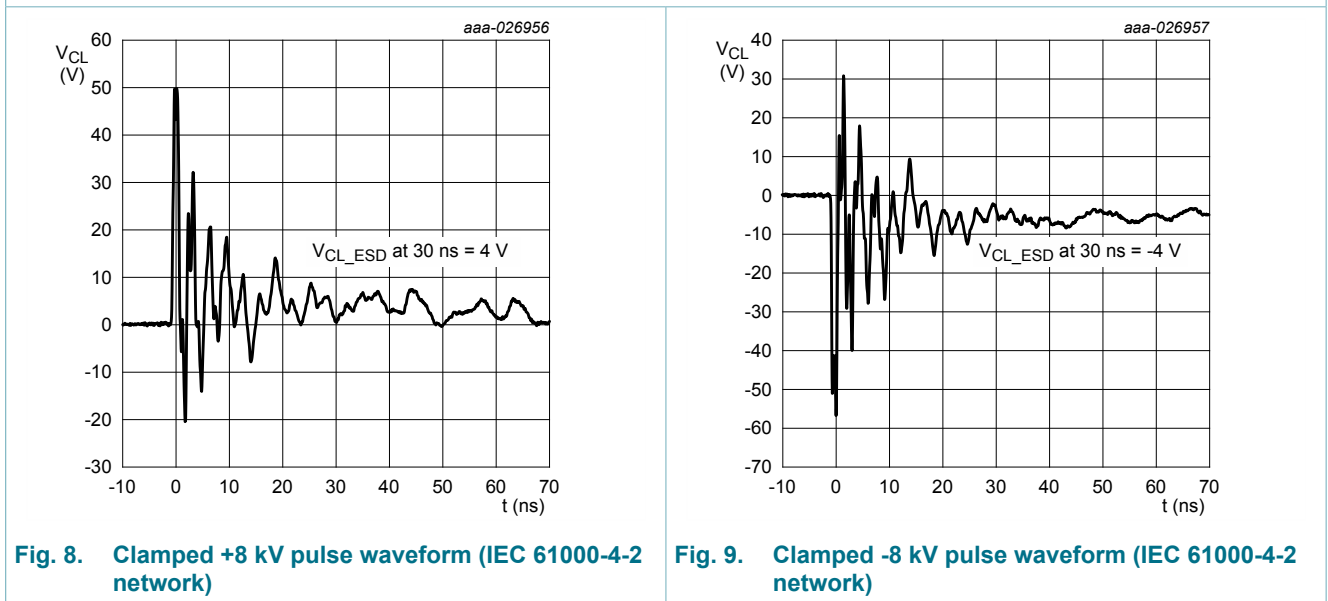


Fig. 7. ESD clamping test setup and waveforms



10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

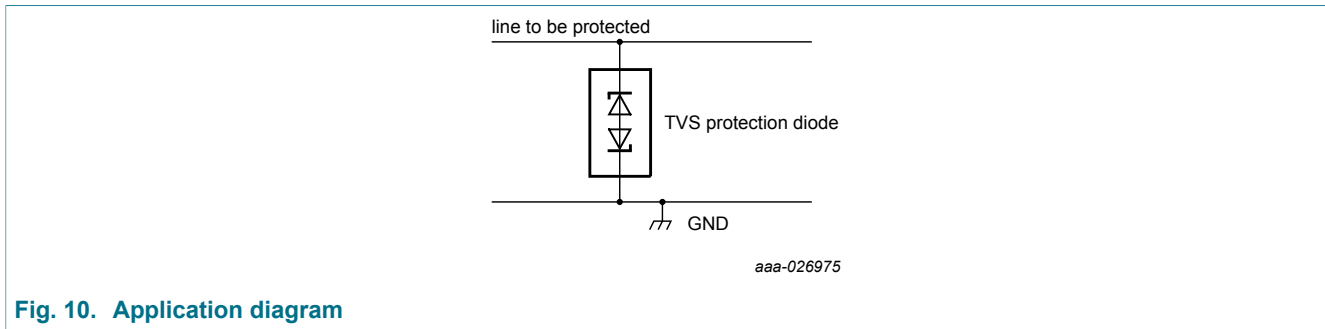


Fig. 10. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

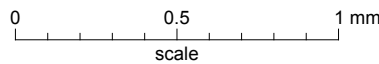
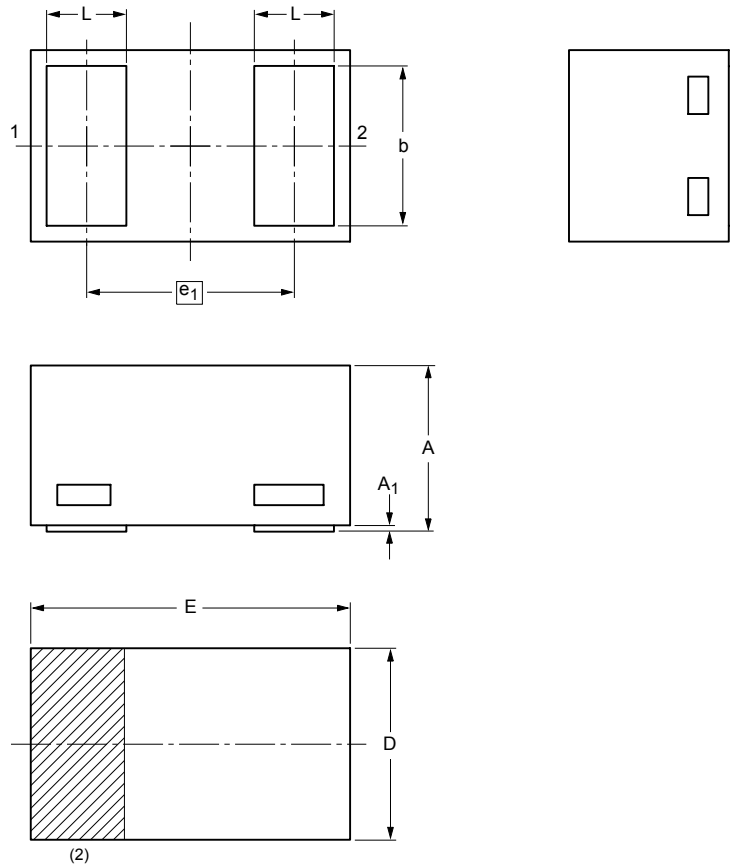
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN1006-2: Leadless ultra small plastic package; 2 terminals; body 1.0 x 0.6 x 0.5 mm

SOD882



Dimensions (mm are the original dimensions)

| Unit | A ⁽¹⁾ | A ₁ | b | D | E | e ₁ | L |
|------|------------------|----------------|------|------|------|----------------|------|
| mm | max 0.50 | 0.03 | 0.55 | 0.62 | 1.02 | | 0.30 |
| | nom | | | | | 0.65 | |
| | min 0.46 | | 0.47 | 0.55 | 0.95 | | 0.22 |

Note

- Including plating thickness
- The marking bar indicates the cathode (if applicable)

sod882_po

| Outline version | References | | | European projection | Issue date |
|-----------------|------------|-------|-------|---------------------|---------------------------------|
| | IEC | JEDEC | JEITA | | |
| SOD882 | | | | | 14-08-26 14-08-27 |

Fig. 11. Package outline DFN1006-2 (SOD882)

13. Soldering

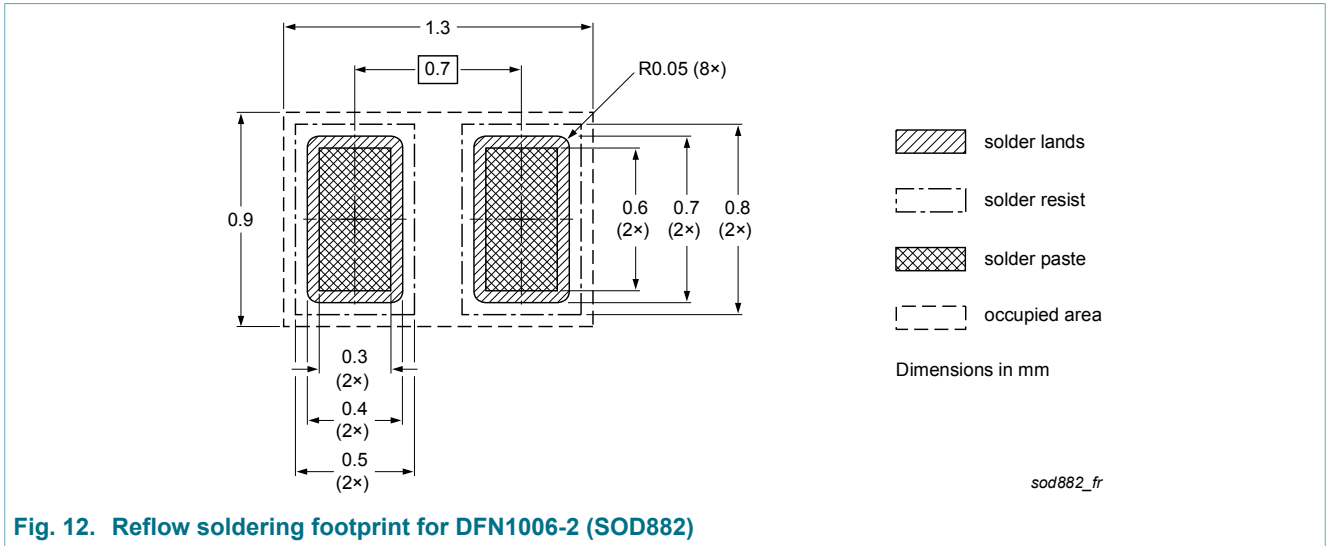


Fig. 12. Reflow soldering footprint for DFN1006-2 (SOD882)

14. Revision history

Table 7. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|--------------|--------------------|---------------|------------|
| PTVS3V3D1BAL v.1 | 20180126 | Product data sheet | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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