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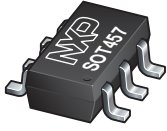
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Kind regards,

Team Nexperia



# PUSB2X4D

## ESD protection for high-speed interfaces

Rev. 1 — 5 November 2013

Product data sheet

## 1. Product profile

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### 1.1 General description

The device is designed to protect high-speed interfaces such as USB 2.0 ports against ElectroStatic Discharge (ESD).

The device includes four high-level ESD protection diode structures for high-speed signal lines. It is encapsulated in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of 0.85 pF maximum. This configuration provides protection to downstream components from ESD voltages up to  $\pm 12$  kV contact according to IEC 61000-4-2, level 4.

### 1.2 Features and benefits

- System ESD protection for USB 2.0
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of  $\pm 12$  kV according to IEC 61000-4-2, level 4
- Line capacitance of 0.85 pF maximum for each channel

### 1.3 Applications

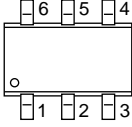
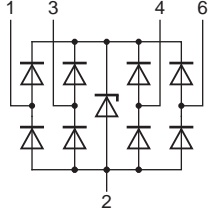
The device is designed for receiver and transmitter port protection in:

- Portable devices
- TVs, monitors
- DVD recorders and players
- Notebooks, mother boards, graphic cards and ports
- Set-top boxes and game consoles



## 2. Pinning information

**Table 1. Pinning**

Pin	Description	Simplified outline	Graphic symbol
1	ESD protection for I/O signals		
2	ground		
3	ESD protection for I/O signals		
4	ESD protection for I/O signals		
5	n.c.		
6	ESD protection for I/O signals		

018aaa176

## 3. Ordering information

**Table 2. Ordering information**

Type number	Package		
	Name	Description	Version
PUSB2X4D	SC-74	plastic surface-mounted package; 6 leads	SOT457

## 4. Marking

**Table 3. Marking codes**

Type number	Marking code
PUSB2X4D	DE

## 5. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_I$	input voltage		-0.5	+5.5	V
$V_{ESD}$	electrostatic discharge voltage	pins 1, 3, 4 and 6 to ground; IEC 61000-4-2, level 4			
		contact discharge	-12	+12	kV
		air discharge	-15	+15	kV
$T_{amb}$	ambient temperature		-40	+85	°C
$T_{stg}$	storage temperature		-55	+125	°C

## 6. Characteristics

**Table 5. Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{BR}$	breakdown voltage	$I_I = 1\text{ mA}$	6	-	9	V
$I_{RM}$	reverse leakage current	per channel; $V_I = 5\text{ V}$	-	-	1	$\mu\text{A}$
$V_F$	forward voltage	$I_I = 1\text{ mA}$	-	0.7	-	V
$C_{line}$	line capacitance	$f = 1\text{ MHz}$	[1]			
		$V_I = 0\text{ V}$	-	0.7	0.85	pF
		$V_I = 2.5\text{ V}$	-	0.6	0.75	pF
$\Delta C_{line}$	line capacitance difference	$f = 1\text{ MHz}; V_I = 2.5\text{ V}$	[1]	-	0.1	pF
$r_{dyn}$	dynamic resistance	surge	[2]			
		positive transient	-	0.41	-	$\Omega$
		negative transient	-	0.34	-	$\Omega$
		TLP	[3]			
		positive transient	-	0.48	-	$\Omega$
		negative transient	-	0.34	-	$\Omega$
$V_{CL}$	clamping voltage	positive transient	[2]			
		$I_{PP} = 4.8\text{ A}$	-	4.3	-	V
		negative transient				
		$I_{PP} = -5.2\text{ A}$	-	-2.7	-	V

[1] This parameter is guaranteed by design.

[2] According to IEC 61000-4-5 (8/20  $\mu\text{s}$  current waveform).

[3] 100 ns Transmission Line Pulse (TLP); 50  $\Omega$ ; pulser at 80 ns.

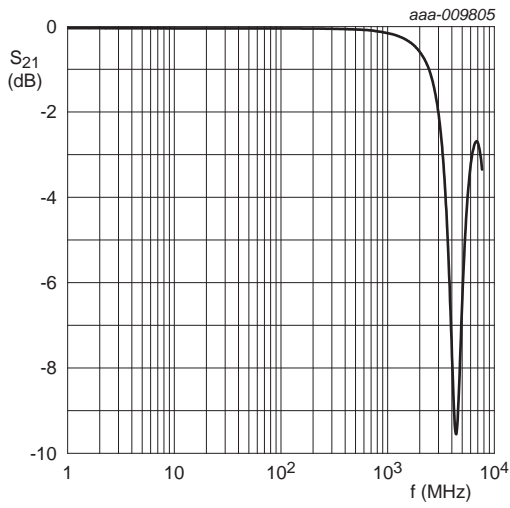


Fig 1. Insertion loss; typical values

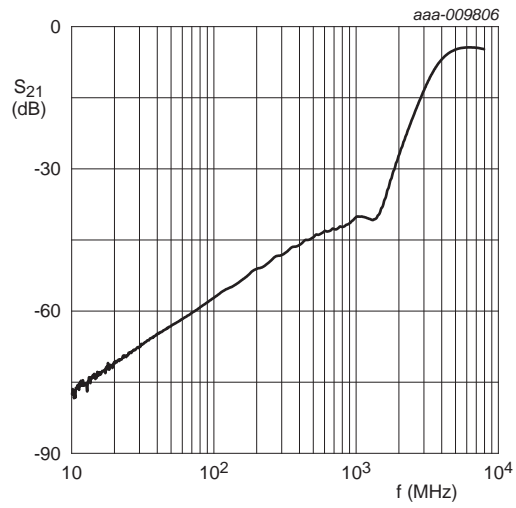
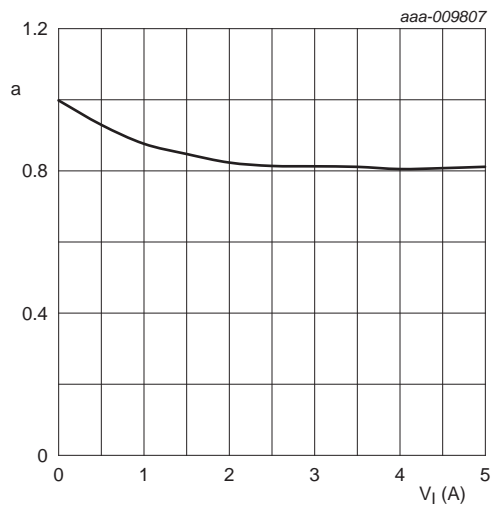
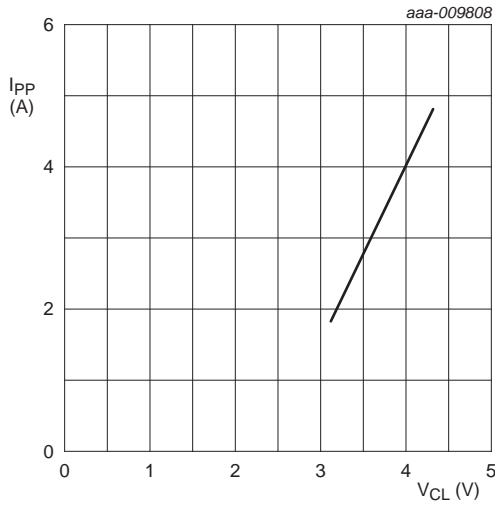


Fig 2. Crosstalk; typical values



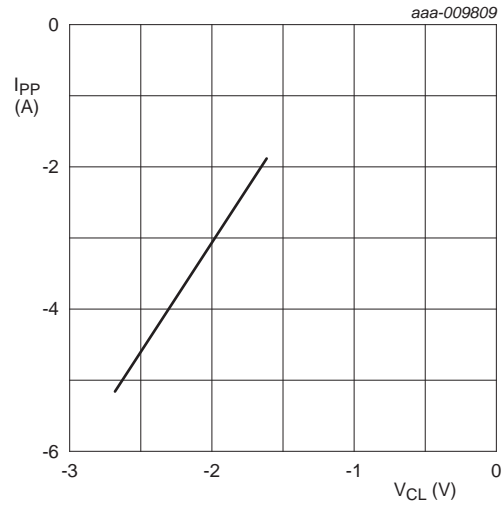
$$a = \frac{C_{line}}{C_{line}(V_1 = 0 V)}$$

Fig 3. Relative capacitance as a function of input voltage; typical values



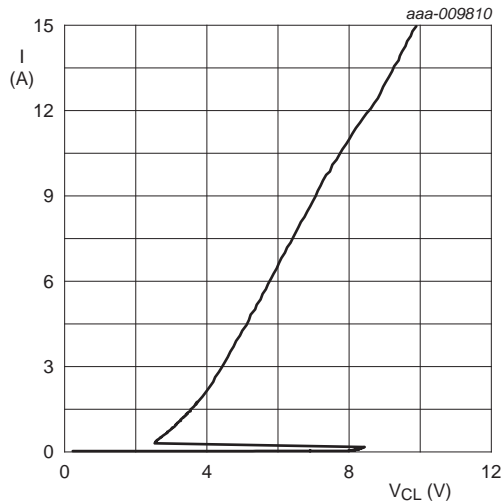
IEC 61000-4-5;  $t_p = 8/20 \mu s$ ; positive pulse

**Fig 4. Dynamic resistance with positive clamping; typical values**



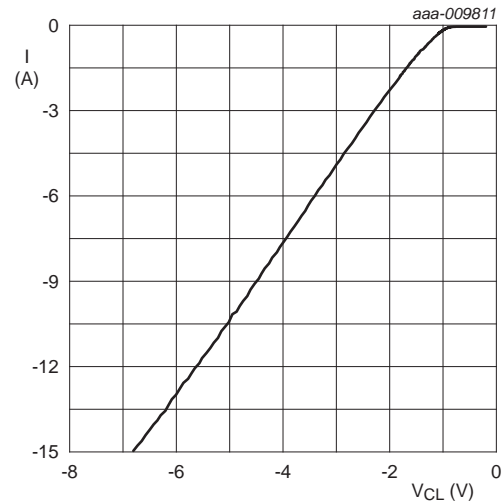
IEC 61000-4-5;  $t_p = 8/20 \mu s$ ; negative pulse

**Fig 5. Dynamic resistance with negative clamping; typical values**



$t_p = 100 ns$ ; Transmission Line Pulse (TLP)

**Fig 6. Dynamic resistance with positive clamping; typical values**

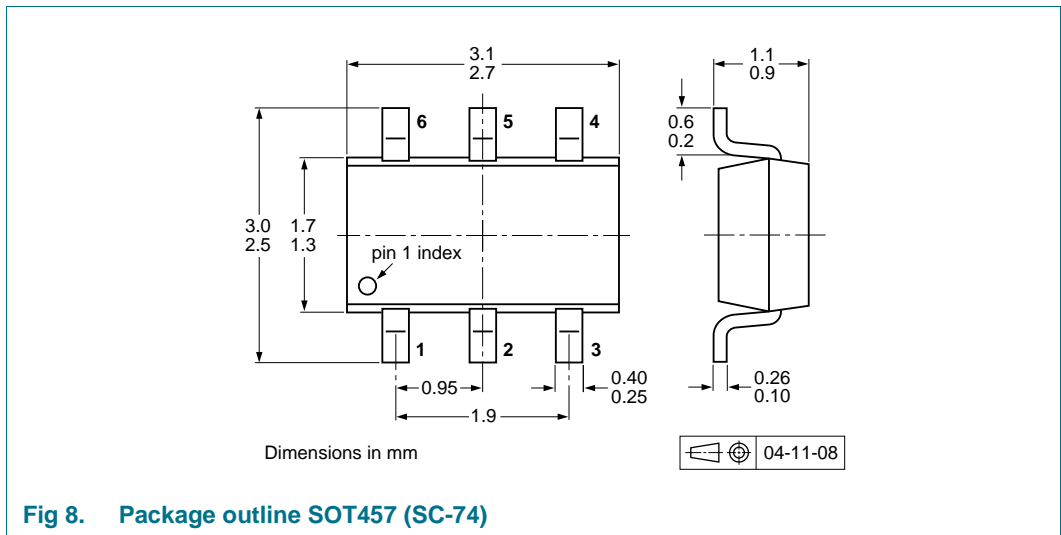


$t_p = 100 ns$ ; Transmission Line Pulse (TLP)

**Fig 7. Dynamic resistance with negative clamping; typical values**

The device uses an advanced clamping structure, which shows a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

7. Package outline



## 8. Soldering

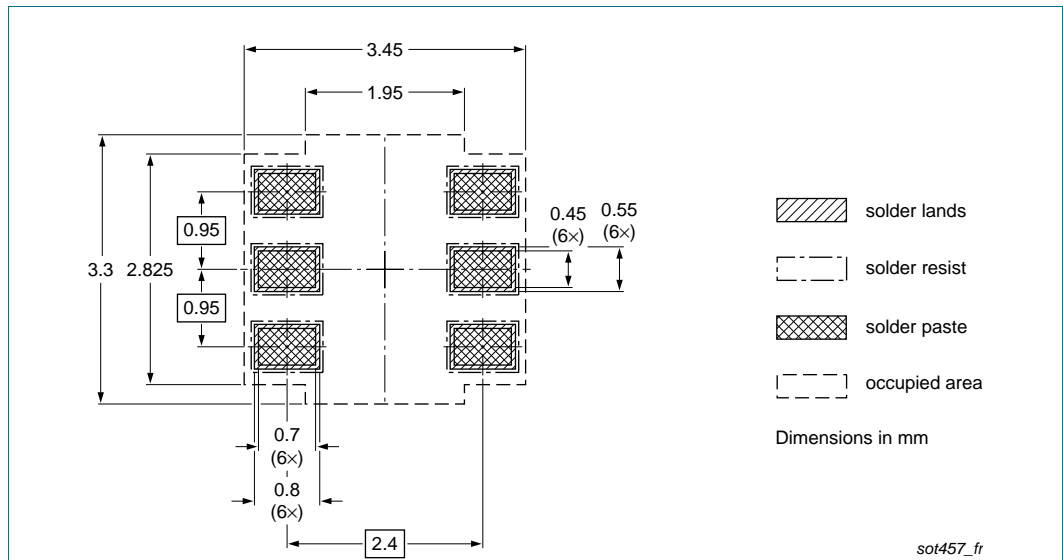


Fig 9. Reflow soldering footprint SOT457 (SC-74)

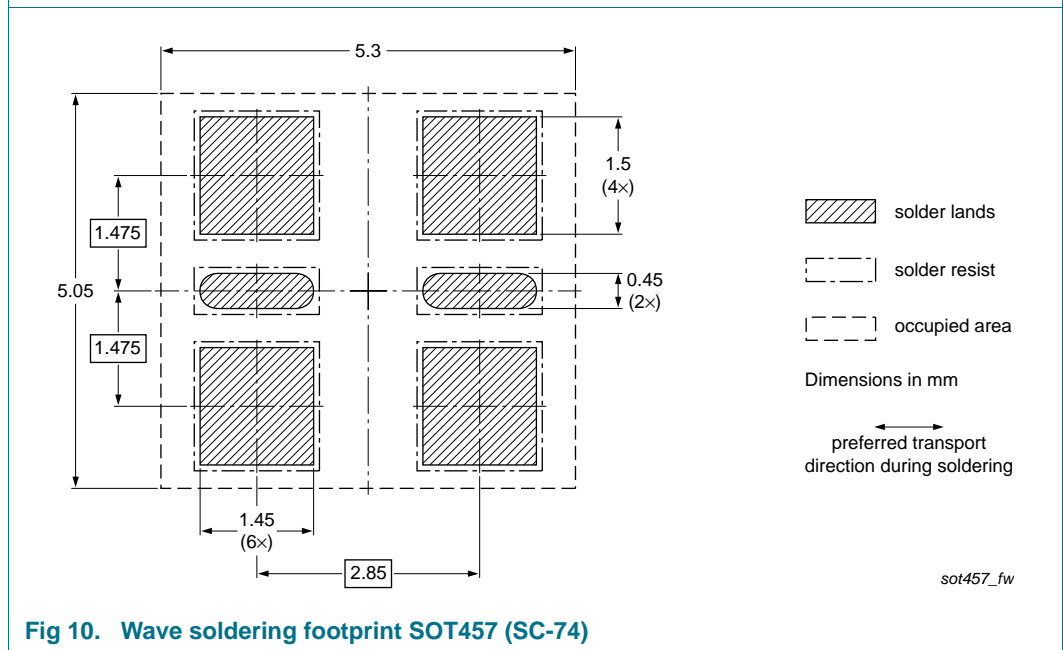


Fig 10. Wave soldering footprint SOT457 (SC-74)



## 9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PUSB2X4D v.1	20131105	Product data sheet	-	-

## 10. Legal information

### 10.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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