XC7WH126

Dual buffer/line driver; 3-state

Rev. 3 — 25 February 2019

Product data sheet

1. General description

The XC7WH126 is a high-speed Si-gate CMOS devices. This device provides a dual non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input (nOE). A LOW at nOE causes the output to assume a high-impedance OFF-state.

2. Features and benefits

- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- · Balanced propagation delays
- ESD protection:
 - HBM JESD22-A114E: exceeds 2000 V
 - MM JESD22-A115-A: exceeds 200 V
 - CDM JESD22-C101C: exceeds 1000 V
- Specified from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package							
	Temperature range	Name	Description	Version				
XC7WH126DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2				
XC7WH126DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1				

4. Marking

Table 2. Marking codes

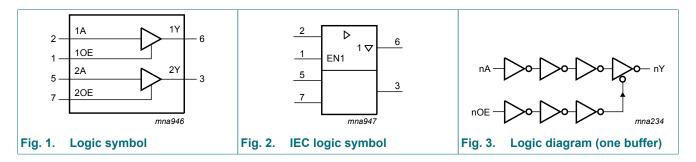
Type number	Marking[1]
XC7WH126DP	f26
XC7WH126DC	f26

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.



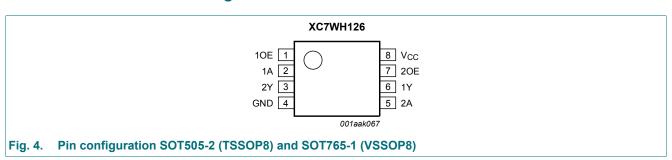
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5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Table 5. Fill description							
Symbol	Pin	Description					
10E, 20E	1, 7	output enable input (active HIGH)					
1A, 2A	2, 5	data input					
GND	4	ground (0 V)					
1Y, 2Y	6, 3	data output					
V _{CC}	8	supply voltage					

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

	Input	Output
nOE	nA	nY
Н	L	L
Н	Н	Н
L	X	Z

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V}$ [1]	-20	-	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I _O	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$	-	±25	mA
I _{CC}	supply current		-	75	mA
I_{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$ [2]	-	250	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		2.0	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	-	-	100	ns/V
		V _{CC} = 5.0 V ± 0.5 V	-	-	20	ns/V

^[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K. For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

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10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol Parameter		Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Тур	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = -50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
		I_{O} = -8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
I _{OZ}	OFF-state output current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	0.25	-	2.5	-	10	μΑ
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	1.0	-	10	-	40	μΑ
Cı	input capacitance		-	1.5	10	-	10	-	10	pF

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11. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V; for test circuit see Fig. 7.

Symbol	Parameter	Conditions			25 °C		-40 °C	to +85 °C	-40 °C to +125 °C		Unit
				Min	Тур	Max	Min	Max	Min	Max	
t _{pd}	propagation	nA to nY; see Fig. 5	[1]								
t _{pd} propagation delay		V _{CC} = 3.0 V to 3.6 V	[2]								
		C _L = 15 pF		-	4.7	8.0	1.0	9.5	1.0	11.5	ns
		C _L = 50 pF		-	6.6	11.5	1.0	13.0	1.0	14.5	ns
		V _{CC} = 4.5 V to 5.5 V	[3]								
		C _L = 15 pF		-	3.4	5.5	1.0	6.5	1.0	7.0	ns
		C _L = 50 pF		-	4.8	7.5	1.0	8.5	1.0	9.5	ns
t _{en}	enable time	nOE to nY; see Fig. 6	[1]								
		V _{CC} = 3.0 V to 3.6 V	[2]								
		C _L = 15 pF		-	5.0	8.0	1.0	9.5	1.0	11.5	ns
		C _L = 50 pF		-	6.9	11.5	1.0	13.0	1.0	14.5	ns
		V _{CC} = 4.5 V to 5.5 V	[3]								
		C _L = 15 pF		-	3.6	5.1	1.0	6.0	1.0	6.5	ns
		C _L = 50 pF		-	4.9	7.5	1.0	9.0	1.0	9.5	ns
t _{dis}	disable time	nOE to nY; see Fig. 6	[1]								
		V _{CC} = 3.0 V to 3.6 V	[2]								
		C _L = 15 pF		-	6.0	9.7	1.0	11.5	1.0	12.5	ns
		C _L = 50 pF		-	8.3	13.2	1.0	15.0	1.0	16.5	ns
		V _{CC} = 4.5 V to 5.5 V	[3]								
		C _L = 15 pF		-	4.1	6.8	1.0	8.0	1.0	8.5	ns
		C _L = 50 pF		-	5.7	8.8	1.0	10.0	1.0	11.0	ns
C _{PD}	power dissipation capacitance	per buffer; $C_L = 50 \text{ pF}$; $f_i = 1 \text{ MHz}$; $V_I = \text{GND to } V_{CC}$	[4]	-	10	-	-	-	-	-	pF

 t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{en} is the same as t_{PZL} and t_{PZH} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} . Typical values are measured at V_{CC} = 3.3 V. Typical values are measured at V_{CC} = 5.0 V.

 $P_D = C_{PD} x V_{CC}^2 x f_i + \sum (C_L x V_{CC}^2 x f_o)$ where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

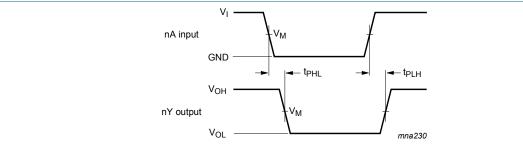
C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts.

^[4] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

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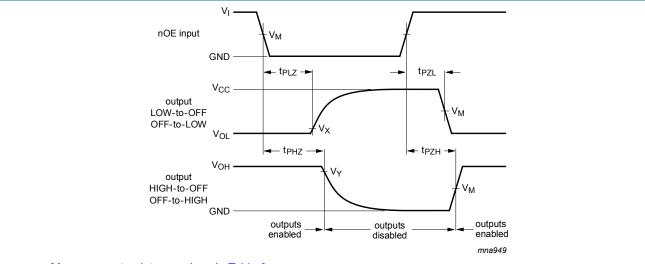
11.1. Waveforms and test circuit



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Input (nA) to output (nY) propagation delays



Measurement points are given in Table 9.

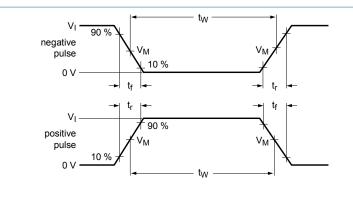
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

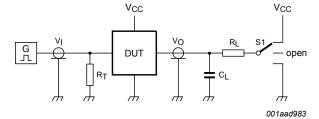
Fig. 6. Enable and disable times

Table 9. Measurement points

Туре	Input	Output				
	V_{M}	V _M	V_X	V _Y		
XC7WH126	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.3 V	V _{OH} - 0.3 V		

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Test data is given in Table 10.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 C_L = Load capacitance including jig and probe capacitance.

 R_L = Load resistance.

S1 = Test selection switch.

Fig. 7. Test circuit for measuring switching times

Table 10. Test data

Туре	Input	Load			S1 position		
	V _I	t _r , t _f	C _L	R_L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t_{PZL}, t_{PLZ}
XC7WH126	V _{CC}	≤ 3 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}

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12. Package outline

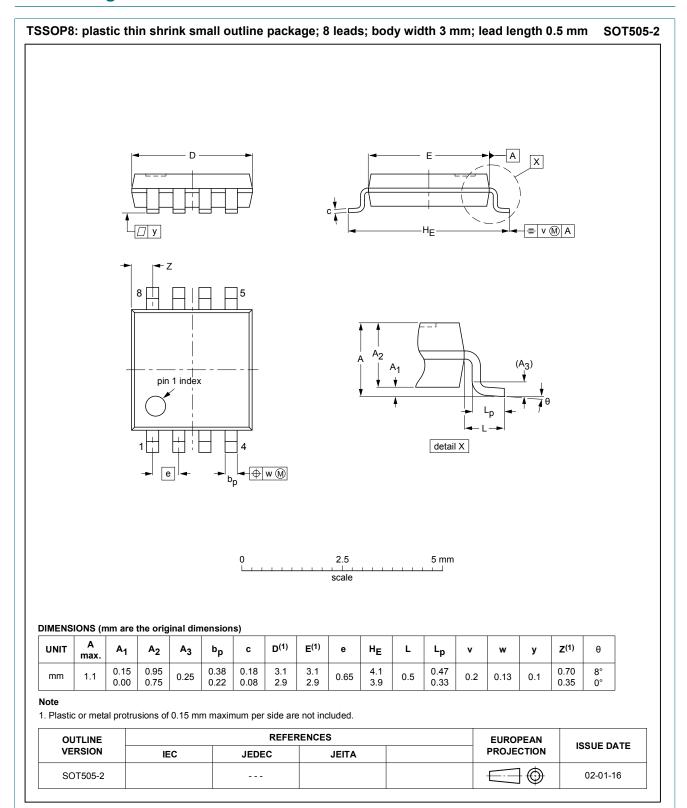


Fig. 8. Package outline SOT505-2 (TSSOP8)

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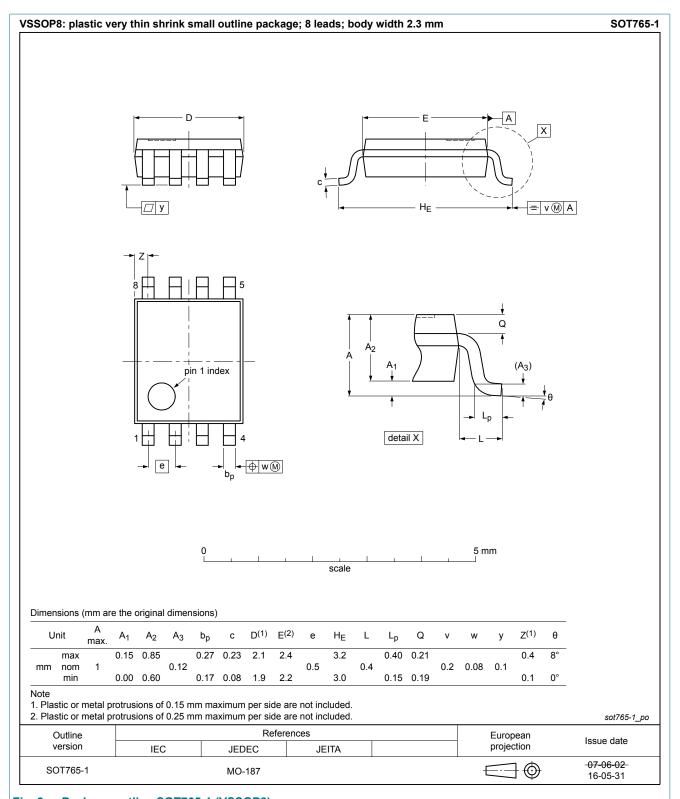


Fig. 9. Package outline SOT765-1 (VSSOP8)

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13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 12. Revision history

Document ID	ment ID Release date Data sheet status		Release date Data sheet status Change notice		9		Supersedes	
XC7WH126 v.3	20190225	Product data sheet	-	XC7WH126 v.2				
Modifications:	guidelines of Legal texts h Type number Table 3: pin o	e format of this data sheet has been redesigned to comply with the identity idelines of Nexperia. gal texts have been adapted to the new company name where appropriate. be number XC7WH126GD (SOT996-2 / (XSON8) removed. ble 3: pin description for pins 1OE and 2OE corrected. 9: package outline drawing SOT765-1 changed.						
XC7WH126 v.2	20130508	Product data sheet - XC		XC7WH126 v.1				
Modifications:	For type num	For type number XC7WH126GD XSON8U has changed to XSON8.						
XC7WH126 v.1	20090902	Product data sheet	-					

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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