

## System Reset IC with Watchdog Timer

### ■FEATURES

- Full compatible with NJM2102
- Detection voltage  $V_{SL}=4.2V\pm 1.0\%$
- Watchdog timer function
- Reset output of both positive and negative logic
- Operating temperature  $T_a=-40$  to  $125^\circ\text{C}$
- Low quiescent current  $320\mu\text{A typ.}$
- Low reset operation voltage  $0.8V$  typ.
- Package DMP8

### ■GENERAL DESCRIPTION

The NJU2102A is a system reset IC with watchdog timer to detect the abnormal conditions, such as shutdown of all supply voltages at once, or sudden voltage down and then generate the reset signal.

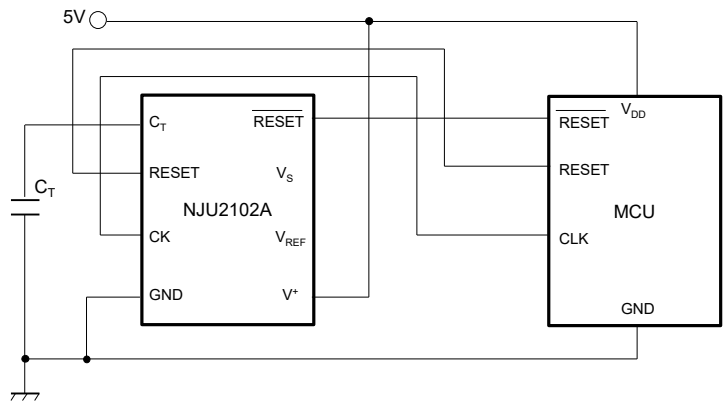
It is possible to direct replacement from NJM2102.

Furthermore, it improves usability by extending operating temperature, standardizing AC characteristics, and making each parameter highly accurate.

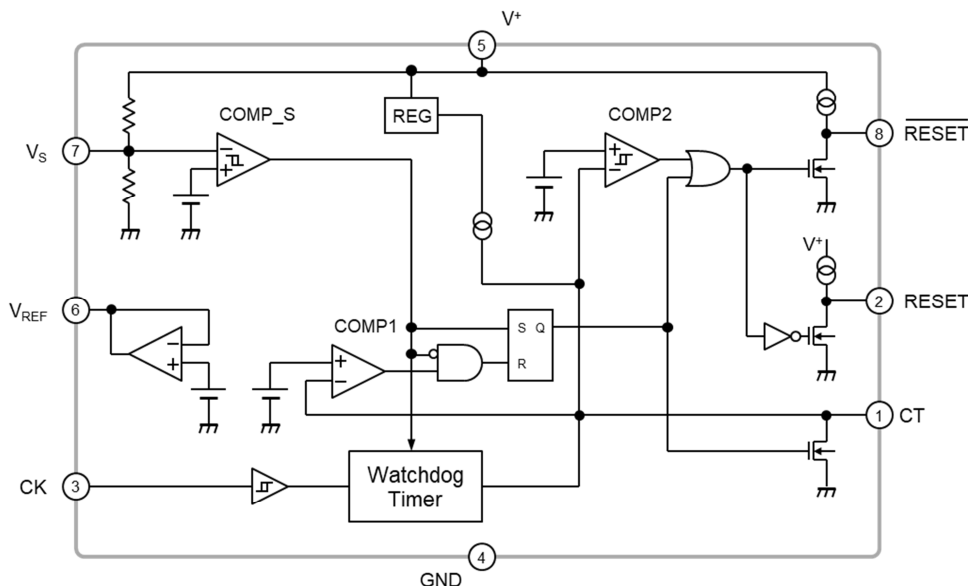
### ■APPLICATION

- Industrial equipment
- Housing and facility equipment
- OA equipment
- Amusement equipment

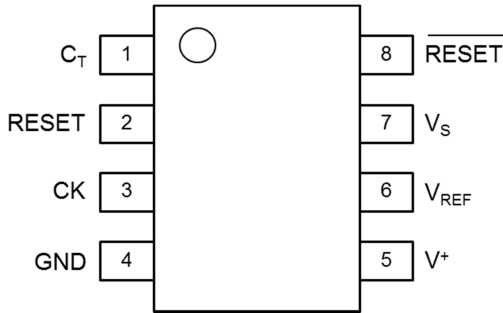
### ■TYPICAL APPLICATION



### ■BLOCK DIAGRAM



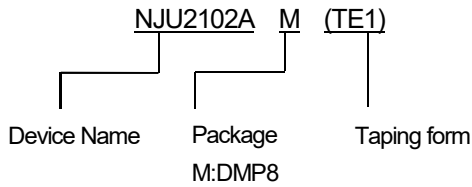
## ■PIN CONFIGURATION



DMP8

PIN No.	PIN NAME	FUNCTION
1	C <sub>T</sub>	Connects Capacitor pin for setting WDT monitor time, WDT reset time, and Reset signal hold time.
2	RESET	RESET output pin. (Active High)
3	CK	Clock input pin.
4	GND	GND pin.
5	V <sup>+</sup>	Power Supply pin.
6	V <sub>REF</sub>	Output reference voltage pin.
7	V <sub>S</sub>	Comparator S input pin.
8	RESET	RESET output pin. (Active Low)

## ■PRODUCT NAME INFORMATION



## ■ORDERING INFORMATION

PRODUCT NAME	PACKAGE OUTLINE	RoHS	Halogen-Free	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJU2102AM(TE1)	DMP8	○	○	Sn-2Bi	2102A	95	2000

Note) "-" is non-evaluation. Please contact your sales representative for more information.

## ■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V^+$	-0.3 to 20	V
Input Voltage	$V_S$	-0.3 to $V^+ + 0.3$ (<20)	V
Clock Input Voltage	$V_{CK}$	-0.3 to 20	V
$C_T$ Pin Voltage	$V_{CT}$	-0.3 to $V^+ + 0.3$ (<20)	V
$\overline{RESET}$ Output Voltage	$V_{\overline{RESET}}$	-0.3 to $V^+ + 0.3$ (<20)	V
RESET Output Voltage	$V_{RESET}$	-0.3 to $V^+ + 0.3$ (<20)	V
Power Dissipation (Ta=25°C) DMP8	$P_D$	(2-layer / 4-layer) 470 <sup>(1)</sup> / 600 <sup>(2)</sup>	mW
Junction Temperature	$T_J$	-40 to +150	°C
Operating Temperature	$T_{opr}$	-40 to +125	°C
Storage Temperature	$T_{stg}$	-50 to +150	°C

(1): Mounted on glass epoxy board.(76.2 x 114.3 x 1.6 :based on EIA/JEDEC standard, 2 Layers)

(2): Mounted on glass epoxy board.(76.2 x 114.3 x 1.6 :based on EIA/JEDEC standard, 4 Layers) internal Cu area: 74.2 x 74.2mm

## ■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V^+$	3.5 to 18	V
Input Voltage	$V_S$	0 to $V^+$	V
Clock Input Voltage	$V_{CK}$	0 to 18	V
$\overline{RESET}$ Output Current	$I_{\overline{RESET}}$	0 to 20	mA
RESET Output Current	$I_{RESET}$	0 to 20	mA
$V_{REF}$ Output Current	$I_{VREF}$	-200 to +5	μA
Watchdog Timer Monitor Time	$t_{WD}$	0.1 to 1000	ms
Watchdog Timer Reset Time	$t_{WR}$	0.02 to 200	ms
Reset Signal Hold Time	$t_{PR}$	1 to 10000	ms
$C_T$ Pin Capacitor	$C_T$	0.001 to 10	μF

## ■ELECTRICAL CHARACTERISTICS

### (DC Characteristics)

Unless other noted,  $V^+=5.0V$ ,  $C_T=0.1\mu F$ ,  $T_a=25^\circ C$

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	$I_{CC}$	Watchdog timer operation	-	320	430	$\mu A$
Detection Voltage 1	$V_{SL}$	$V^+$ sweep down	4.158	4.200	4.242	V
Detection Voltage 2	$V_{SH}$	$V^+$ sweep up	4.210	4.300	4.390	V
Hysteresis Width	$V_{HYS}$	$V_{HYS} = V_{SH} - V_{SL}$	50	100	150	mV
Reference Voltage	$V_{REF}$		1.217	1.235	1.253	V
Reference Voltage Line Regulation	$\Delta V_{REF1}$	$V^+=3.5V$ to $18V$	-10	3	10	mV
Reference Voltage Load Regulation	$\Delta V_{REF2}$	$I_{OUT}=-200\mu A$ to $+5\mu A$	-5	-	5	mV
CK Input Threshold Voltage	$V_{TH}$		0.7	1.2	1.9	V
CK Input Current 1	$I_{IH}$	$V_{CK}=5V$	-	10	20	$\mu A$
CK Input Current 2	$I_{IL}$	$V_{CK}=0V$	-0.1	0	0.1	$\mu A$
$C_T$ Charge Current 1	$I_{CTC1}$	Watchdog timer operation, $V_{CT}=1V$	20	50	110	$\mu A$
$C_T$ Charge Current 2	$I_{CTC2}$	Power on reset operating, $V_{CT}=1V$	0.6	1.4	3.0	$\mu A$
$C_T$ Discharge Current 1	$I_{CTD1}$	Watchdog timer operation, $V_{CT}=1V$	6	10	13	$\mu A$
$C_T$ Discharge Current 2	$I_{CTD2}$	Power on reset operating, $V_{CT}=1V$	100	2000	-	$\mu A$
High Level Output Voltage 1	$V_{OH1}$	$V_S=OPEN$ , $I_{RESET}=-5\mu A$	4.5	4.9	-	V
High Level Output Voltage 2	$V_{OH2}$	$V_S=0V$ , $I_{RESET}=-5\mu A$	4.5	4.9	-	V
Output Saturation Voltage 1	$V_{OL1}$	$V_S=0V$ , $I_{RESET}=3mA$	-	0.05	0.4	V
Output Saturation Voltage 2	$V_{OL2}$	$V_S=0V$ , $I_{RESET}=10mA$	-	0.15	0.5	V
Output Saturation Voltage 3	$V_{OL3}$	$V_S=OPEN$ , $I_{RESET}=3mA$	-	0.05	0.4	V
Output Saturation Voltage 4	$V_{OL4}$	$V_S=OPEN$ , $I_{RESET}=10mA$	-	0.15	0.5	V
Output Sink Current 1	$I_{OL1}$	$V_S=0V$ , $V_{RESET}=1V$	20	60	-	mA
Output Sink Current 2	$I_{OL2}$	$V_S=OPEN$ , $V_{RESET}=1V$	20	60	-	mA
RESET Minimum Operating Voltage	$V_{OCL1}$	$V_{RESET}=0.4V$ , $I_{RESET}=0.2mA$	-	0.8	1.2	V
RESET Minimum Operating Voltage	$V_{OCL2}$	$V_{RESET}=V^+-0.1V$ , $R_L=1M\Omega$ (RESET-GND)	-	0.8	1.2	V

### (AC Characteristics)

Unless other noted,  $V^+=5.0V$ ,  $C_T=0.1\mu F$ ,  $T_a=25^\circ C$

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$V^+$ Input Pulse width	$t_{PI}$		8	-	-	$\mu s$
CK Input Pulse width	$t_{CKW}$		3	-	-	$\mu s$
CK Input Cycle	$t_{CK}$		20	-	-	$\mu s$
Watchdog Timer Monitor Time	$t_{WD}$	$C_T=0.1\mu F$	5	10	15	ms
Watchdog Timer Reset Time	$t_{WR}$	$C_T=0.1\mu F$	1	2	3	ms
Reset Signal Hold Time	$t_{PR}$	$C_T=0.1\mu F$	50	100	150	ms
Output Propagation Delay Time from $V^+$	$t_{PD1}$	RESET pin, $R_L=2.2k\Omega$ , $C_L=100pF$	-	2	10	$\mu s$
	$t_{PD2}$	RESET pin, $R_L=2.2k\Omega$ , $C_L=100pF$	-	3	10	$\mu s$
Output Rise Time	$t_{R1}$	RESET pin, 10% to 90%, $R_L=2.2k\Omega$ , $C_L=100pF$	-	1.0	1.5	$\mu s$
	$t_{R2}$	RESET pin, 10% to 90%, $R_L=2.2k\Omega$ , $C_L=100pF$	-	1.0	1.5	$\mu s$
Output Fall Time	$t_{F1}$	RESET pin, 90% to 10%, $R_L=2.2k\Omega$ , $C_L=100pF$	-	0.1	0.5	$\mu s$
	$t_{F2}$	RESET pin, 90% to 10%, $R_L=2.2k\Omega$ , $C_L=100pF$	-	0.1	0.5	$\mu s$

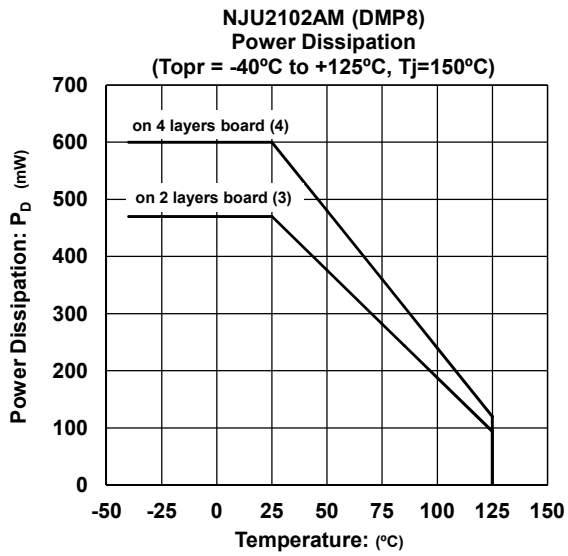
## ■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE		UNIT
Junction-to-ambient thermal resistance	$\theta_{ja}$	DMP8	262 <sup>(3)</sup> 206 <sup>(4)</sup>	°C/W
Junction-to-Top of package characterization parameter	$\psi_{jt}$	DMP8	72 <sup>(3)</sup> 65 <sup>(4)</sup>	°C/W

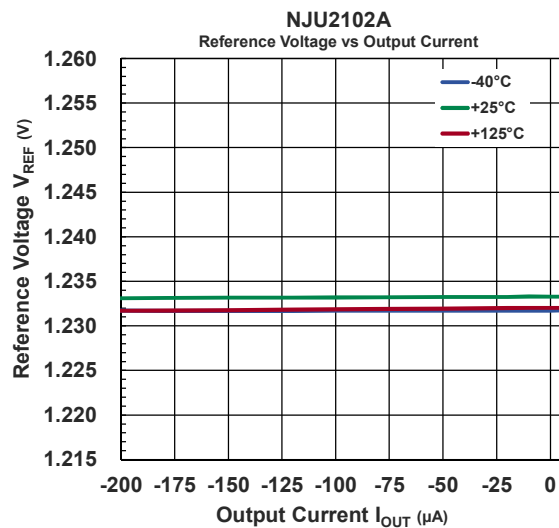
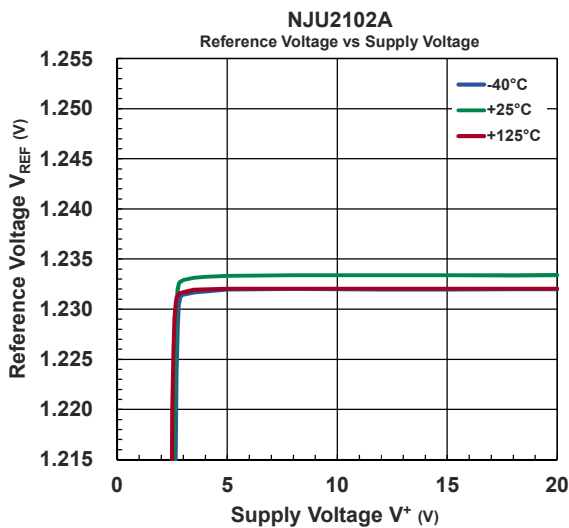
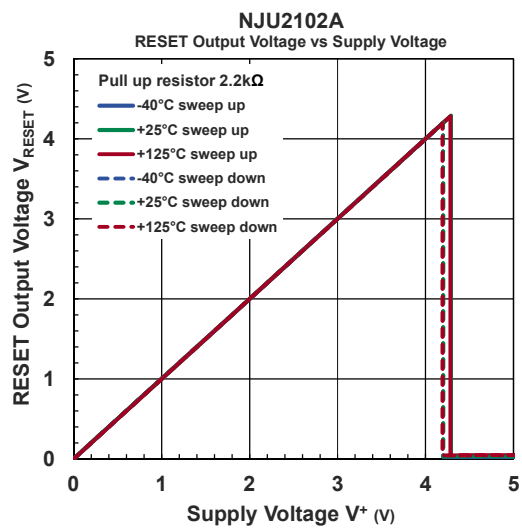
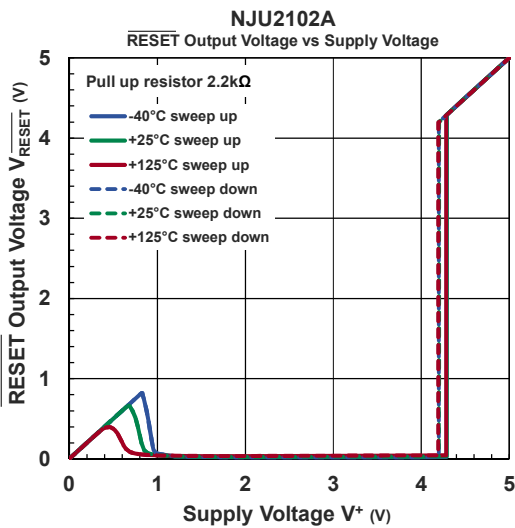
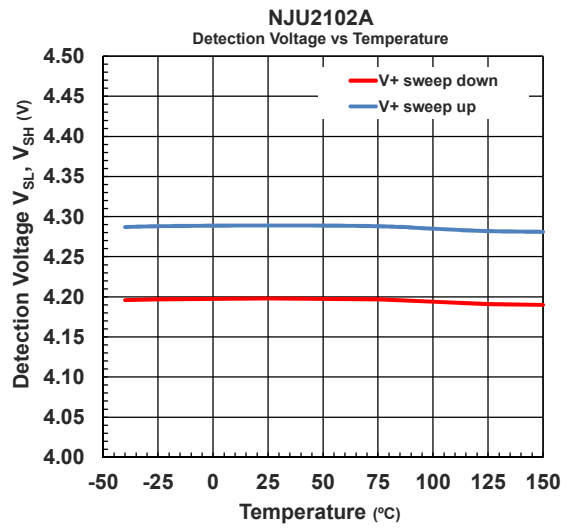
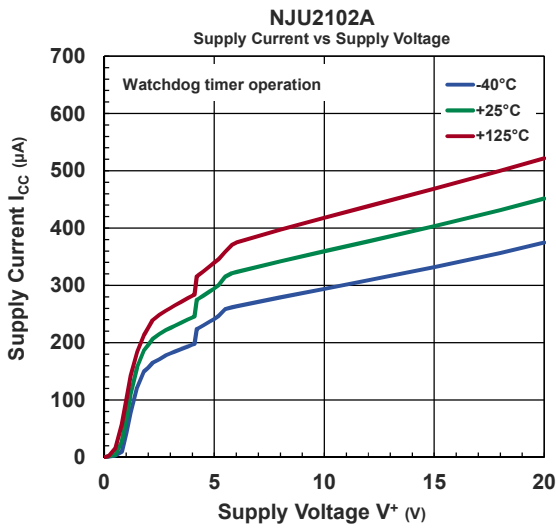
(3): Mounted on glass epoxy board.(76.2 x 114.3 x 1.6 :based on EIA/JEDEC standard, 2 Layers)

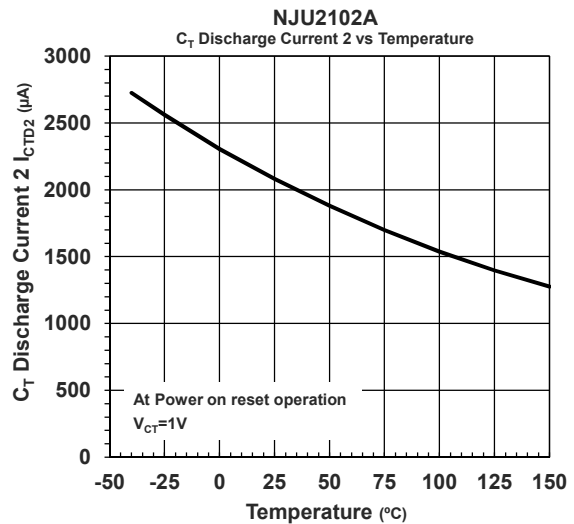
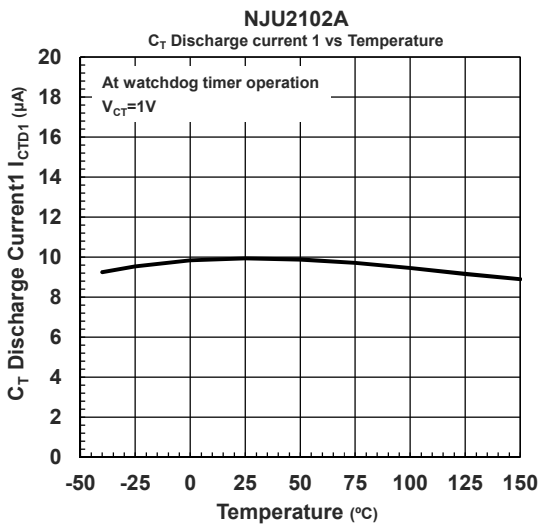
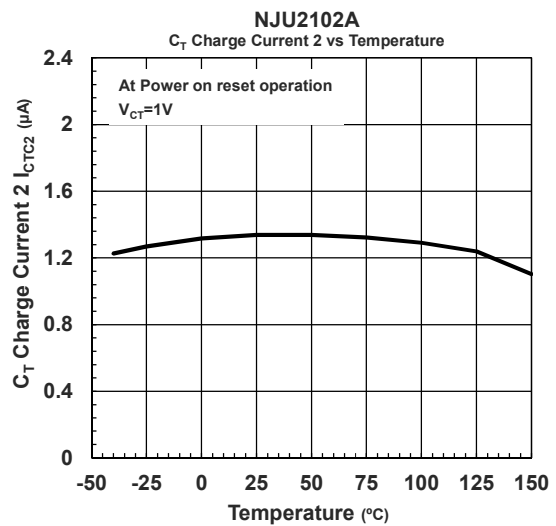
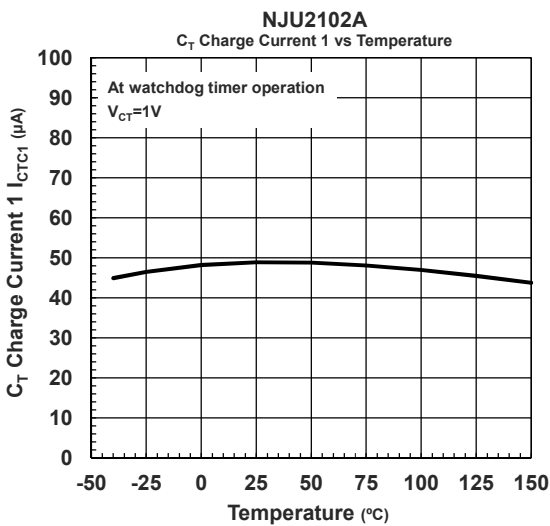
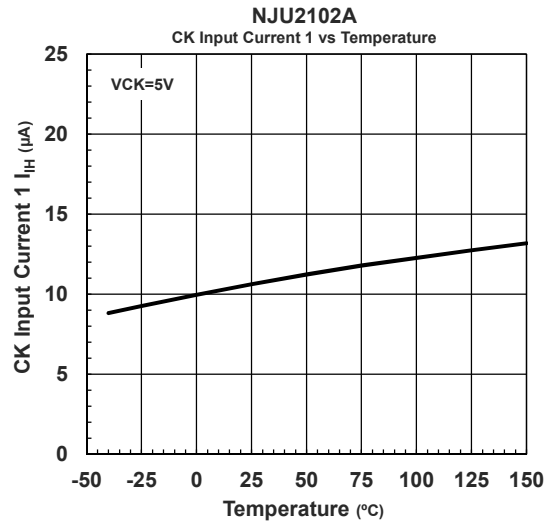
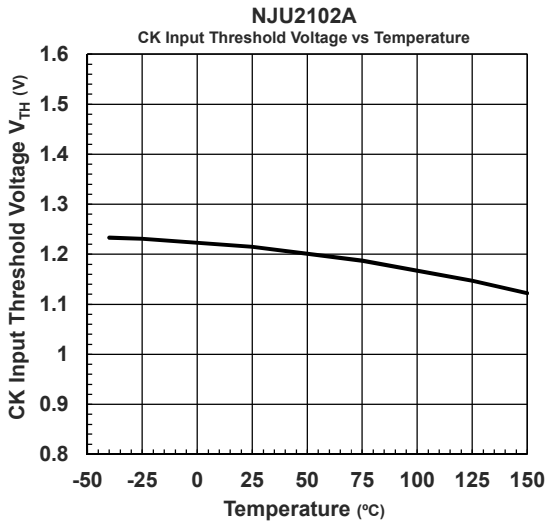
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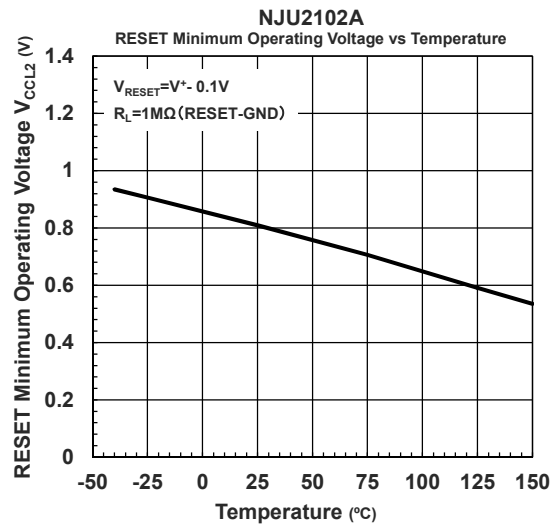
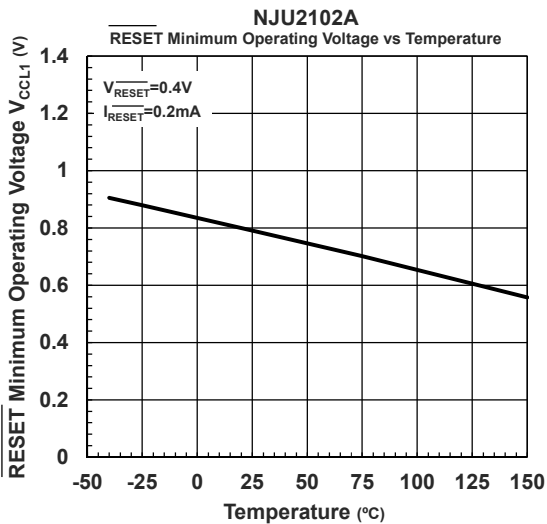
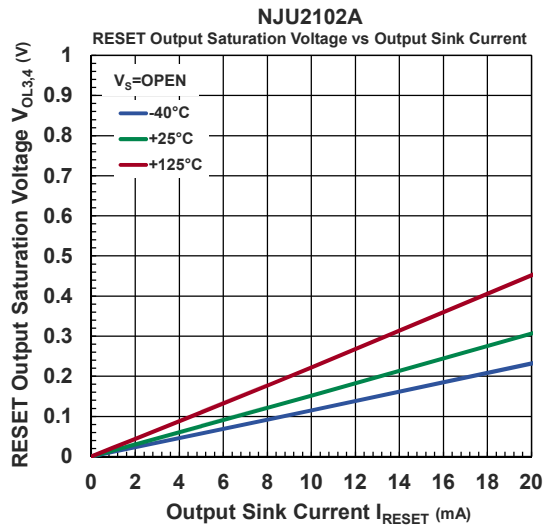
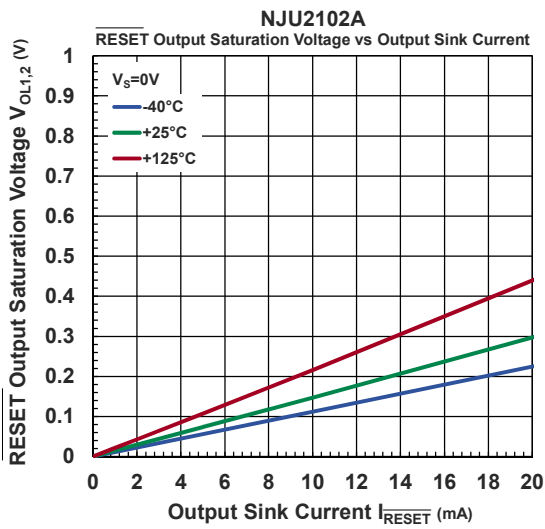
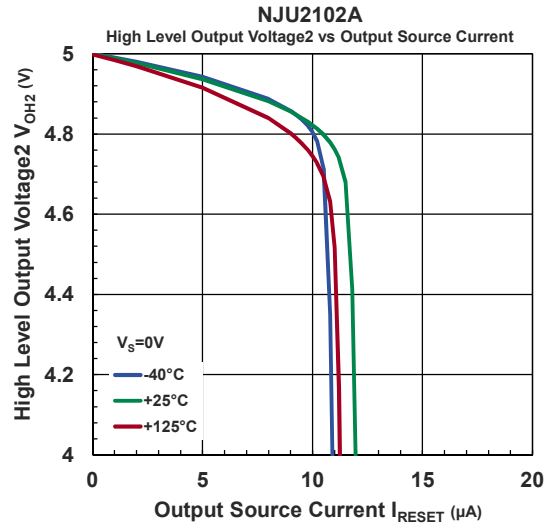
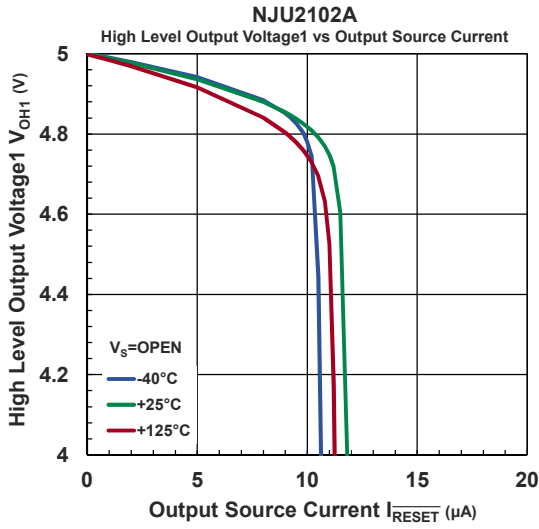
## ■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



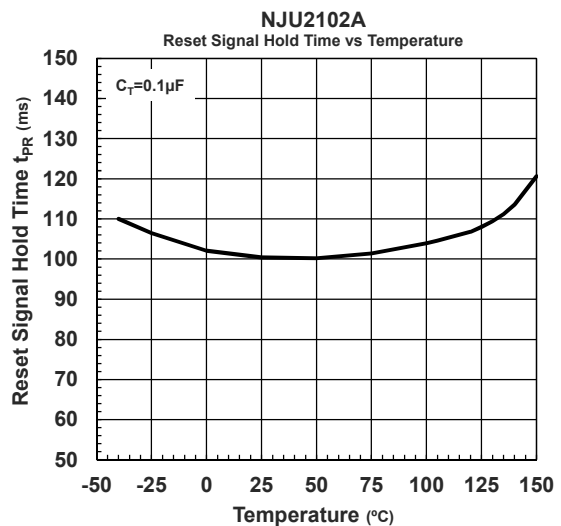
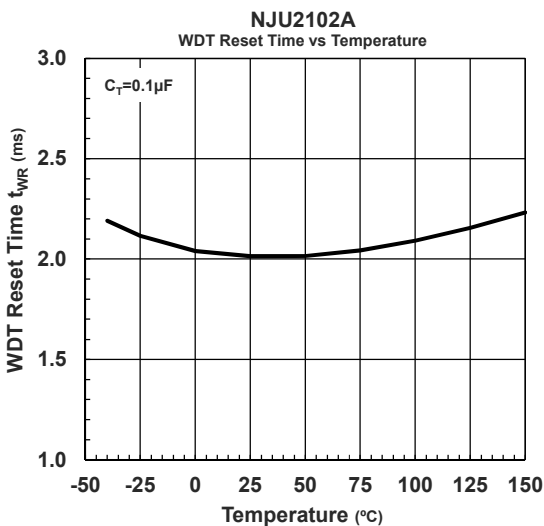
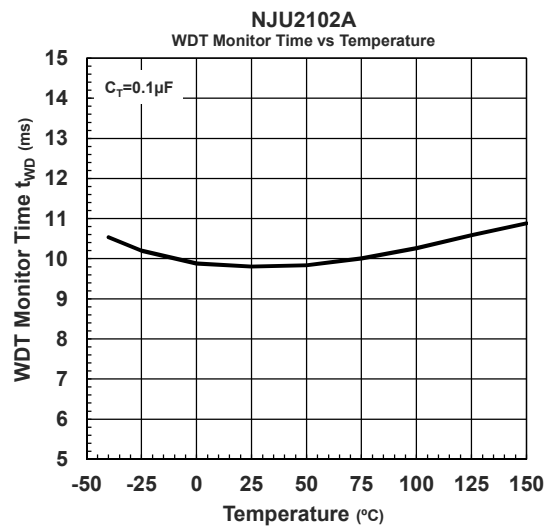
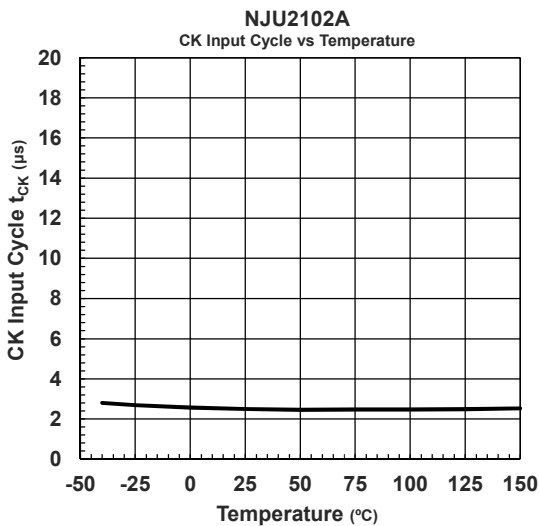
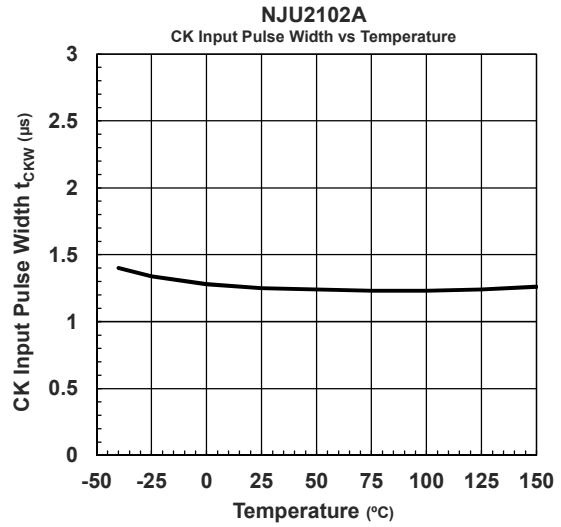
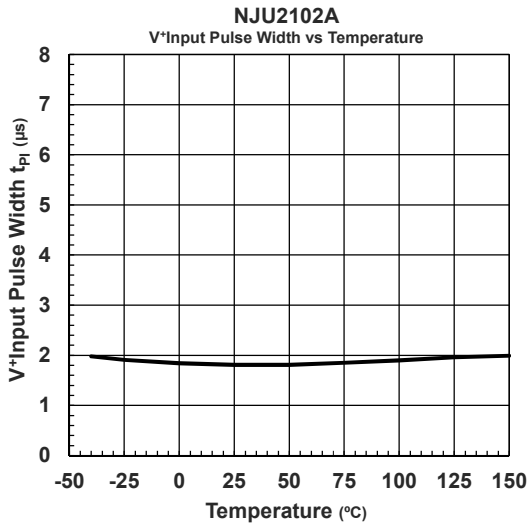
## ■ TYPICAL CHARACTERISTICS

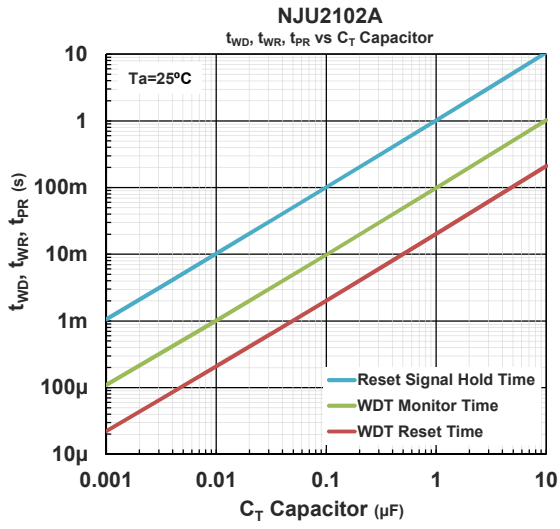








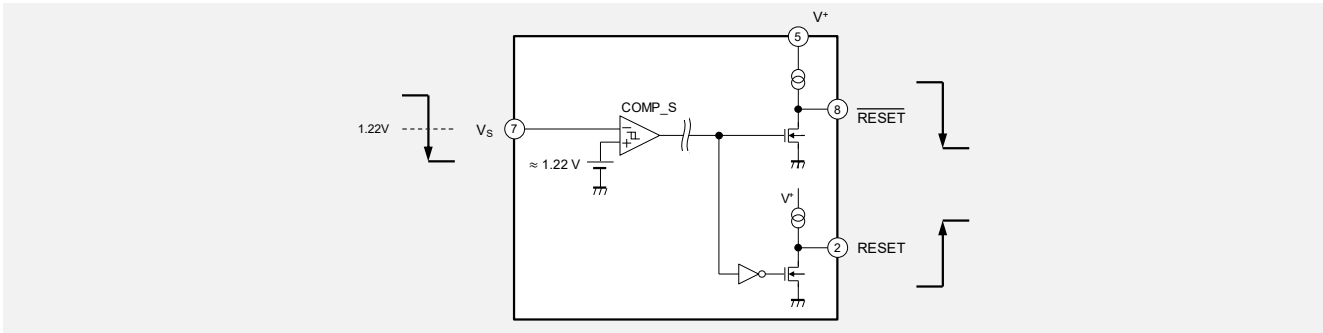




## Technical Information

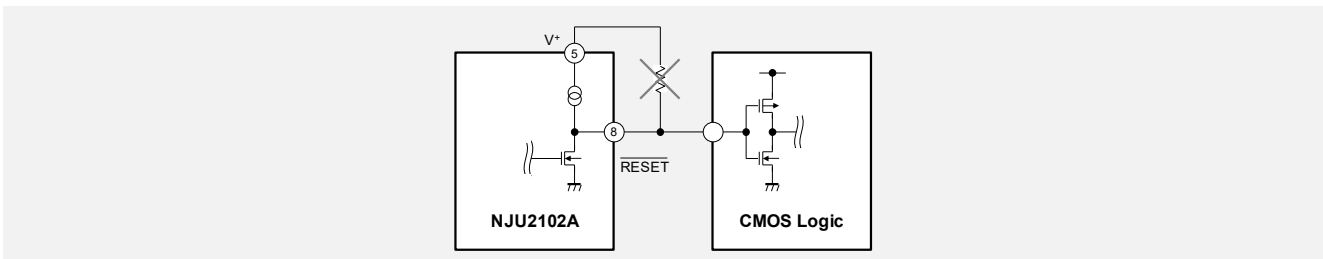
### FUNCTION EXPLANATION

The  $\overline{\text{COMP\_S}}$  is the comparator with hysteresis in detection voltage. When  $V_S$  pin voltage becomes about 1.22V or less, the  $\overline{\text{RESET}}$  output becomes "Low" and RESET output becomes "High".



The NJU2102A can detect the instantaneous interruption and the instantaneous drop of the power line with a time of about 2  $\mu\text{s}$  width. If this level of instantaneous interruption or drop is not a problem, it can have a delayed trigger function by connecting capacitor between the  $V_S$  pin and GND (refer to Fig.2).

Since the  $\overline{\text{RESET}}$  pin and RESET pin are internally pulled up to  $V^+$ , an external pull-up resistor isn't required in case of high impedance load like a CMOS logic IC.



The watchdog timer monitors the clock input to CK pin. And CK pin detects falling edge of clock. While the supply voltage is below the detection voltage, the watchdog timer operation is disabled.

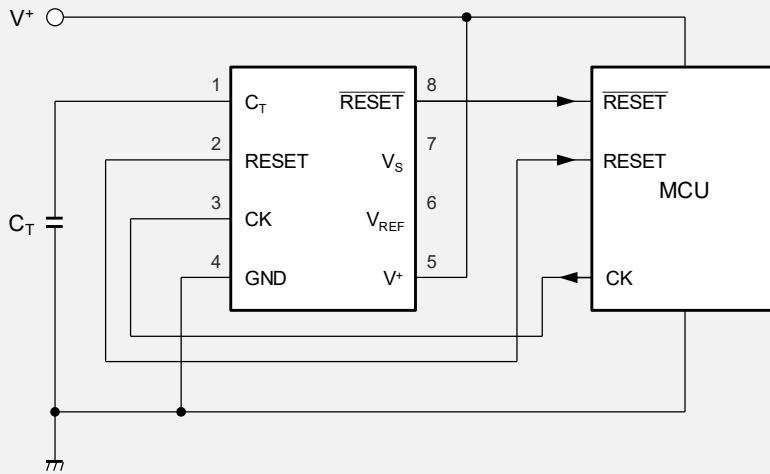
The  $V_{\text{REF}}$  pin outputs reference voltage of 1.235V typ. And it is possible to monitor the multiple supply voltage or over voltage by adding an external comparator.

Unused Pin should be treated as shown in the table below.

Pin. No.	Pin Name	Treatment method of unused Pin
2	RESET	OPEN
3	CK	Connect to GND
6	$V_{\text{REF}}$	OPEN
7	$V_S$	OPEN
8	$\overline{\text{RESET}}$	OPEN

## Technical Information

### OPERATION EXPLANATION



$$t_{PR} [\text{ms}] \approx 1000 \times C_T [\mu\text{F}]$$

$$t_{WD} [\text{ms}] \approx 100 \times C_T [\mu\text{F}]$$

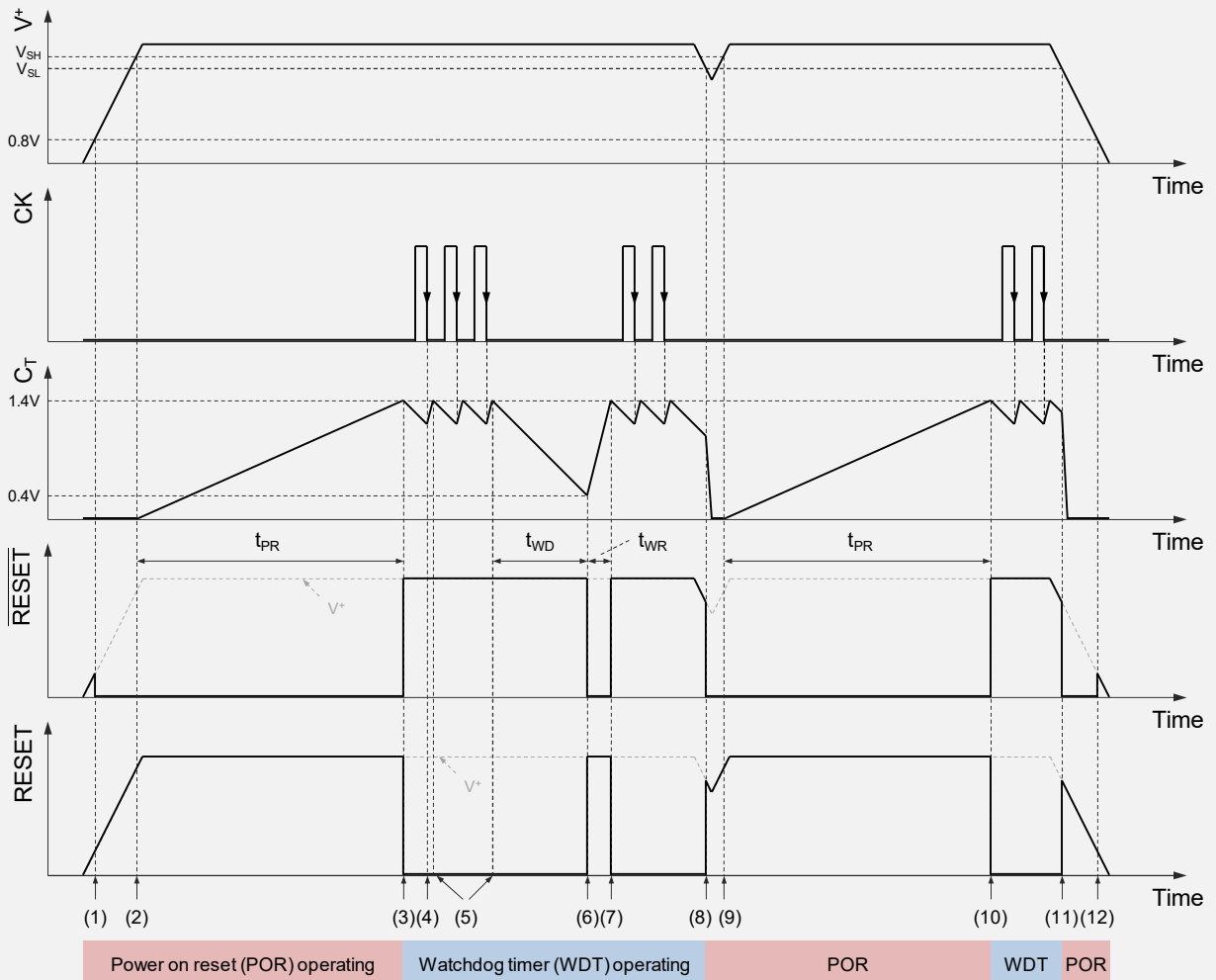
$$t_{WR} [\text{ms}] \approx 20 \times C_T [\mu\text{F}]$$

e.g.  $C_T = 0.1\mu\text{F}$

$$t_{PR} \approx 100\text{ms}$$

$$t_{WD} \approx 10\text{ms}$$

$$t_{WR} \approx 2\text{ms}$$



## Technical Information

### (Power-ON Reset Operation)

- (1) When  $V^+$  increases to Minimum operating Voltage  $V_{CCL}$  (0.8V typ.), each output becomes reset state ( $\overline{\text{RESET}}=\text{"Low"}$ ,  $\text{RESET}=\text{"High"}$ ).
- (2) When  $V^+$  increases to  $V_{SH}$  (4.3V typ.), it starts to charge to capacitor  $C_T$ . At this time, each output holds the reset state ( $\overline{\text{RESET}}=\text{"Low"}$ ,  $\text{RESET}=\text{"High"}$ ).
- (3) When the  $C_T$  voltage reaches the threshold voltage (about 1.4V), each output releases the reset state ( $\overline{\text{RESET}}=\text{"High"}$ ,  $\text{RESET}=\text{"Low"}$ ). The Reset Signal Hold Time  $t_{PR}$  is the time from when  $V^+$  reaches to  $V_{SH}$  to the output reset is released. And it is calculated as follows.

$$\text{Reset Signal Hold Time } t_{PR} [\text{ms}] \approx 1000 \times C_T [\mu\text{F}]$$

After the reset release, it starts to discharge the capacitor  $C_T$  and the watchdog timer operation is started. Also, it is not affected by CK input during power-on reset operation.

### (Watchdog Timer Operation)

- (4) If a clock from MCU is input to the CK pin during discharging of capacitor  $C_T$ ,  $C_T$  is switched from discharging to charging. And CK pin detects falling edge.
- (5) When the  $C_T$  voltage reaches the threshold voltage (about 1.4V),  $C_T$  is switched from charging to discharging. Repeat the steps (4) and (5) as long as a normal clock is input.
- (6) When the clock stops and  $C_T$  voltage decrease to the threshold voltage (about 0.4V), each output goes into reset state ( $\overline{\text{RESET}}=\text{"Low"}$ ,  $\text{RESET}=\text{"High"}$ ). At the same time,  $C_T$  is switched from discharging to charging. The Watchdog Timer Monitor Time  $t_{WD}$  is the  $C_T$  discharge time when  $C_T$  is switched from charging to discharging until reset is output. And it is calculated as follows.

$$\text{Watchdog Timer Monitor Time } t_{WD} [\text{ms}] \approx 100 \times C_T [\mu\text{F}]$$

- (7) When the  $C_T$  voltage reaches the threshold voltage (about 1.4V), the reset output is released and  $C_T$  is switched from charging to discharging ( $\overline{\text{RESET}}=\text{"High"}$ ,  $\text{RESET}=\text{"Low"}$ ). The Watchdog Timer Reset Time  $t_{WR}$  is the  $C_T$  charge time when  $C_T$  switches from charging to discharging after reset signal output and it is calculated as follows.

$$\text{Watchdog Timer Reset Time } t_{WR} [\text{ms}] \approx 20 \times C_T [\mu\text{F}]$$

After that, repeat the steps (4) and (5) as long as the normal clock is input, but when the clock stops, repeat (6) and (7).

### (Power-ON Reset Operation)

- (8) When  $V^+$  decrease below the  $V_{SL}$  (4.2V typ.), each output goes into reset state ( $\overline{\text{RESET}}=\text{"Low"}$ ,  $\text{RESET}=\text{"High"}$ ). At the same time,  $C_T$  is discharged rapidly.
- (9) When  $V^+$  increase to  $V_{SH}$ ,  $C_T$  is started to charge. In case of instantaneous  $V^+$  drop, if the time from the decreasing of  $V^+$  below  $V_{SL}$  to the increasing above  $V_{SH}$  is longer than  $V^+$  Input Pulse Width  $t_{PI}$ ,  $C_T$  charging will start after discharging  $C_T$ .
- (10) The reset output is released after  $t_{PR}$  from the time when  $V^+$  becomes higher than  $V_{SH}$  ( $\overline{\text{RESET}}=\text{"High"}$ ,  $\text{RESET}=\text{"Low"}$ ), and the watchdog timer operation is started. After that, when  $V^+$  becomes  $V_{SL}$  or less, repeat the steps (8) to (10).
- (11) In the case of power off, when  $V^+$  decrease to  $V_{SL}$ , the output becomes reset state ( $\overline{\text{RESET}}=\text{"Low"}$ ,  $\text{RESET}=\text{"High"}$ ).
- (12) Then, when  $V^+$  decrease to 0V, hold the output reset state ( $\overline{\text{RESET}}=\text{"Low"}$ ,  $\text{RESET}=\text{"High"}$ ) until  $V^+$  reaches Minimum operating Voltage  $V_{CCL}$  (0.8V typ.).

## Technical Information

### APPLICATION EXAMPLE

#### 1. 5V Power supply monitor and watchdog timer

Monitor the 5V power supply with  $V_S$ (COMP\_S). Detection voltage is Detection Voltage 1 (4.2V typ.) and Detection Voltage 2 (4.3V typ.) according to ELECTRICAL CHARACTERISTICS. Also, monitor the clock from a MCU by watchdog timer.

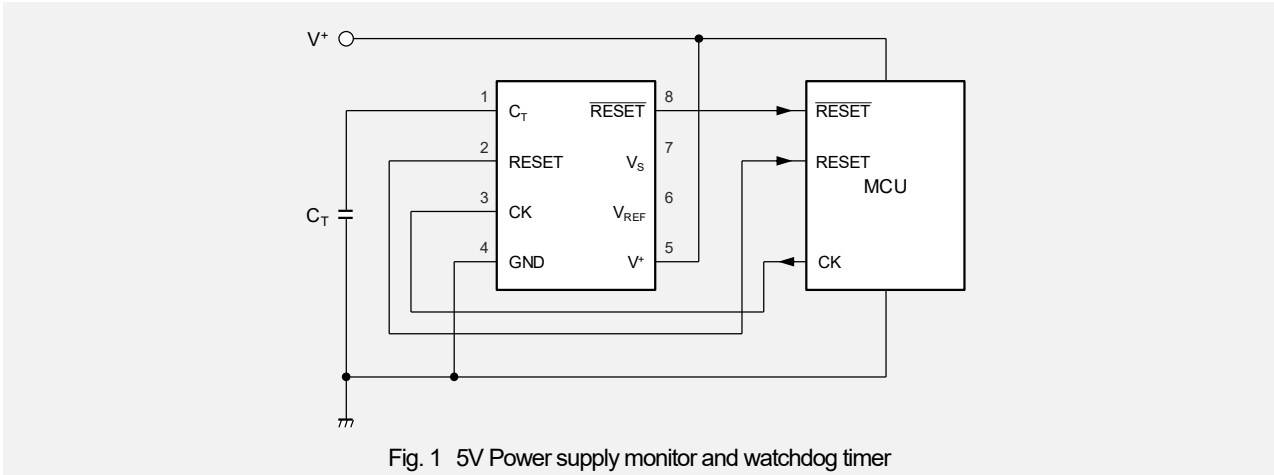


Fig. 1 5V Power supply monitor and watchdog timer

#### 2. Power supply voltage monitoring by delayed trigger

Add an arbitrary delay to the COMP\_S operation by connecting capacitor  $C_1$  between  $V_S$  pin and GND

When  $C_1$  is connected,  $V^+$  Input Pulse width  $t_{PI}$  becomes longer. e.g.  $t_{PI} = 40\mu s$  ( $C_1 = 1000pF$ )

$V^+$  Input Pulse width  $t_{PI}$  in case of  $C_1$  connected is calculated as following formula.

$$V^+ \text{ Input Pulse width } t_{PI} [\mu s] \approx (R' \parallel R'') \times \ln \left( \frac{5-4}{V_{SAL}-4} \right) \times 10^{-6} \times C_1 [\text{pF}] \approx 4.7 \times 10^{-2} \times C_1 [\text{pF}]$$

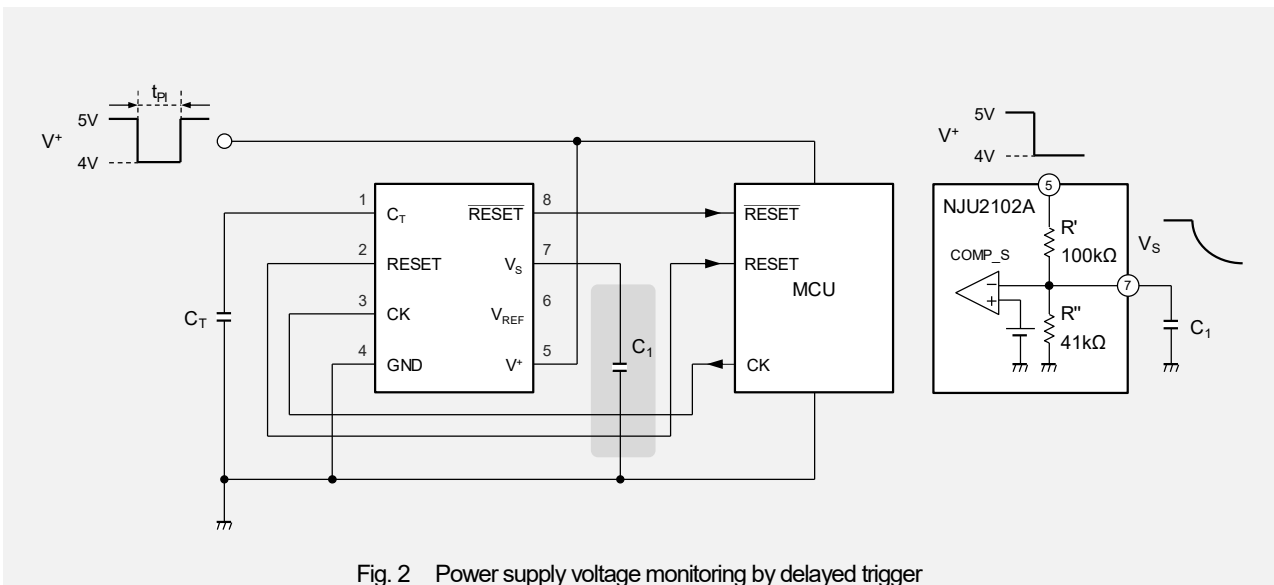


Fig. 2 Power supply voltage monitoring by delayed trigger

## Technical Information

### 3. Power supply monitor (adjust detection voltage by external resistor)

The detection voltage of  $V^+$  can be adjusted with an external resistor.

By selecting the external voltage-dividing resistors  $R_1$  and  $R_2$  to a sufficiently smaller value than internal voltage-dividing resistors  $R'$ ,  $R''$  (100 k $\Omega$ , 41 k $\Omega$ ), the detection voltage can be set by the resistance ratio of  $R_1$  and  $R_2$  (refer to Tab.1).

The detection voltage should be set higher than the recommended minimum supply voltage (3.5V). Also, the method of adjusting the detection voltage using only either  $R_1$  or  $R_2$  is not recommended because of bad accuracy.

#### Detection voltage calculate formula ( $R_1 \ll 100\text{k}\Omega$ , $R_2 \ll 41\text{k}\Omega$ )

$$\text{Detection Voltage(falling)} = \frac{(R_1 \parallel R') + (R_2 \parallel R'')}{R_2 \parallel R''} \times \frac{R''}{R' + R''} \times V_{SL} \approx \frac{R_1 + R_2}{R_2} \times 1.2213 \text{ [V]}$$

$$\text{Detection Voltage(rising)} = \frac{(R_1 \parallel R') + (R_2 \parallel R'')}{R_2 \parallel R''} \times \frac{R''}{R' + R''} \times V_{SH} \approx \frac{R_1 + R_2}{R_2} \times 1.2504 \text{ [V]}$$

Tab. 1 Setting example

External resistor $R_1$ [k $\Omega$ ]	External resistor $R_2$ [k $\Omega$ ]	Detection Voltage(falling) [V]	Detection Voltage(rising) [V]
10	3.9	4.34	4.44
9.1	3.9	4.08	4.18

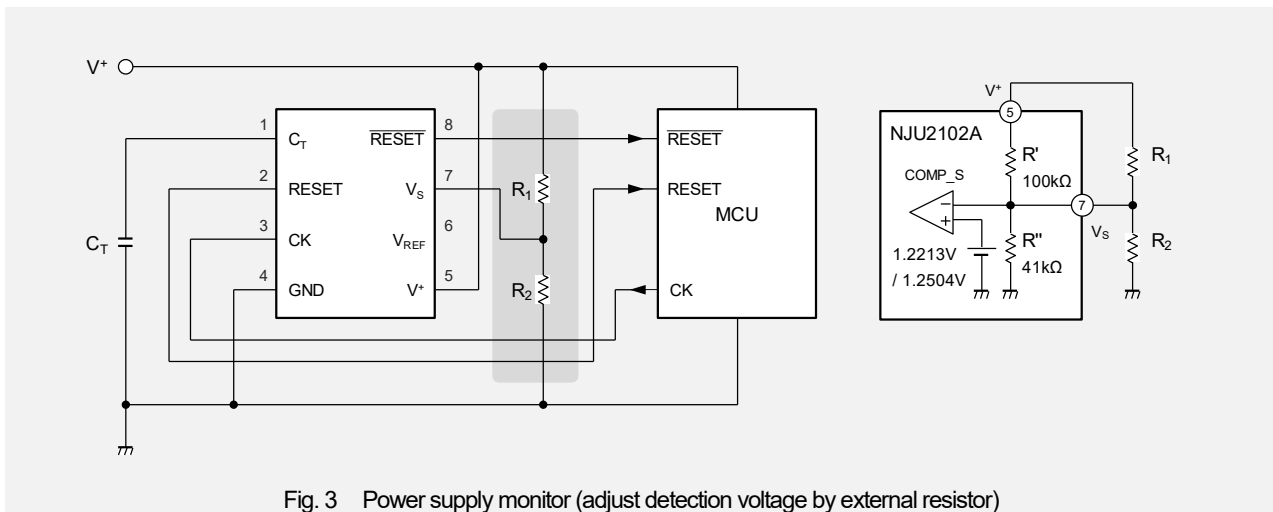


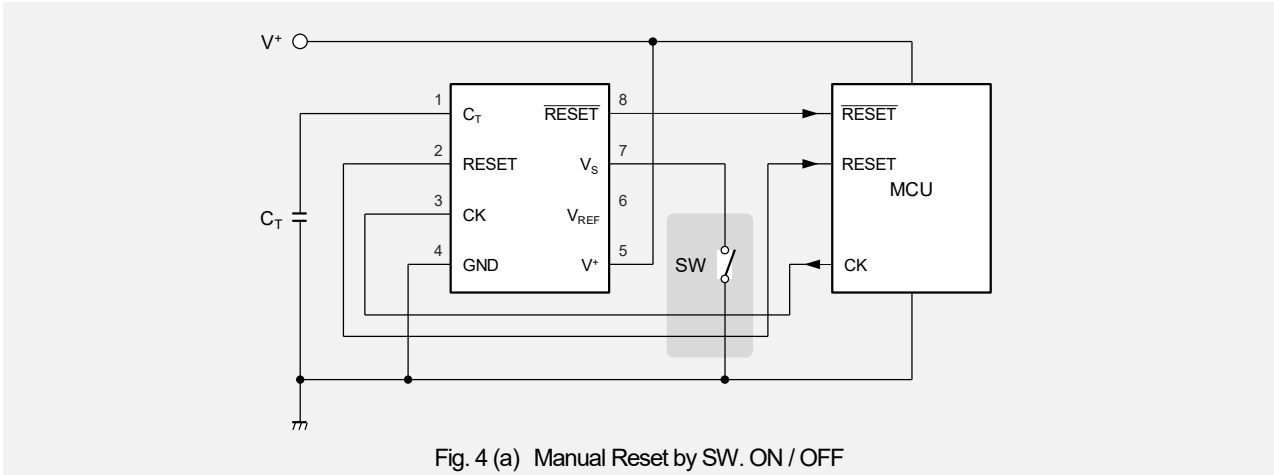
Fig. 3 Power supply monitor (adjust detection voltage by external resistor)

## Technical Information

### 4. Manual Reset function

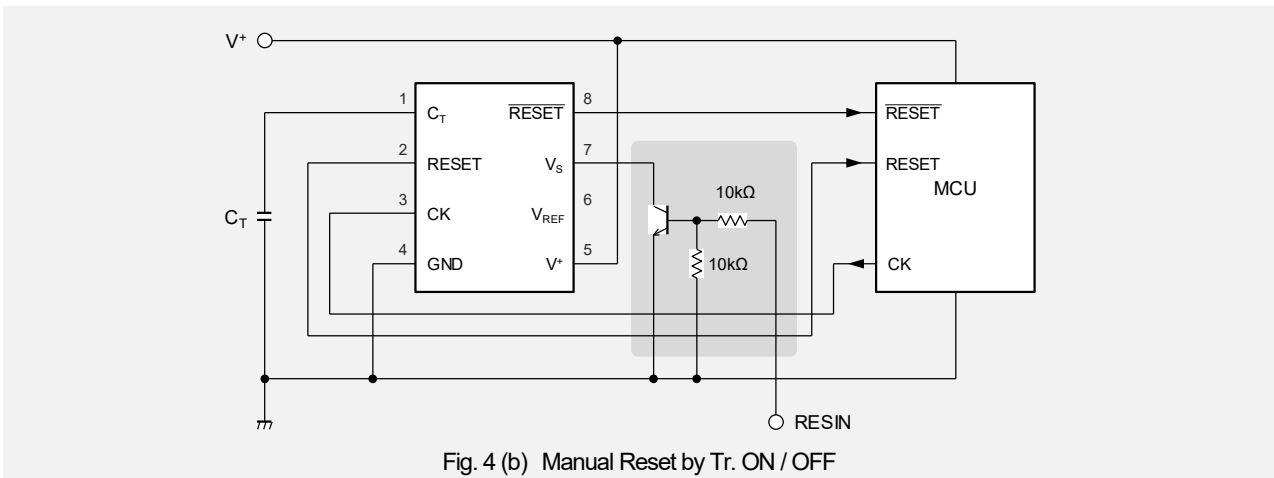
#### (a) Manual Reset by SW. ON / OFF

By setting  $V_S$  pin to GND with SW\_ON, it is possible to output reset signal ( $\overline{\text{RESET}}$ ="Low", RESET="High") arbitrarily regardless of the state of  $V^+$ .



#### (b) Manual Reset by Tr. ON / OFF

By turning on Tr. with the RESIN signal, it is possible to output reset signal ( $\overline{\text{RESET}}$ ="Low", RESET="High") arbitrarily regardless of the state of  $V^+$ .





## Technical Information

### 5. Disable watchdog timer operation

Disable watchdog timer operation when HALT="High",  $\overline{\text{HALT}}$ ="Low". When the MCU is in standby mode, even if the clock from the MCU is interrupted, it is possible to monitor the power supply without resetting by the watchdog timer.

(Notes)

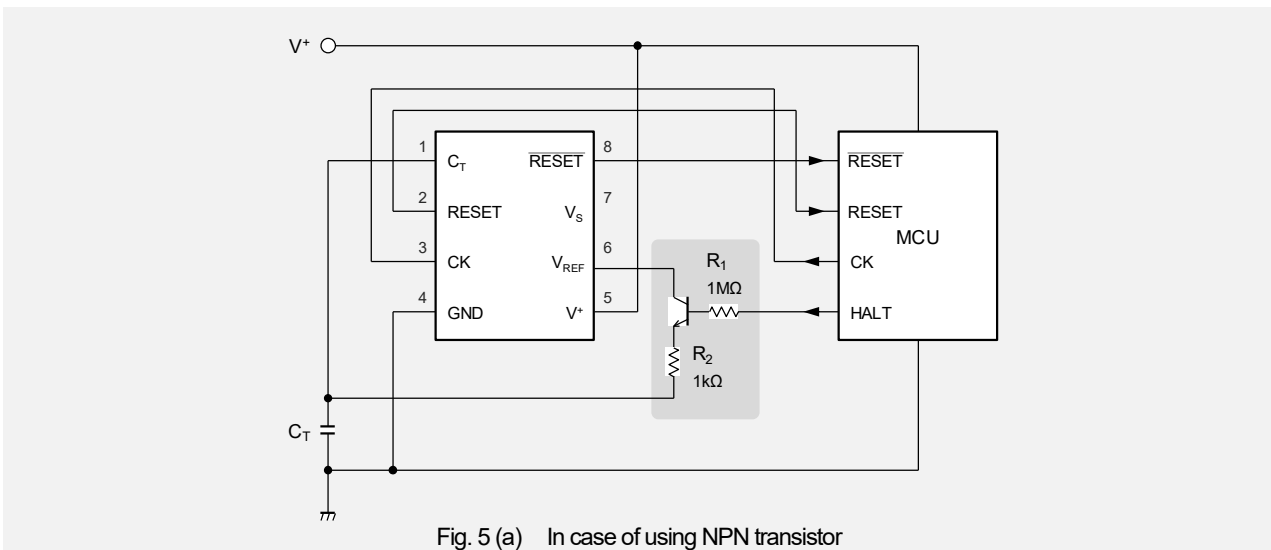
In Fig.5 (a) and (b), it should be set HALT="Low",  $\overline{\text{HALT}}$ ="High" during  $C_T$  charging at power-on reset operation. In this circuit, the watchdog timer operation is disabled by fixing  $C_T$  pin voltage with  $V_{REF}$ .

If it set HALT="High",  $\overline{\text{HALT}}$ ="Low" during  $C_T$  charging at power-on reset operation,  $C_T$  is not charged till the reset release voltage.

On the other hand, in Fig.5 (c) and (d), it can be used without considering the logic of HALT and  $\overline{\text{HALT}}$  at power on reset operation by applying a logic gate.

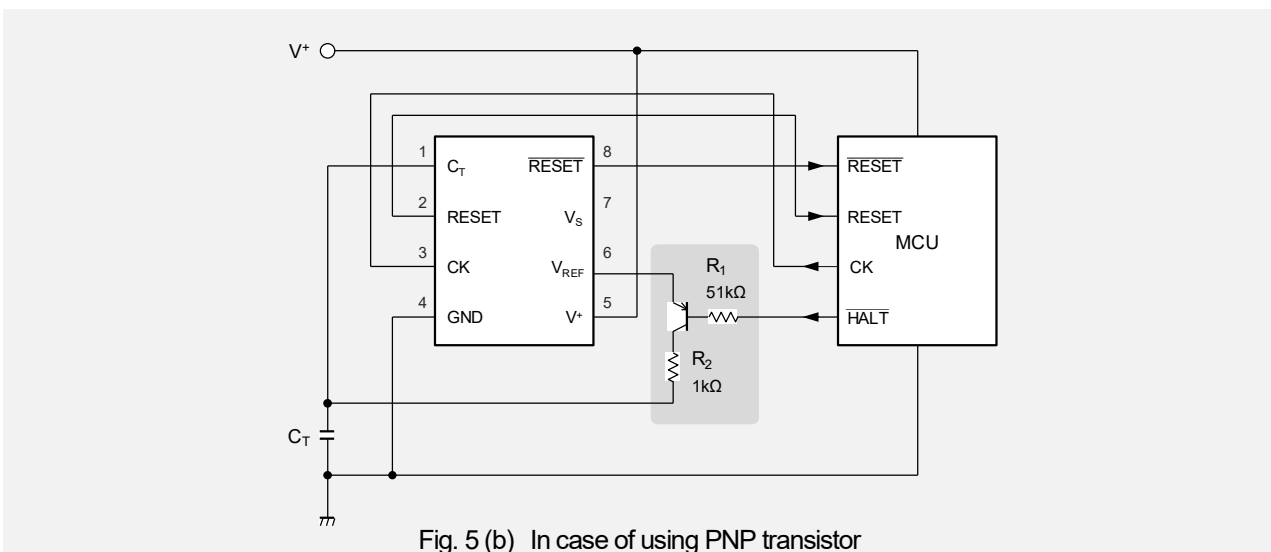
#### (a) In case of using NPN transistor

Disable the watchdog timer operation with HALT="High". Should be set HALT="Low" during power-on reset operation.



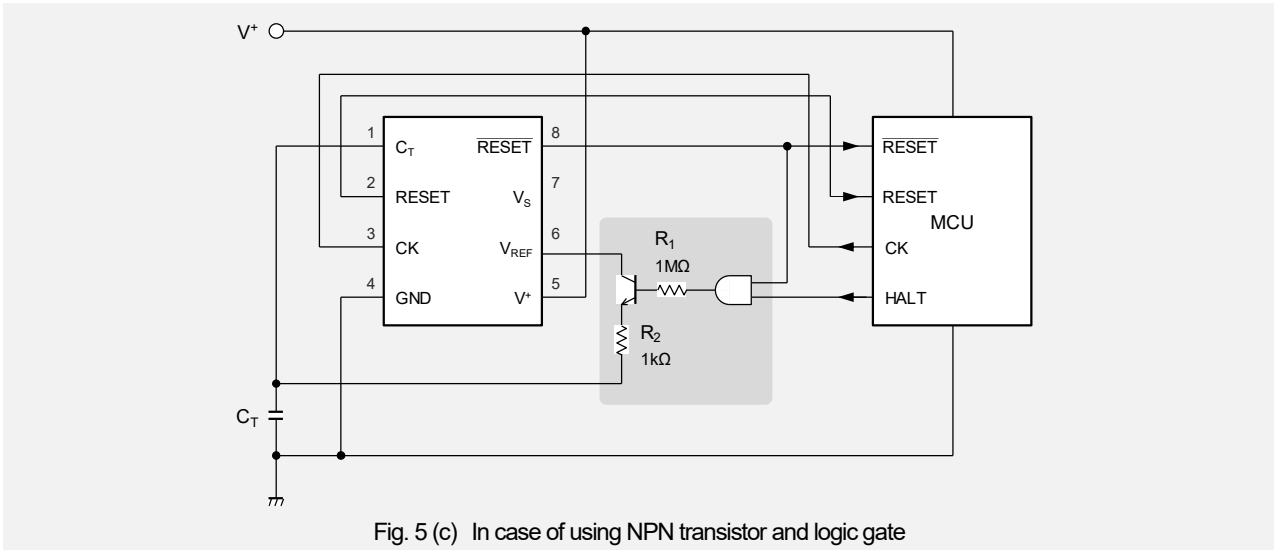
#### (b) In case of using PNP transistor

Disable the watchdog timer operation with HALT="Low". Should be set HALT="High" during power-on reset operation.

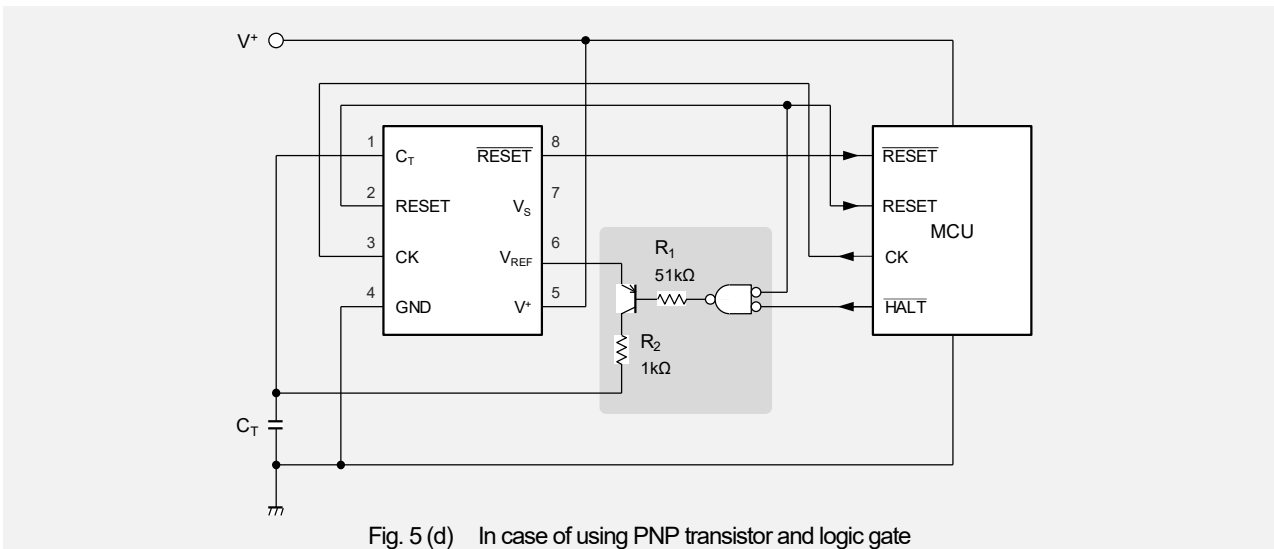


## Technical Information

- (c) In case of using NPN transistor and logic gate  
 Disable the watchdog timer operation with HALT="High".



- (d) In case of using PNP transistor and logic gate  
 Disable the watchdog timer operation with HALT="Low".



## Technical Information

### 6. Shortening of Reset Signal Hold Time $t_{PR}$

By inserting a diode between  $C_T$  and RESET pin and increasing  $C_T$  charge current, Reset Signal Hold Time  $t_{PR}$  can be shortened. The available output is only RESET. Estimated value of Reset Signal Hold Time  $t_{PR}$  is calculated as following formula.

Comparison of shortened circuit and standard circuit at  $C_T = 0.1 \mu\text{F}$  is shown in Tab. 2.

Reset Signal Hold Time (shortened circuit)	Reset Signal Hold Time (standard circuit)
$t_{PR} [\text{ms}] \approx 100 \times C_T [\mu\text{F}]$	$t_{PR} [\text{ms}] \approx 1000 \times C_T [\mu\text{F}]$
$t_{WD} [\text{ms}] \approx 100 \times C_T [\mu\text{F}]$	$t_{WD} [\text{ms}] \approx 100 \times C_T [\mu\text{F}]$
$t_{WR} [\text{ms}] \approx 16 \times C_T [\mu\text{F}]$	$t_{WR} [\text{ms}] \approx 20 \times C_T [\mu\text{F}]$

Tab. 2 Comparison of shortened circuit and standard circuit ( $C_T=0.1\mu\text{F}$ )

Item	Reset Signal Hold Time shortened circuit	Standard circuit
$t_{PR} \approx$	10 ms	100 ms
$t_{WD} \approx$	10 ms	10 ms
$t_{WR} \approx$	1.6 ms	2.0 ms

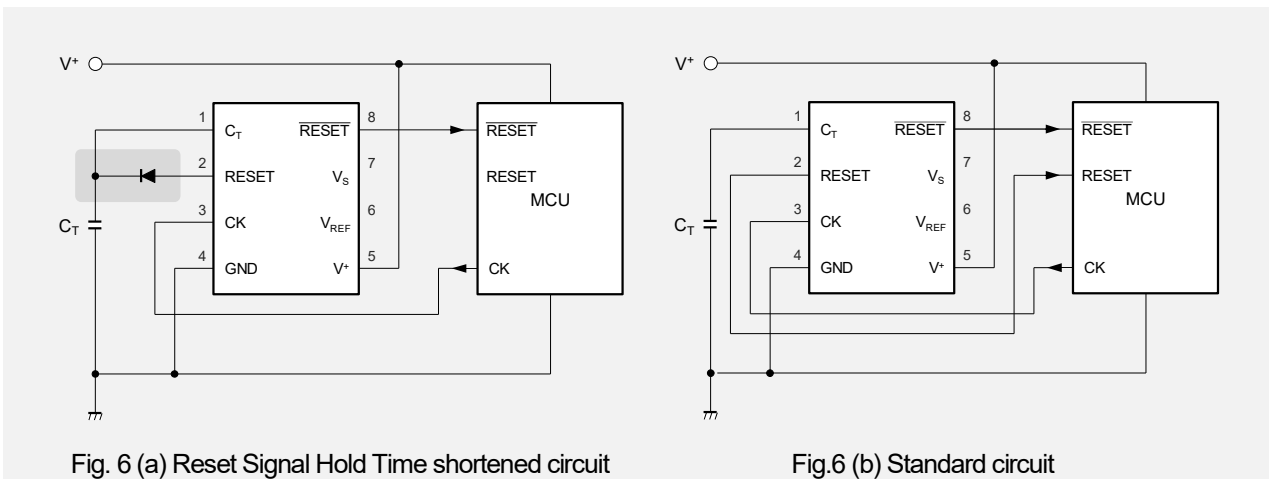


Fig. 6 (a) Reset Signal Hold Time shortened circuit

Fig.6 (b) Standard circuit

## Technical Information

### 7. Upper limit of Clock input frequency

Set the clock input frequency upper limit  $f_H$  from MCU by external filters made of  $C_2$  and  $R_2$ . When the clock frequency from the MCU exceeds  $f_H$ , reset signal is output. On the other hand, the lower limit is set by  $C_T$ .

When the MCU outputs a clock like the Fig. 7, if the clock cycle  $t_2$  is shorter, the clock interval  $t_1$  also becomes shorter. If the clock input to NJU2102A ( $C_2$  voltage) does not reach the CK Input Threshold Voltage  $V_{TH}$  (1.2V typ.), a reset signal output.

The  $t_1$  value can be calculated as following formula. However,  $t_3$  must be 3.0 $\mu$ s or more according to the minimum value of the CK Input Pulse width  $t_{CKW}$  and  $t_2$  must be 20 $\mu$ s or more according to the minimum value of the CK Input Cycle  $t_{CK}$ .

A setting example of  $C_2$ ,  $R_2$  is shown in Tab.3.

$$t_1 \approx C_2 R_2 \ln \left( \frac{V^+}{V^+ - 1.2} \right) = 0.3 C_2 R_2 \quad \text{However, } V^+ = 5 \text{ V, } t_3 \geq 3.0 \mu\text{s, } t_2 \geq 20 \mu\text{s}$$

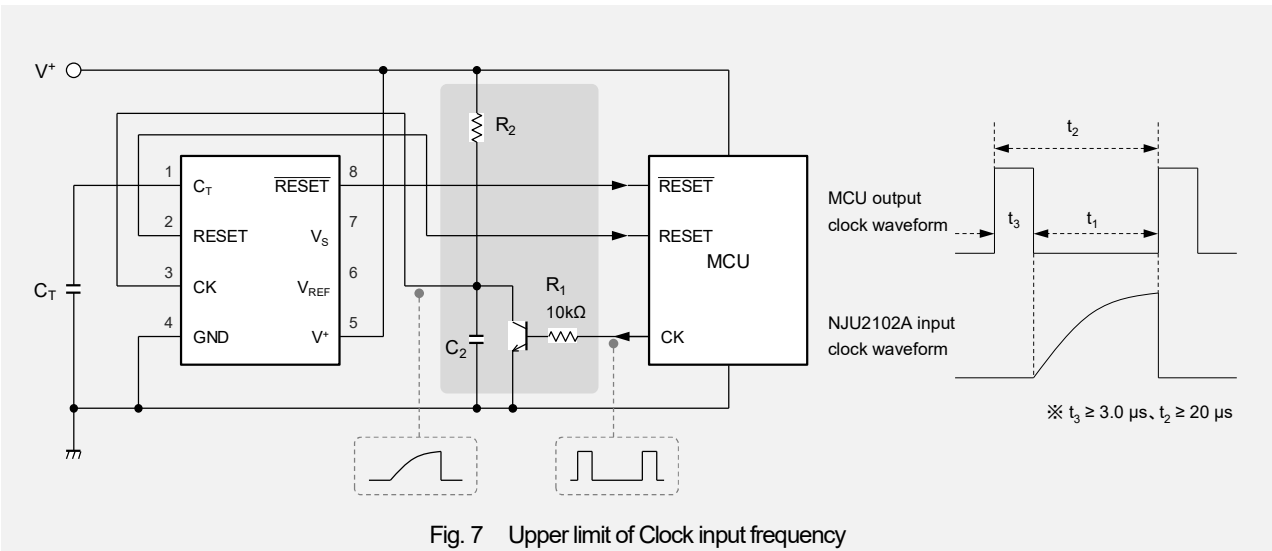
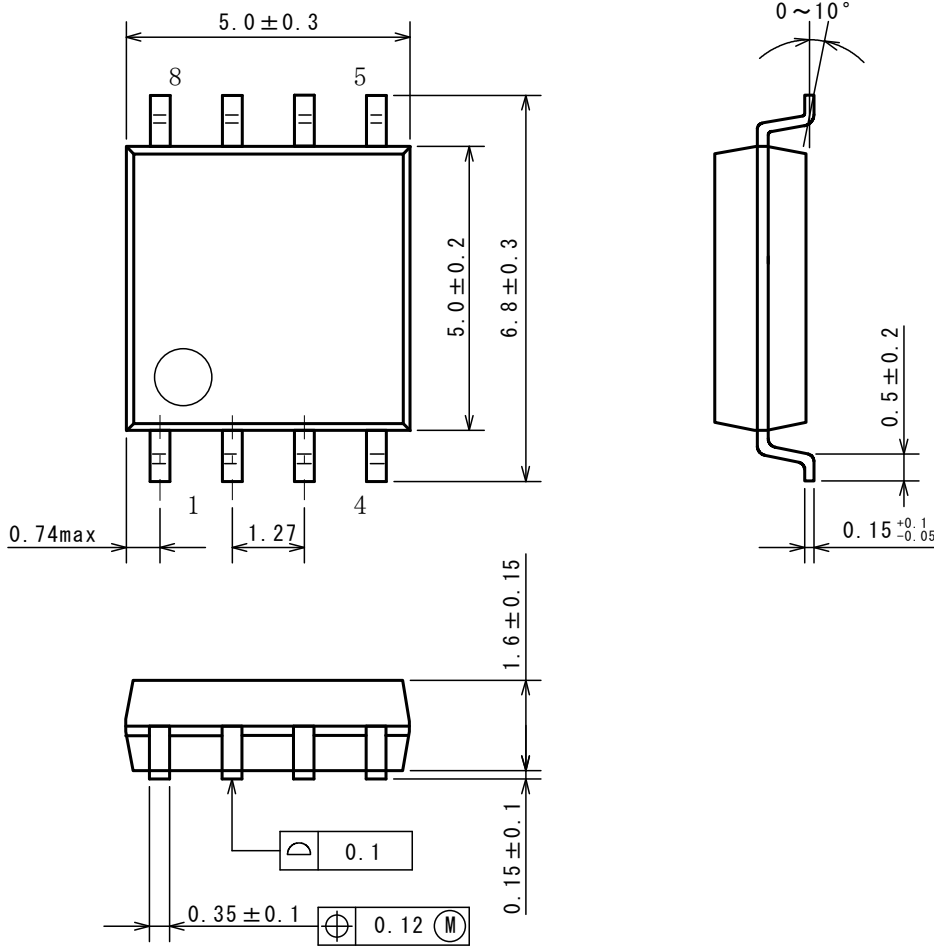


Fig. 7 Upper limit of Clock input frequency

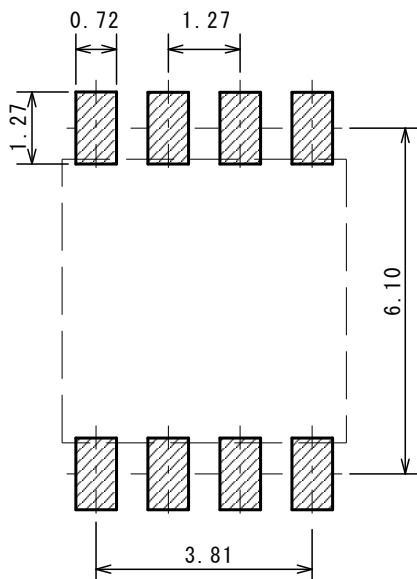
Tab. 3 Setting example of  $C_2$ ,  $R_2$

$C_2$	$R_2$	$t_1$
0.01 $\mu$ F	10 k $\Omega$	30 $\mu$ s
0.1 $\mu$ F	10 k $\Omega$	300 $\mu$ s

### ■PACKAGE DIMENSIONS



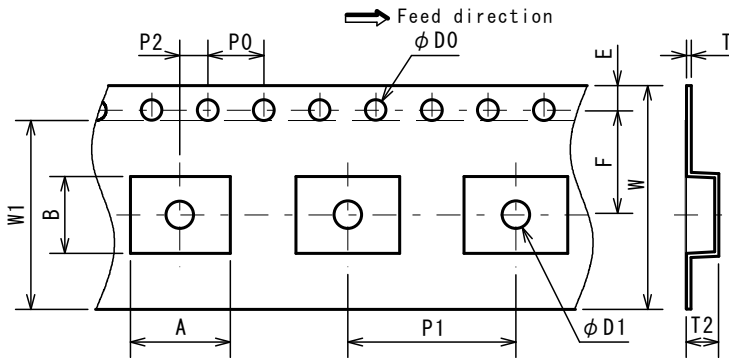
### ■EXAMPLE OF SOLDER PADS DIMENSIONS



### PACKING SPEC

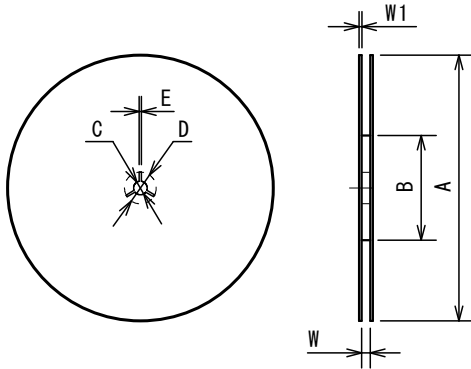
Unit: mm

#### TAPING DIMENSIONS



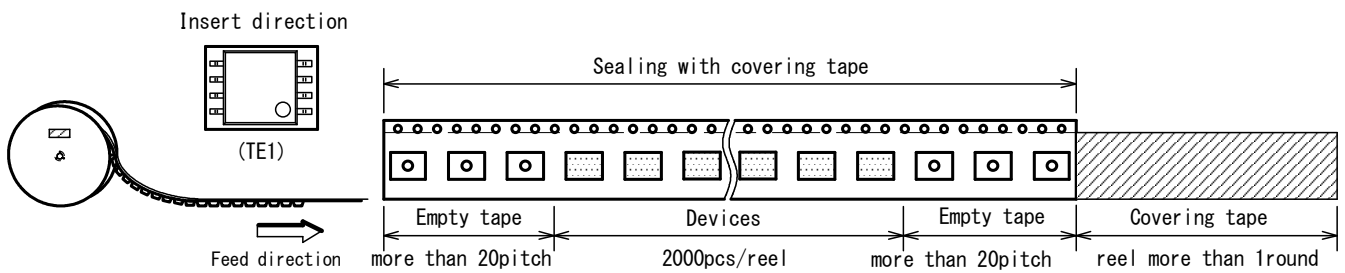
SYMBOL	DIMENSION	REMARKS
A	7.1	BOTTOM DIMENSION
B	5.4	BOTTOM DIMENSION
D0	1.55±0.05	
D1	2.05±0.1	
E	1.75±0.1	
F	7.5±0.1	
P0	4.0±0.1	
P1	12.0±0.1	
P2	2.0±0.1	
T	0.3±0.05	
T2	2.3	
W	16.0±0.3	
W1	13.5	THICKNESS 0.1max

#### REEL DIMENSIONS

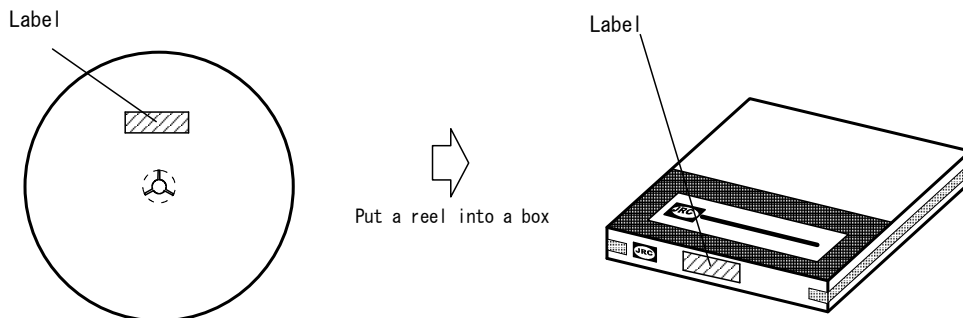


SYMBOL	DIMENSION
A	φ 330±2
B	φ 80±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	17.5±0.5
W1	2±0.2

#### TAPING STATE

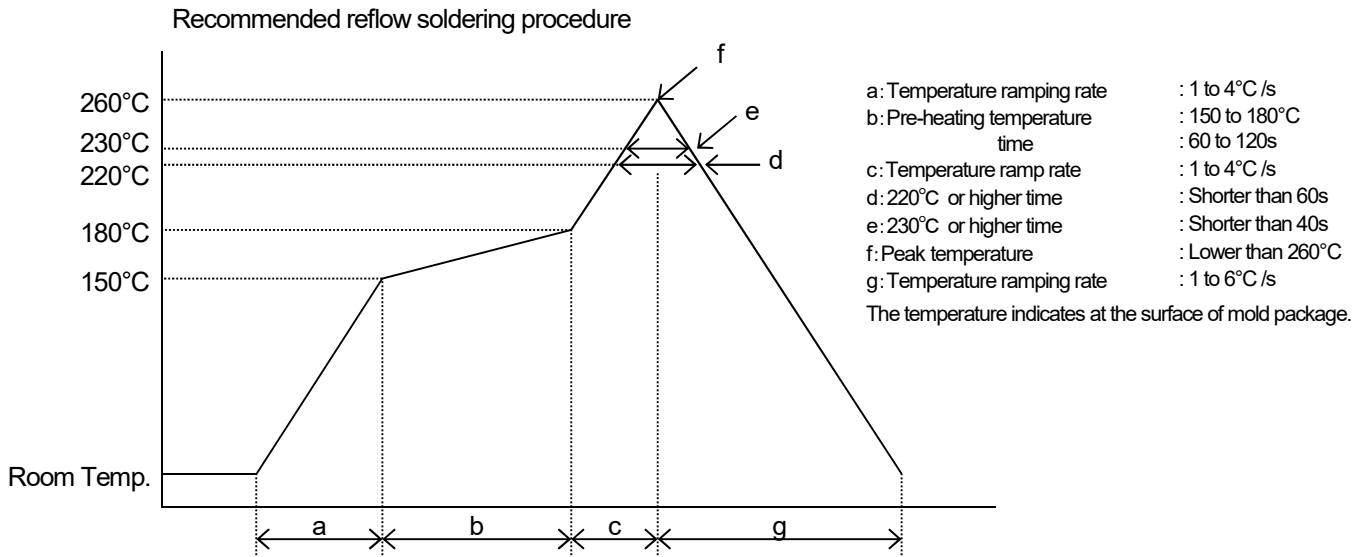


#### PACKING STATE



## RECOMMENDED MOUNTING METHOD

### INFRARED REFLOW SOLDERING METHOD



## ■REVISION HISTORY

Date	Revision	Changes
18.Sep.2018	1.0	New Release
08.Nov.2018	1.1	Add the Technical Information. (FUNCTION EXPLAMATION, OPERATION EXPLAMATION, APPLICATION EXAMPLE)



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