

nRF52840 Product Specification



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1. nRF52840 Product Specification

This Product Specification contains functional descriptions, register tables, and electrical specifications, and is organized into chapters based on the modules and peripherals that are available in this IC.

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Note: The HTML rendition of the Product Specification corresponds to the latest version only. All versions are available as PDF files.

Features:

- Bluetooth® 5, IEEE 802.15.4-2006, 2.4 GHz transceiver
 - -95 dBm sensitivity in 1 Mbps Bluetooth low energy mode
 - -103 dBm sensitivity in 125 kbps Bluetooth low energy mode (long range)
 - -20 to +8 dBm TX power, configurable in 4 dB steps
 - On-air compatible with nRF52, nRF51, nRF24L, and nRF24AP Series devices
 - Supported data rates:
 - Bluetooth 5 – 2 Mbps, 1 Mbps, 500 kbps, and 125 kbps
 - IEEE 802.15.4-2006 – 250 kbps
 - Proprietary 2.4 GHz – 2 Mbps, 1 Mbps
 - Single-ended antenna output (on-chip balun)
 - 128-bit AES/ECB/CCM/AAR co-processor (on-the-fly packet encryption)
 - 4.8 mA peak current in TX (0 dBm)
 - 4.6 mA peak current in RX
 - RSSI (1 dB resolution)
- Arm® Cortex®-M4 32-bit processor with FPU, 64 MHz
 - 212 EEMBC CoreMark® score running from flash memory
 - 52 µA/MHz running CoreMark from flash memory
 - Watchpoint and trace debug modules (DWT, ETM, and ITM)
- Flexible power management
 - 1.7 V to 5.5 V supply voltage range
 - On-chip DC/DC and LDO regulators with automated low current modes
 - 1.8 V to 3.3 V regulated supply for external components
 - Automated peripheral power management
 - Fast wake-up using 64 MHz internal oscillator
 - 0.4 µA at 3 V in System OFF mode, no RAM retention
 - 1.5 µA at 3 V in System ON mode, no RAM retention, wake on RTC
- 1 MB flash and 256 kB RAM
- Advanced on-chip interfaces
 - USB 2.0 full speed (12 Mbps) controller
 - QSPI 32 MHz interface
 - High-speed 32 MHz SPI
 - Type 2 near field communication (NFC-A) tag with wake-on field
 - Touch-to-pair support
 - Programmable peripheral interconnect (PPI)

Features:

- Serial wire debug (SWD)
- Rich set of security features
 - Arm TrustZone® CryptoCell™ 310 security subsystem
 - NIST SP800-90A and SP800-90B compliant random number generator
 - AES-128 – ECB, CBC, CMAC/CBC-MAC, CTR, CCM/CCM*
 - Chacha20/Poly1305 AEAD supporting 128- and 256-bit key size
 - SHA-1 and SHA-2 up to 256 bit
 - Keyed-hash message authentication code (HMAC)
 - RSA up to 2048-bit key size
 - SRP up to 3072-bit key size
 - ECC support for most used curves, including P-256 (secp256r1) and Ed25519/Curve25519
 - Application key management using derived key model
 - Secure boot ready
 - Flash access control list (ACL)
 - Root-of-trust (RoT)
 - Debug control and configuration
 - Access port protection (CTRL-AP)
 - Secure erase
- 48 general purpose I/O pins
- EasyDMA automated data transfer between memory and peripherals
- Nordic SoftDevice ready with support for concurrent multiprotocol
- 12-bit, 200 ksps ADC – 8 configurable channels with programmable gain
- 64 level comparator
- 15 level low-power comparator with wake-up from System OFF mode
- Temperature sensor
- Four 4 channel pulse width modulator (PWM) units with EasyDMA
- Audio peripherals – I²S, digital microphone interface (PDM)
- Five 32-bit timers with counter mode
- Up to four SPI masters/three SPI slaves with EasyDMA
- Up to two I²C compatible two-wire master/slave
- Two UART (CTS/RTS) with EasyDMA
- Quadrature decoder (QDEC)
- Three real-time counters (RTC)
- Single crystal operation
- Package variants
 - aQFN73™ package, 7 x 7 mm
 - QFN48 package, 6 x 6 mm
 - WLCSP package, 3.544 x 3.607 mm

Applications:

- Advanced computer peripherals and I/O devices
 - Mouse
 - Keyboard
 - Multi-touch trackpad
- Advanced wearable devices
 - Health/fitness sensors and monitoring devices
 - Wireless payment enabled devices
- Internet of things (IoT)
 - Smart home sensors and controllers
 - Industrial IoT sensors and controllers
- Interactive entertainment devices
 - Remote controls
 - Gaming controllers

Revision history

About this document This document is organized into chapters that are based on the modules and peripherals available in the

IC.

Block diagram This block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

Recommended operating conditions The operating conditions are the physical parameters that the chip can operate within.

Absolute maximum ratings

Ordering information This chapter contains information on device marking, ordering codes, and container sizes.

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