

Product Overview

The NSi1042 is an isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSi1042 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSi1042 device is safety certified by UL1577 support 5kV_{rms} insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSi1042 is up to 5Mbps, and it can support at least 110 CAN nodes. The NSi1042 provides thermal protection and transmit data dominant time out function.

Key Features

- Fully compatible with the ISO11898-2 standard
- Up to 5000Vrms Insulation voltage
- Power supply voltage
VDD1: 2.5V to 5.5V
VDD2: 4.5V to 5.5V
- Bus fault protection of -70V to +70V
- Transmit data (TXD) dominant time out function
- Over current and over temperature protection
- Date rate: up to 5Mbps
- High CMTI: 150kV/us
- Low loop delay: <220ns
- High system level EMC performance:
Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40°C~125°C
- RoHS-compliant packages:
SOW8
SOW16

Safety Regulatory Approvals

- UL recognition: up to 5000Vrms for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Isolated CAN Bus
- Telecom

Device Information

Part Number	Package	Body Size
NSi1042-DSWVR	SOW8	5.85mm × 7.50mm
NSi1042-DSWR	SOW16	10.30mm × 7.50mm
NSi1052-DSWR	SOW16	10.30mm × 7.50mm

Functional Block Diagrams

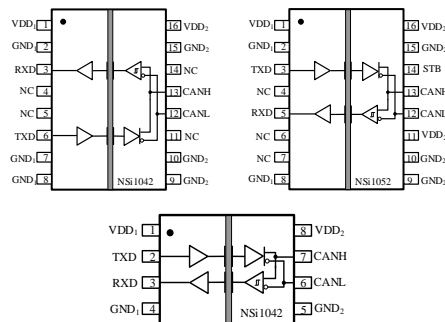


Figure 1. NSi1042 Block Diagram

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1. Pin Configuration and Functions

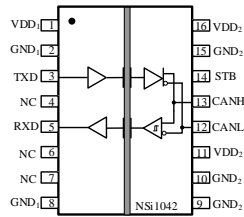


Figure 1.1 NSI1052-DSWR Package

Table1.1 NSI1052-DSWR Pin Configuration and Description

NSI1052-DSWR PIN NO.	SYMBOL	FUNCTION
1	VDD ₁	Power Supply for Side 1
2	GND ₁	Ground 1, the ground reference for Isolator Side 1
3	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
4	NC	No Connection
5	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
6	NC	No Connection
7	NC	No Connection
8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	GND ₂	Ground 2, the ground reference for Isolator Bus Side
10	GND ₂	Ground 2, the ground reference for Isolator Bus Side
11	VDD ₂	Power supply for Bus Side, this pin must be connected externally to PIN16
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	STB	Standby mode control input
15	GND ₂	Ground 2, the ground reference for Isolator Bus Side
16	VDD ₂	Power supply for Bus Side, this pin must be connected externally to PIN11

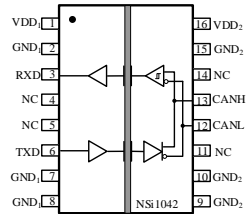


Figure 1.1 NSI1042-DSWR Package

Table1.2 NSI1042-DSWR Pin Configuration and Description

NSI1042-DSWR PIN NO.	SYMBOL	FUNCTION
1	VDD ₁	Power Supply for Side 1
2	GND ₁	Ground 1, the ground reference for Isolator Side 1
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	NC	No Connection
5	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
6	NC	No Connection
7	NC	No Connection
8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	GND ₂	Ground 2, the ground reference for Isolator Bus Side
10	GND ₂	Ground 2, the ground reference for Isolator Bus Side
11	VDD ₂	Power supply for Bus Side, this pin must be connected externally to PIN16
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	NC	No Connection
15	GND ₂	Ground 2, the ground reference for Isolator Bus Side
16	VDD ₂	Power supply for Bus Side, this pin must be connected externally to PIN11

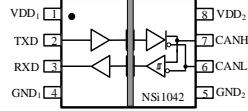


Figure 1.2 NSI1042-DSWVR Package

Table 1.2 NSI1042-DSWVR Pin Configuration and Description

NSI1042-DSWVR PIN NO.	SYMBOL	FUNCTION
1	VDD ₁	Power Supply for Side 1
2	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	GND ₁	Ground 1, the ground reference for Isolator Side 1
5	GND ₂	Ground 2, the ground reference for Isolator Bus Side
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	VDD ₂	Power supply for Bus Side

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD ₁ , VDD ₂	-0.5		6.5	V	
Maximum Input Voltage	V _{TXD}	-0.4		VDD ₁ +0.4	V	
Maximum BUS Pin Voltage	V _{CANH} , V _{CANL}	-70		+70	V	
Output current	I _o	-15		15	mA	
Operating Temperature	T _{opr}	-40		125	°C	
Storage Temperature	T _{stg}	-40		150	°C	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply voltage, controller side	V_{CC1}	2.5		5.5	V	
Supply voltage, bus side	V_{CC2}	4.5	5	5.5	V	
Voltage at bus pins (separately or common mode)	V_I or V_{IC}	-30		30	V	
High-level input voltage	V_{IH}	2		5.5	V	TXD
Low-level input voltage	V_{IL}	0		0.8	V	TXD
High-level output current	I_{OH}	-70			mA	Driver
		-4			mA	Receiver
Low-level output current	I_{OL}			70	mA	Driver
				4	mA	Receiver
Ambient Temperature	T_A	-40		125	°C	
Junction temperature	T_J	-40		150	°C	

4. Thermal Information

Parameters	Symbol	SOW8	SOW16	Unit
Junction-to-ambient thermal resistance	θ_{JA}	100	69.9	°C/W
Junction-to-case(top) thermal resistance	$\theta_{JC(top)}$	40.8	31.8	
Junction-to-board thermal resistance	θ_{JB}	51.8	29	

批注 [A1]: 热阻修改

5. Specifications

5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	VDD ₁	2.5		5.5	V	
	VDD ₂	4.5	5	5.5	V	
Logic side supply current	IDD ₁		1.97	3.50	mA	VDD ₁ =3.3V, TXD=0
			0.97	2.00	mA	VDD ₁ =3.3V, TXD=VCC1
			2.02	3.50	mA	VDD ₁ =5V, TXD=0
			1.02	2.00	mA	VDD ₁ =5V, TXD=VCC1
Bus side supply current	IDD ₂		46	70	mA	VI=0V, R _{Load} =60Ω
			4.45	10	mA	VI=VDD ₂
Thermal-Shutdown Threshold	T _{TS}	155	165	180	°C	
Common Mode Transient Immunity	CMTI	±100	±150		kV/us	
Logic Side						
High level input voltage	V _{IH}	2			V	TXD pin
Low level input voltage	V _{IL}			0.8	V	TXD pin
High level input current	I _{IH}			10	uA	TXD pin
Low level input current	I _{IL}	-10			uA	TXD pin
Output Voltage High	V _{OH}	VDD ₁ -0.4			V	I _{OH} = -4mA, RXD pin
Output Voltage Low	V _{OL}			0.4	V	I _{OL} = 4mA, RXD pin
Input Capacitance	C _{IN}		2		pF	TXD pin
Driver						
CANH output voltage (Dominant)	V _{OH(D)}	2.8	3.44	4.5	V	TXD=0V, R _{Load} =60Ω
CANL output voltage (Dominant)	V _{OL(D)}	0.8	1.33	2.25	V	TXD=0V, R _{Load} =60Ω
CAN bus output voltage (Recessive)	V _{O(R)}	2	0.5*VDD2	3	V	TXD=VDD1, R _{Load} =60Ω
Differential output voltage (Dominant)	V _{OD(D)}	1.5		3	V	VCC=5V, TXD=0, R _{Load} =60Ω, see Figure 5.1
Differential output voltage (Recessive)	V _{OD(R)}	-0.05		0.05	V	VCC=5V, TXD=VIO, R _{Load} =60Ω, see Figure 5.1

		-0.1		0.1	V	VCC=5V, TXD=V _{IO} , NO Load, see Figure 5.1
Dominant short-circuit output current	I _{O(sc)dom}	-100		-40	mA	TXD=0V, t < t _{to(dom)TXD} , V _{CANH} = -30V
		40		100	mA	TXD=0V, t < t _{to(dom)TXD} , V _{CANL} = 30V
Recessive short-circuit output current	I _{O(sc)rec}	-5		5	mA	Normal/Silent mode; V _{TXD} = VDD1; V _{CANH} = V _{CANL} = -27 V to +30 V
Receiver						
Positive-going bus input threshold voltage	V _{IT+}		750	900	mV	
Negative-going bus input threshold voltage	V _{IT-}	500	650		mV	
Hysteresis voltage	V _{HYS}		100		mV	
Power-off (unpowered) bus input leakage current	I _{IOFF(LKG)}	-5		5	uA	V _{CANH} /V _{CANL} = 5V, VCC = 0V, VIO = 0V
Input capacitance to ground	C _I		13		pF	CANH or CANL
Differential input	C _{ID}		5		pF	
Differential input resistance	R _{ID}	30		80	kΩ	
Input resistance	R _{IN}	15	30	40	kΩ	
Input resistance matching	R _{I_{match}}	-3		+3	%	CANH=CANL
Common-mode voltage range	V _{COM}	-30		+30	V	

5.2. SWITCHING Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Loop delay1	T_{loop1}		120	220	ns	Driver input to receiver output, Recessive to Dominant, see Figure 5.7
Loop delay2	T_{loop2}		100	220	ns	Driver input to receiver output, Dominant to Recessive, see Figure 5.7
transmitted recessive bit width	$t_{bit(bus)}$	435		530	ns	$t_{bit(TXD)} = 500$ ns
		155		210	ns	$t_{bit(TXD)} = 200$ ns
bit time on pin RXD	$t_{bit(RXD)}$	400		550	ns	$t_{bit(TXD)} = 500$ ns
		120		220	ns	$t_{bit(TXD)} = 200$ ns
Driver						
Propagation delay time, recessive-to- dominant output	t_{PLH}		100		ns	see Figure 5.4
Propagation delay time, dominant-to- recessive output	t_{PHL}		80		ns	see Figure 5.4
Differential output signal rise time	t_r		42		ns	see Figure 5.4
Differential output signal fall time	t_f		32		ns	see Figure 5.4
Bus dominant time-out time	t_{TXD_DTO}	800	2000	4000	us	see Figure 5.8
Receiver						
Propagation delay time, low-to-high-level output	t_{PLH}		50		ns	see Figure 5.6
Propagation delay time, high-to-low-level output	t_{PHL}		30		ns	see Figure 5.6
RXD signal rise time	t_r		3		ns	see Figure 5.6
RXD signal fall time	t_f		3		ns	see Figure 5.6

5.3. Parameter Measurement Information

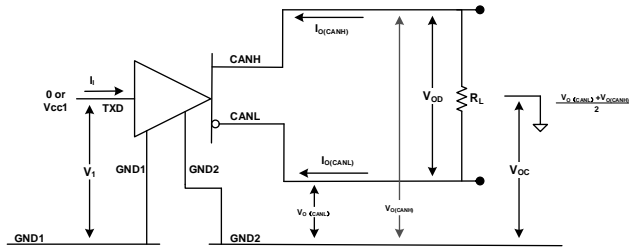


Figure 5.1. Driver Voltage, Current and Test Definitions

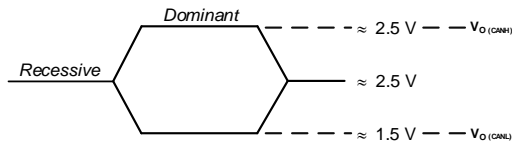


Figure 5.2. Bus Logic State Voltage Definitions

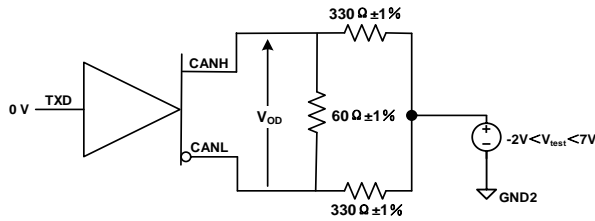
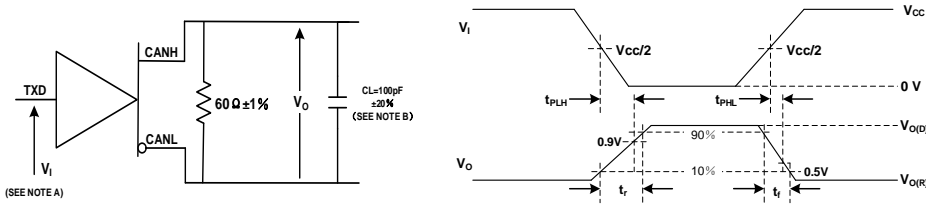


Figure 5.3. Driver VOD With Common-Mode Loading Test Circuit



- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, ZO = 50 Ω .
- B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 5.4. Driver Test Circuit and Voltage Waveform

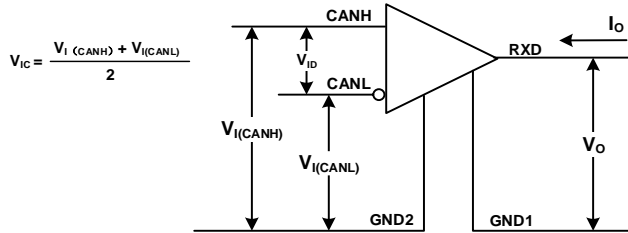
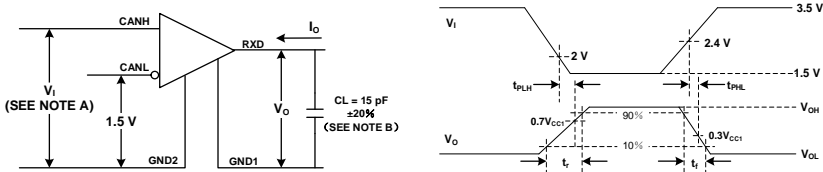


Figure 5.5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_0 = 50 \Omega$.
 B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5.6. Receiver Test Circuit and Voltage Waveform

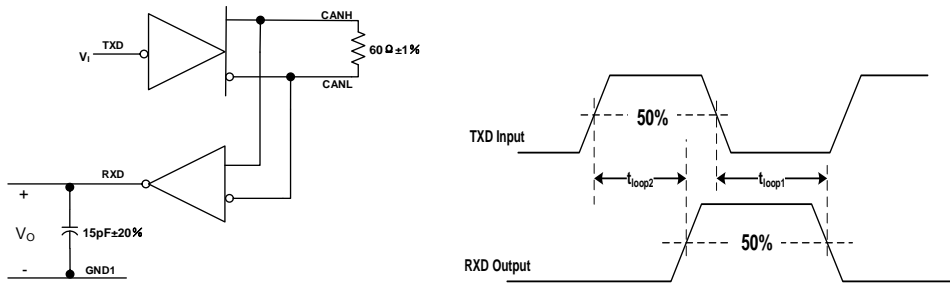
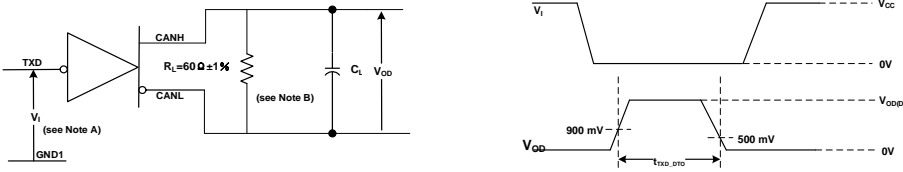


Figure 5.7. t_{LOOP} Test Circuit and Voltage Waveform



- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 125 \text{ kHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_0 = 50 \Omega$.
- B. C_L includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 5.8. Dominant Time-out Test Circuit and Voltage Waveform

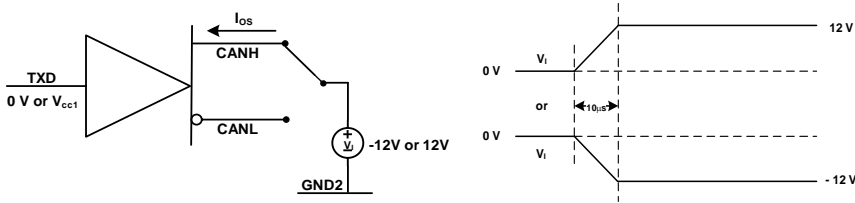


Figure 5.9. Driver Short-Circuit Current Test Circuit and Waveform

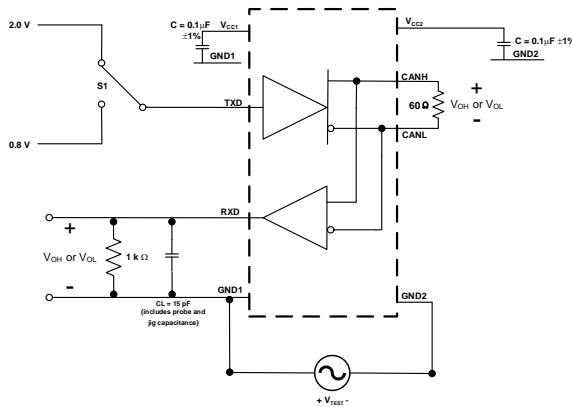


Figure 5.10. Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Description	Test Condition	Symbol	Value		Unit
			SOW8	SOW16	
Min. External Air Gap (Clearance)		CLR	8	8	mm
Min. External Tracking (Creepage)		CPG	8	8	mm
Distance through the Insulation		DTI	32		um
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>600		V
Material Group	IEC 60112		I		
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage ≤ 150Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 600Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 1000Vrms			I to III	I to III	
Insulation Specification per DIN VDE V 0884-11:2017-01 ¹⁾					
Climatic Category			40/125/21		
Pollution Degree	per DIN VDE 0110, Table 1		2		
Maximum Working Isolation Voltage	AC voltage	V _{IOWM}	1500	1500	V _{RMS}
	DC voltage		2121	2121	V _{DC}
Maximum Repetitive Isolation Voltage		V _{IORM}	2121	2121	V _{peak}
Input to Output Test Voltage, Method B1	V _{ini, b} = V _{IOTM} , V _{pd(m)} = V _{IORM} × 1.875, t _{ni} = t _m = 1 sec, q _{pd} ≤ 5 pC, 100% production test	V _{pd(m)}	3977	3977	V _{peak}
Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	V _{ini, a} = V _{IOTM} , V _{pd(m)} = V _{IORM} × 1.6, t _{ni} = 60 sec, t _m = 10 sec, q _{pd} ≤ 5 pC	V _{pd(m)}	3394	3394	V _{peak}
Input to Output Test Voltage, Method A. After Input and Output Safety Test Subgroup 2 and Subgroup 3	V _{ini, a} = V _{IOTM} , V _{pd(m)} = V _{IORM} × 1.2, t _{ni} = 60 sec, t _m = 10 sec, q _{pd} ≤ 5 pC	V _{pd(m)}	2545	2545	V _{peak}
Maximum Transient Isolation Voltage	t = 60 sec	V _{IOTM}	8000	8000	V _{peak}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, V _{TEST} = 1.6 × V _{IOSM}		6250	6250	V _{peak}
Isolation Resistance	V _{IO} = 500 V, T _{amb} = T _S	R _{IO}	>10 ⁹		Ω

Description	Test Condition	Symbol	Value	Unit
	$V_{IO} = 500 \text{ V}, 100 \text{ }^\circ\text{C} \leq T_{amb} \leq 125 \text{ }^\circ\text{C}$		$>10^{11}$	Ω
Isolation Capacitance	$f = 1\text{MHz}$	C_{IO}	1.2	pF
Insulation Specification per UL1577				
Withstand Isolation Voltage	$V_{TEST} = 1.2 \times V_{ISO}, t = 1 \text{ sec}, 100\% \text{ production test}$	V_{ISO}	5000	V_{rms}

1) This coupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

6.2. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSI1042-DSWVR

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 100 \text{ }^\circ\text{C/W}, T_J = 150 \text{ }^\circ\text{C}, T_A = 25 \text{ }^\circ\text{C}$	1250	mW
Safety Supply Current	$R_{\theta JA} = 100 \text{ }^\circ\text{C/W}, V_i = 5\text{V}, T_J = 150 \text{ }^\circ\text{C}, T_A = 25 \text{ }^\circ\text{C}$	250	mA
Safety Temperature ²⁾		150	$^\circ\text{C}$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8(300mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

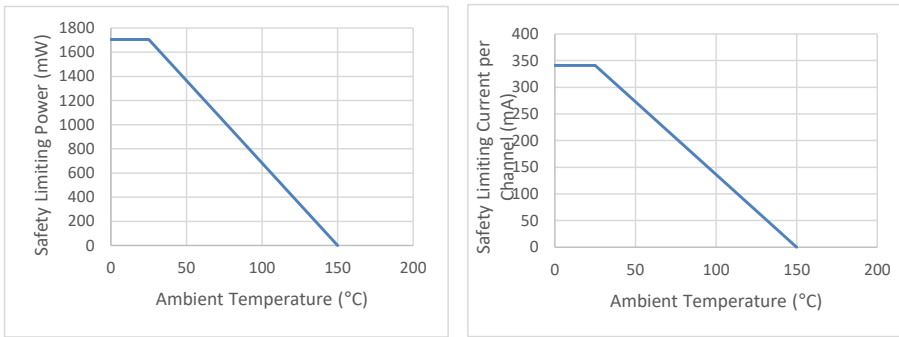


Figure 6.1 NSI1042-DSWVR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

批注 [A2]: 已按新热阻更新参数, 但图片还未更新

批注 [A3]: 需按新参数修改图片

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSI1042-DSWR/NSI1052-DSWR

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 69.9 \text{ }^\circ\text{C/W}$, $T_J = 150 \text{ }^\circ\text{C}$, $T_A = 25 \text{ }^\circ\text{C}$	1788	mW
Safety Supply Current	$R_{\theta JA} = 69.9 \text{ }^\circ\text{C/W}$, $V_I = 5\text{V}$, $T_J = 150 \text{ }^\circ\text{C}$, $T_A = 25 \text{ }^\circ\text{C}$	357	mA
Safety Temperature ²⁾		150	$^\circ\text{C}$

- 3) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16(300mil) package (*Thermal Information Table*) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 4) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

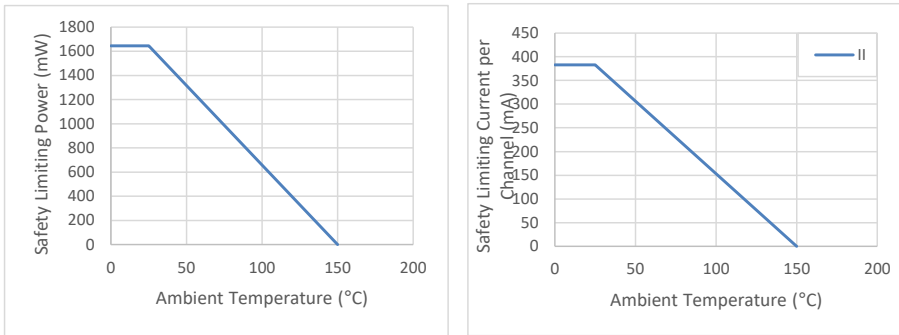


Figure 6.2 NSI1042-DSWR/NSI1052-DSWR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

批注 [A4]: 需按新参数修改图片

6.3. Regulatory information

The NSI1042/NSI1052 is approved by the organizations listed in table.

	CUL	VDE	CQC
UL 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01 ²	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V _{rms} Isolation voltage	Single Protection, 5000V _{rms} Isolation voltage	Reinforced Insulation 2121V _{peak} , $V_{IOSM}=6250\text{peak}$	Basic insulation
File (pending)	File (pending)	File (pending)	File (pending)

7. Function Description

The NSi1042 is an isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSi1042 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSi1042 device is safety certified by UL1577 support $5kV_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSi1042 is up to 5Mbps, and it can support at least 110 CAN nodes. The NSi1042 provides thermal protection and transmit data dominant time out function.

7.1. Device Functional Modes

Table 7.1. Driver Function Table

TXD	CANH	CANL	BUS STATE
L	H	L	Dominant
H	Z	Z	Recessive
Open	Z	Z	Recessive

¹ H= high level; L=low level; Z= common mode(recessive) bias to $V_{cc}/2$

Table 7.2. Receiver Function Table

$V_{ID}=CANH-CANL$	RXD	BUS STATE
$V_{ID} \geq 0.9V$	L	Dominant
$0.5 < V_{ID} < 0.9V$	X	Uncertain
$V_{ID} \leq 0.5V$	H	Recessive
Open	H	Recessive

¹ H= high level; L=low level; X= uncertain

7.2. Standby mode

The NSI1042 cannot transmit or receive regular CAN messages in Standby mode. Only the isolator and low-power CAN receiver are active, monitoring the bus lines for activity. The bus wake-up filter ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)bus}$ are reflected on the RXD pin. To reduce current consumption, the CAN bus is terminated to GND and not biased to $V_{DD2}/2$ as in Normal mode. Standby mode is selected by setting pin STB HIGH. An internal pull-up ensures that Standby mode is selected by default when pin STB is not connected.

In Standby mode:

- The CAN transmitter is off
- The normal CAN receiver is off
- The low-power CAN receiver is active
- CANH and CANL are biased to GND
- The signal received at the low-power CAN receiver is reflected on pin RXD

The isolation function of the NSI1042 is not disabled in Standby mode. Overall quiescent current is not reduced significantly in this mode. The NSI1042 is not designed to support CAN bus wake-up functionality with very low quiescent currents.

7.3. TXD dominant time-out function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTC}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

7.4. Bus dominant time-out function

In Standby mode, a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than $t_{to(dom)bus}$, the RXD pin is forced HIGH. This prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

7.5. Current Protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

7.6. Over Temperature Protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{TS} , the output drivers will be disabled until the virtual junction temperature becomes lower than T_{TS} and TXD becomes recessive again.

By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

8. Application Note

8.1. TYPICAL APPLICATION

The NSI1042 requires a 0.1 μ F bypass capacitors between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. The figure 8.1 is the basic schematic of NSI1042.

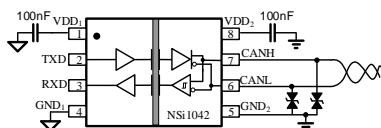


Figure 8.1 Basic schematic of NSI1042

8.2. PCB Layout

The recommended PCB layout shown below.

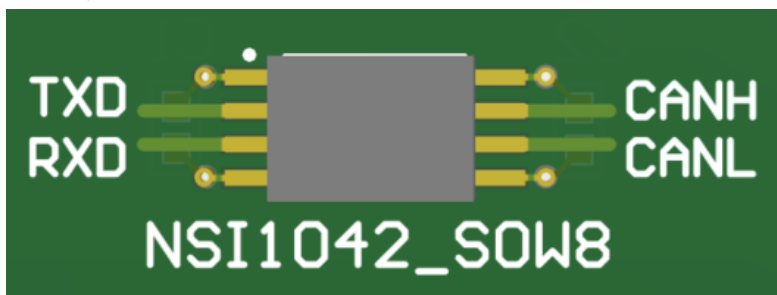


Figure 8.2 Recommended PCB Layout — Top Layer



Figure 8.3 Recommended PCB Layout — Bottom Layer

9. Package Information

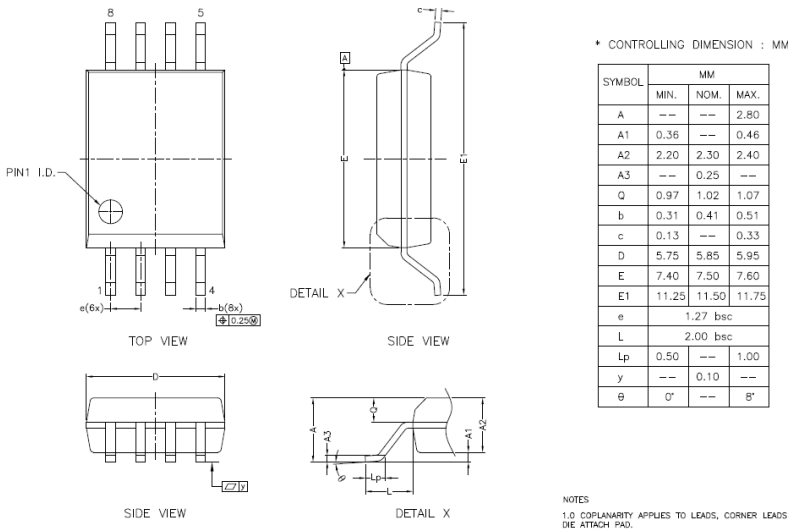


Figure 9.1 SOW8 Package Shape and Dimension in millimeters

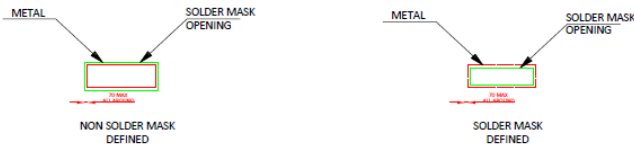
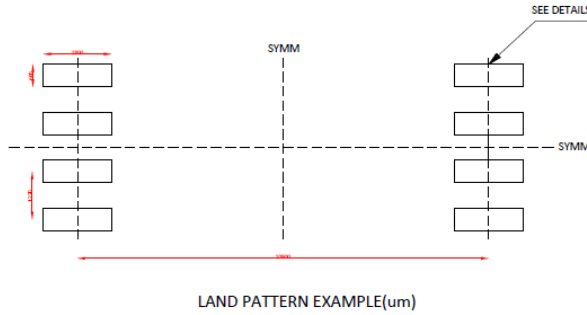


Figure 9.2 SOW8 Package Board Layout Example

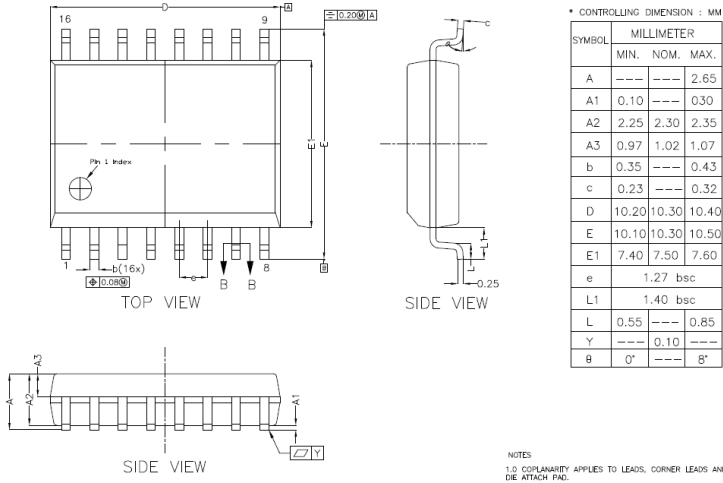


Figure 9.3 SOW16 Package Shape and Dimension in millimeters

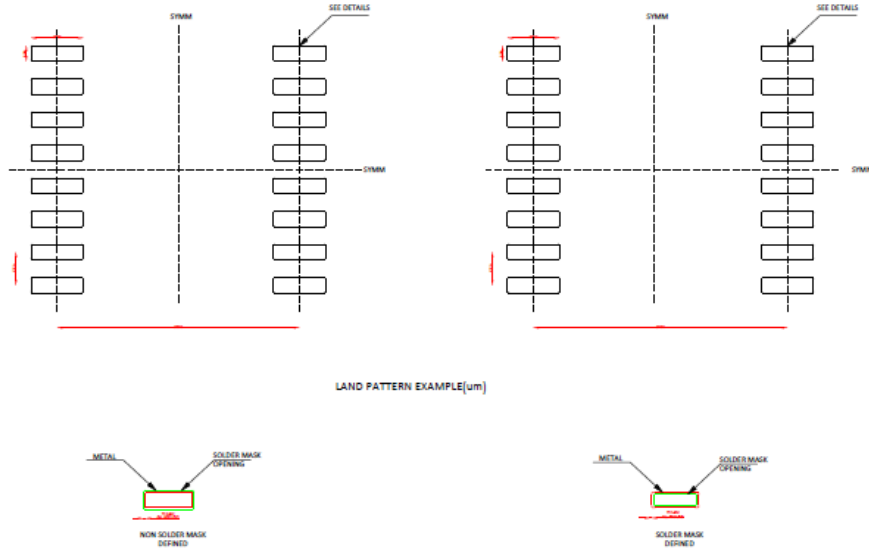


Figure 9.4 SOW16 Package Board Layout Example

10. Order Information

Part Number	Isolation Rating (kV)	Max Data Rate (Mbps)	Temperature	MSL	Package Type	Package Drawing	SPQ
NSI1042-DSWVR	5	5 (CAN FD)	-40 to 125°C	3	SOP8 (300mil)	SOW8	1000
NSI1042-DSWR	5	5 (CAN FD)	-40 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSI1052-DSWR	5	5 (CAN FD)	-40 to 125°C	2	SOP16 (300mil)	SOW16	1000

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI1042	Click here	Click here	Click here	Click here

12. Tape And Reel Information

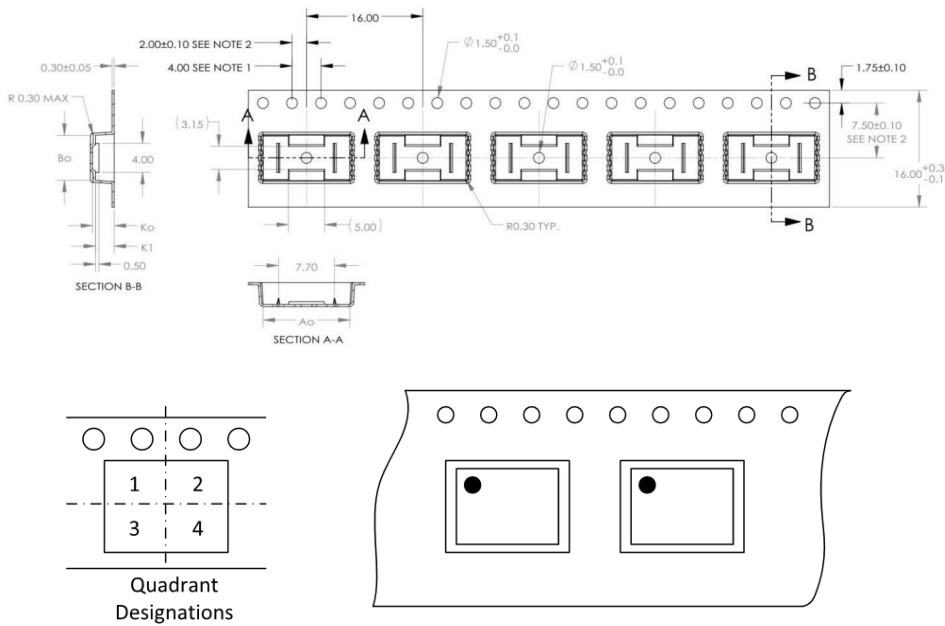
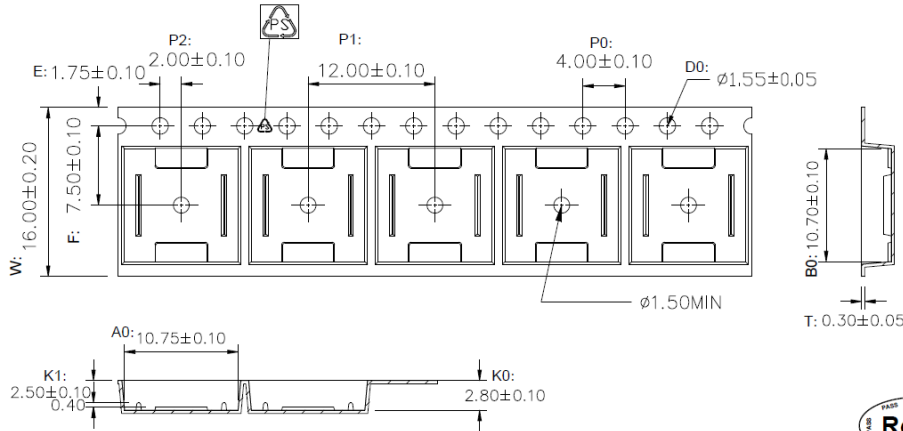


Figure 12.1 Tape and Reel Information of SOW8



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30 ± 0.05 mm.
6. Packing length per 22" reel : 378 Meters. (復卷 N=122)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : $10^5 \sim 10^{10} \Omega/\square$



W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

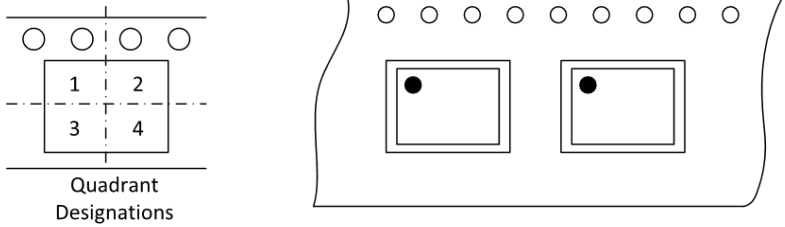


Figure 12.2 Tape and Reel Information of SOW16

13. Revision History

Revision	Description	Date
1.0	Initial version	2021/12/23

单击下面可查看定价，库存，交付和生命周期等信息

[>>Novosense \(纳芯微\)](#)