NOVOSENSE
纳芯微电子

NCA9306

Dual Bidirectional I2C Bus and SMBus Voltage-Level Translator

Datasheet (EN) 1.1

Product Overview

The NCA9306 device is a dual bidirectional I^2C and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.2V to 3.3V V_{REF1} and 1.8V to 5.5V V_{REF2}.

The NCA9306 device allows bidirectional voltage translations between 1.2 V and 5 V, without the use of a direction pin. The low ON-state resistance (R_{ON}) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is off, and a high-impedance state exists between ports.

In addition to voltage translation, the NCA9306 device can be used to isolate a 400kHz bus from a 100kHz bus by controlling the EN pin to disconnect the slower bus during fast-mode communication.

Key Features

- 2 Bit bidirectional translator for SDA and SCL lines in mixed-mode I^2C Applications
- I^2C and SMBus Compatible
- Less than 1.5-ns Maximum Propagation Delay to Accommodate Standard-mode and Fast-mode I^2C Devices and Multiple Masters
- Allows Voltage-level Translation Between
  – 1.2V V_{REF1} and 1.8V, 2.5V, 3.3V, or 5V V_{REF2}
  – 1.8V V_{REF1} and 2.5V, 3.3V, or 5V V_{REF2}
  – 2.5V V_{REF1} and 3.3V or 5V V_{REF2}
  – 3.3V V_{REF1} and 5V V_{REF2}
- Provides Bidirectional Voltage Translation with no Direction Pin
- Low 3.5Ω ON-state Resistance Between Input and Output Ports Provides Less Signal Distortion
- Open-drain I^2C I/O ports (SCL1, SDA1, SCL2, and SDA2)
- 5V Tolerant I^2C I/O Ports to Support Mixed-mode Signal Operation
- High-impedance SCL1, SDA1, SCL2, and SDA2 pins for EN = Low
- Lockup-free Operation for Isolation when EN = Low
- Flow-through Pinout for Ease of Printed-circuit board Trace Routing
- Latch-up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  – 2000V Human-Body Model (A114-A)
  – 1000V Charged-Device Model (C101)

Applications

- I^2C, SMBus, PMBus, MDIO, UART, low-speed SDIO, GPIO, and other two-signal interfaces
- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Industrial Automation

Device Information

Part Number	*Package*	*Body Size*
NCA9306-DVSR	VSSOP8	2.00mm × 2.30mm
NCA9306-DTSHR	TSSOP8	3.00mm × 3.00mm

Functional Block Diagrams

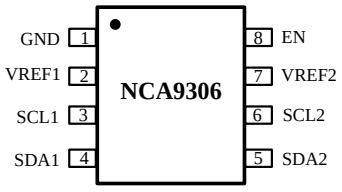

Figure 1. NCA9306 Block Diagram

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1. Pin Configuration and Functions

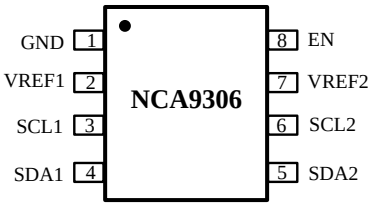


Figure 1.1 NCA9306 Package

Table 1.1 Pin Configuration and Description

Symbol	*Pin*	*Description*
GND	1	Ground, 0 V
V_{REF1}	2	Low-voltage-side reference supply voltage for SCL1 and SDA1
SCL1	3	Serial clock, low-voltage side
SDA1	4	Serial data, low-voltage side
SDA2	5	Serial data, high-voltage side
SCL2	6	Serial clock, high-voltage side
V_{REF2}	7	High-voltage-side reference supply voltage for SCL2 and SDA2
EN	8	Switch enable input

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Conditions*
Reference Voltage(1)	V_{REF1}	-0.5		6	V	
Reference bias Voltage(2)	$V_{bias(REF2)}$	-0.5		6	V	
Input/output Voltage	V_I/V_O	-0.5		6	V	
Input clamp current	I_{IK}			-50	mA	V_I<0V
channel current (DC)	I_{CH}			128	mA	
Operating Temperature	T_{opr}	-40		85	℃	
Storage Temperature	T_{stg}	-40		150	℃	
Electrostatic discharge	HBM			±2000	V	
	CDM			±1000	V	

3. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Max*	*Unit*	*Conditions*

Input/output voltage	V_{IO}	0	5.5	V	SCL1,SDA1,SCL2,SDA2
Reference voltage[1]	V_{REF1}	0	5.5	V	
Reference voltage[1]	V_{REF2}	0	5.5	V	
Enable input voltage	EN	0	5.5	V	
Pass switch current	I_{PASS}	-	64	mA	
Operating ambient temperature	T_A	-40	85	℃	

4. Thermal Information

Parameters	*Symbol*	*VSSOP8*	*TSSOP8*	*Unit*
IC Junction-to-Air Thermal Resistance	θ_{JA}	210.1	189.6	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	81.9	119.6	°C/W
Junction-to-board thermal resistance	θ_{JB}	88.8	102.1	°C/W

5. Specifications

5.1. Electrical Characteristics

VCC = 1.6V to 5.5V; T_{amb} = -40℃ to +85℃; unless otherwise noted. Typical specification are at T_A=25℃

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Conditions*
Input clamp voltage	V_{IK}	-1.2			V	I_I=-18mA,EN=0
Input leakage current	I_{IH}	-	-	1	uA	V_I=5V,EN=0V
Input capacitance	$C_{i(EN)}$		11		pF	V_I=0V or 3V
Off capacitance	$C_{io(off)}$	-	4	6	pF	V_O=0V or 3V,EN=0V;SDAn,SCLn
On capacitance	$C_{io(on)}$	-	10.5	12.5	pF	V_O=0V or 3V,EN=3V;SDAn,SCLn
On-state resistance;SDAn,SCLn[1]	R_{ON}[2]		1.6	3.0	Ω	V_I=0,I_O=64mA,EN=4.5V
			2.0	4.0	Ω	V_I=0,I_O=64mA,EN=3V
			2.6	5.0	Ω	V_I=0,I_O=64mA,EN=2.3V
			2.5	5.0	Ω	V_I=0,I_O=15mA,EN=1.5V
		1	3.9	7.0	Ω	V_I=2.4V, I_O=15mA,EN=4.5V
		20	55	70	Ω	V_I=2.4V, I_O=15mA,EN=3V
		20	46	60	Ω	V_I=1.7V, I_O=15mA,EN=2.3V

[1]Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch.ON-state resistance is determined by the lowest voltage of the two terminals.
[2]Guaranteed by design.

5.2. Switching Characteristics AC Performance

Translating Down

over recommended operating ambient temperature range, EN = 3.3 V, V_{IH} = 3.3 V, V_{IL} = 0, V_M = 1.15 V (unless otherwise noted) (see Figure 5.1).[1,2]

PARAMETER	*FROM (INPUT)*	*TO (OUTPUT)*	*C_L = 50 pF*		*C_L =30 pF*		*C_L = 15 pF*		*UNIT*
			min	*max*	*min*	*max*	*min*	*max*	
t_{plh}	SDA2/SCL2	SDA1/SCL1	0	0.8	0	0.6	0	0.3	ns
t_{phl}			0	1.2	0	1	0	0.5	

over recommended operating ambient temperature range, EN =2.5 V, VIH = 3.3 V, VIL = 0, VM = 0.75 V (unless otherwise noted) (see Figure 5.1).

PARAMETER	*FROM (INPUT)*	*TO (OUTPUT)*	*C_L = 50 pF*		*C_L =30 pF*		*C_L = 15 pF*		*UNIT*
			min	*max*	*min*	*max*	*min*	*max*	
t_{plh}	SDA2/SCL2	SDA1/SCL1	0	1	0	0.7	0	0.4	ns
t_{phl}			0	1.3	0	1	0	0.6	

[1]Translating down: the high-voltage side driving toward the low-voltage side

[2]Guaranteed by design.

Translating UP

over recommended operating ambient temperature range, EN = 3.3 V, VIH = 2.3 V, VIL = 0, VT = 3.3 V, VM = 1.15 V, RL = 300Ω (unless otherwise noted) (see Figure 5.2)[1,2].

PARAMETER	*FROM (INPUT)*	*TO (OUTPUT)*	*C_L = 50 pF*		*C_L =30 pF*		*C_L = 15 pF*		*UNIT*
			min	*max*	*min*	*max*	*min*	*max*	
t_{plh}	SDA1/SCL1	SDA2/SCL2	0	0.9	0	0.6	0	0.4	ns
t_{phl}			0	1.4	0	1.1	0	0.7	

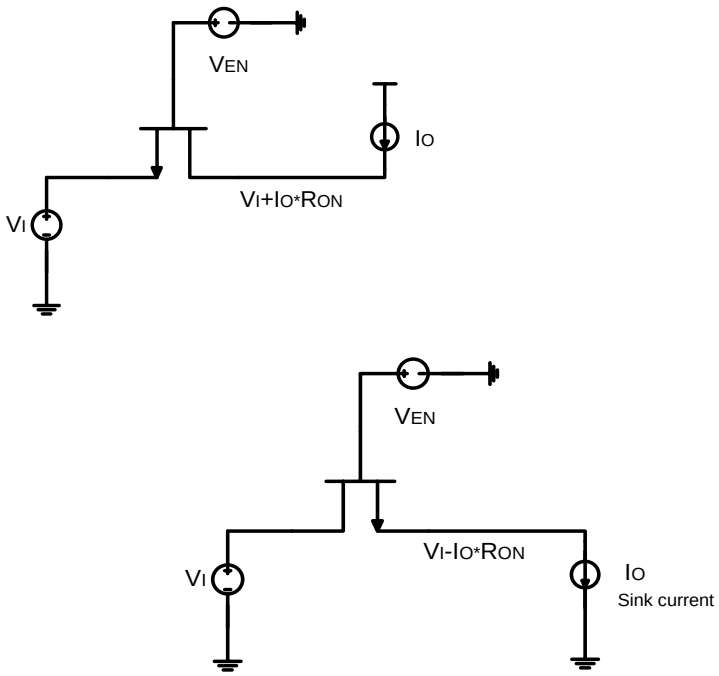
over recommended operating ambient temperature range, EN = 2.5 V, VIH = 2.3 V, VIL = 0, VT = 3.3 V, VM = 0.75 V, RL = 300Ω (unless otherwise noted) (see Figure 5.2).

PARAMETER	*FROM (INPUT)*	*TO (OUTPUT)*	*C_L = 50 pF*		*C_L =30 pF*		*C_L = 15 pF*		*UNIT*
			min	*max*	*min*	*max*	*min*	*max*	
t_{plh}	SDA1/SCL1	SDA2/SCL2	0	1	0	*0.6*	0	0.4	ns
t_{phl}			0	1.3	0	1.3	0	0.8	

[1]Translating up: the low-voltage side driving toward the high-voltage side

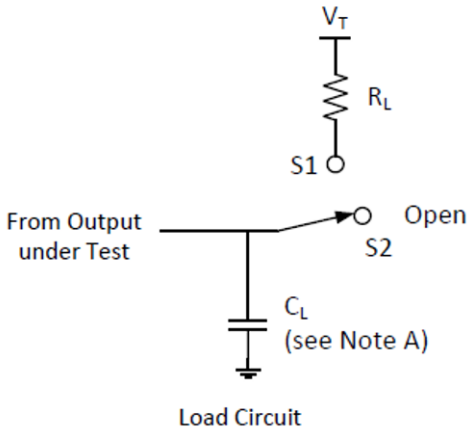
[2]Guaranteed by design.

5.3. Parameter Measurement Information

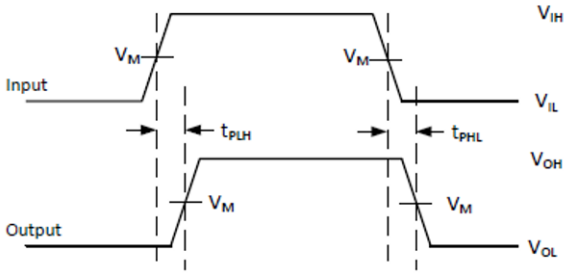


a) Current Source Configuration b) Current Sink Configuration

Figure 5.1 Current Source and Current Sink Configurations for RON Measurements



USAGE	SWITCH
Translating up	S1
Translating down	S2



Notes: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristic : PRR≤10MHz,Z_O=50Ω,t_r≤2ns,t_f≤2ns.

C. The outputs are measured one at a time, with one transition per measurement.

Figure 5.2 Load Circuit for Outputs

6. Function Description

6.1. Overview

The NCA9306 device is a dual bidirectional I^2C and SMBus voltage-level translator with an enable (EN) input and operates without use of a direction pin. The voltage supply range for V_{REF1} is 1.2 V to 3.3 V and the supply range for V_{REF2} is 1.8 V to 5.5 V.

The NCA9306 device can also be used to run two buses, one at 400-kHz operating frequency and the other at 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be disconnected by using the EN pin when the 400-kHz operation of the main bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the level shifter.

In I^2C applications, the bus capacitance limit of 400 pF restricts the number of devices and bus length. The capacitive load on both sides of the NCA9306 device must be taken into account when approximating the total load of the system, ensuring the sum of both sides is under 400 pF.

Both the SDA and SCL channels of the NCA9306 device have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage-translation solutions, because the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower-voltage devices and at the same time protects less-ESD-resistant devices.

Definition of threshold voltage

This document references a threshold voltage denoted as V_{th}, which appears multiple times throughout this document when discussing the NFET between V_{REF1} and V_{REF2}. The value of V_{th} is approximately 0.9 V at room temperature.

Correct Device Set Up

In a normal set up shown in Figure 6.1, the enable pin and V_{REF2} are shorted together and tied to a 200-kΩ resistor, and a reference voltage equal to V_{REF1} plus the FET threshold voltage is established. This reference voltage is used to help pass lows from one side to another more effectively while still separating the different pull up voltages on both sides.

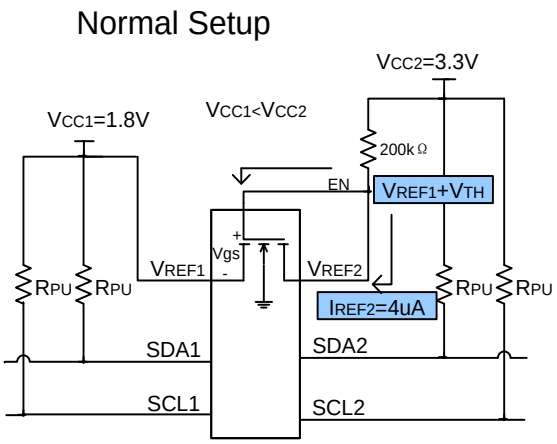


Figure 6.1 Normal Setup

Care should be taken to ensure V_{REF2} has an external resistor tied between it and V_{CC2}. If V_{REF2} is tied directly to the V_{CC2} rail without a resistor, then there is no external resistance from the V_{CC2} to V_{CC1} to limit the current such as in Figure 6.2. This effectively looks like a low impedance path for current to travel through and potentially break the pass FET if the current flowing through the pass FET is larger than the absolute maximum continuous channel current specified in section 1.0. The continuous channel current is larger with a higher voltage difference between V_{CC1} and V_{CC2}.

Figure 6.2 shows an improper set up. If V_{CC2} is larger than V_{CC1} but less than V_{th}, the impedance between V_{CC1} and V_{CC2} is high resulting in a low drain to source current, which does not cause damage to the device. Concern arises when V_{CC2} becomes larger than V_{CC1} by V_{th}. During this event, the NFET turns on and begin to conduct current. This current is dependent on the gate to source voltage and drain to source voltage.

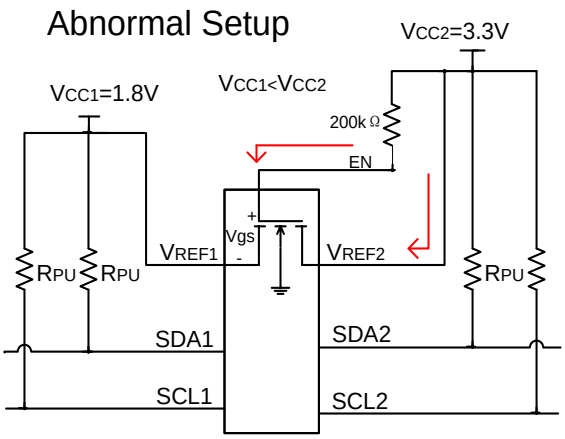


Figure 6.2 Abnormal Setup

Disconnecting a Slave from the Main I2C Bus Using the EN Pin

NCA9306 can be used as a switch to disconnect one side of the device from the main I²C bus. This can be advantageous in multiple situations. One instance of this situation is if there are devices on the I²C bus which only supports fast mode (400 kHz) while other devices on the bus support fast mode plus (1 MHz). An example of this is displayed in Figure 4.1.3.

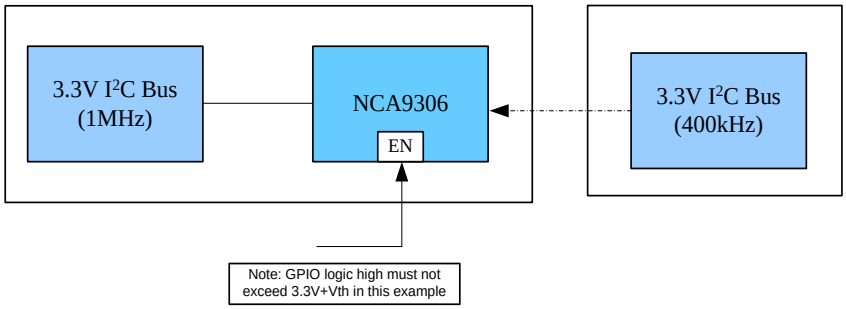


Figure 6.3 Example of an I²C bus with multiple supported frequencies

In this situation, if the master is on the 1 MHz side then communicating at 1 MHz should not be attempted if NCA9306 were enabled. It needs to be disabled for NCA9306 to avoid possibly glitching state machines in devices which were designed to operate correctly at 400 kHz or slower. When NCA9306 is disabled, the master can communicate with the 1 MHz devices without disturbing the 400 kHz bus. When the NCA9306 is enabled, communication across both sides at 400 kHz is acceptable.

Supporting Remote Board Insertion to Backplane with NCA9306

Another situation where NCA9306 is advantageous when using its enable feature is when a remote board with I²C lines needs to be attached to a main board (backplane) with an I²C bus such as in Figure 6.4. If connecting a remote board to a backplane is not done properly, the connection could result in data corruption during a transaction or the insertion could generate an unintended pulse on the SCL line. Which could glitch an I²C device state machine causing the I²C bus to get stuck.

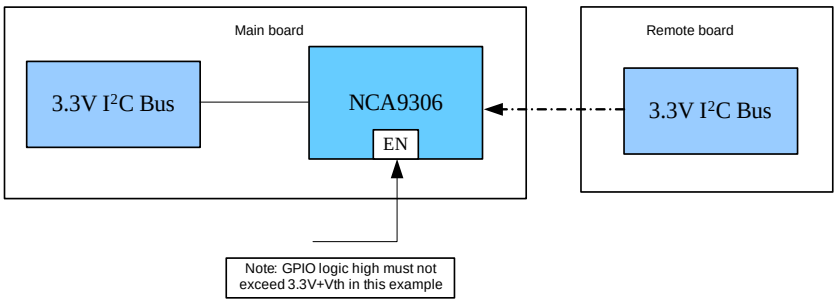


Figure 6.4 An example of connecting a remote board to a main board (backplane)

NCA9306 can be used to support this application because it can be disabled while making the connection. Then it is enabled once the remote board is powered on and the buses on both sides are IDLE.

Switch Configuration

NCA9306 has the capability of being used with its V_{REF1} voltage equal to V_{REF2}. This essentially turns the device from a translator to a device which can be used as a switch, and in some situations this can be useful. The switch configuration is shown in Figure 6.5 and translation mode is shown in Figure 6.6.

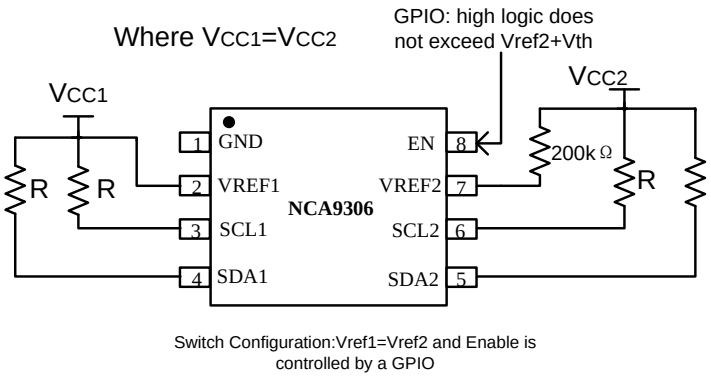


Figure 6.5 Switch Configuration

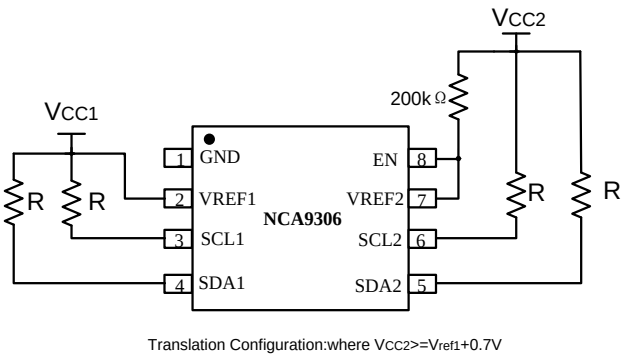
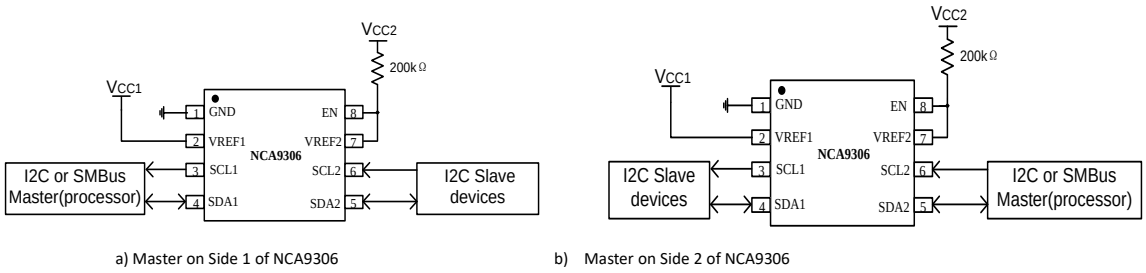


Figure 6.6 Translation Configuration

When NCA9306 is in the switch configuration (V_{REF1} = V_{REF2}), the propagation delays are different compared to the translator configuration. Taking a look at the propagation delays, if the pull up resistance and capacitance on both sides of the bus are equal, then in switch mode the NCA9306 has the same propagation delay from side one to two and side two to one. The propagation delays become lower when V_{CC1}/V_{CC2} is larger. For example, the propagation delay at 1.8 V is longer than at 5 V in the switching configuration. When NCA9306 is in translation mode, side one propagates lows to side two faster than side two can propagate lows to side 1. This time difference becomes larger the larger the difference between V_{CC2} and V_{CC1} becomes.

Master on Side 1 or Side 2 of Device

I²C and SMBus are bidirectional protocol meaning devices on the bus can both transmit and receive data. NCA9306 was designed to allow for signals to be able to be transmitted from either side, thus allowing for the master to be able to placed on either side of the device. Figure 4.1.7 shows the master on Side 1 or Side 2 of NCA9306.



a) Master on Side 1 of NCA9306 b) Master on Side 2 of NCA9306

Figure 6.7 Master on Side 1 or Side 2 of NCA9306

LDO and NCA9306 Concerns

The V_{REF1} pin can be supplied by a low-dropout regulator (LDO), but in some cases the LDO may lose its regulation because of the bias current from V_{REF2} to V_{REF1}. If the LDO cannot sink the bias current, then the current has no other paths to ground and instead charges up the capacitance on the V_{REF1} node (both external and parasitic). This results in an increase in voltage on the V_{REF1} node. If no other paths for current to flow are established (such as back biasing of body diodes or clamping diodes through other devices on the V_{REF1} node), then the V_{REF1} voltage ends up stabilizing when V_{gs} of the pass FET is equal to V_{th}. This means V_{REF1} node voltage is V_{CC2} - V_{th}. Note that any slaves/masters running off of the LDO now see the V_{CC2} - V_{th} voltage which may cause damage to those slaves/masters if they are not rated to handle the increased voltage.

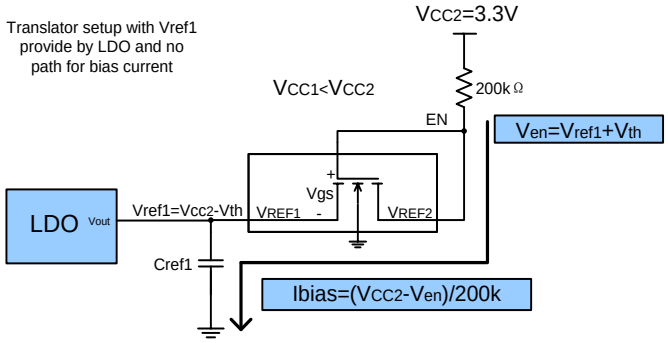


Figure 6.8 Example of no leakage current path when using LDO

To ensure LDO does not lose regulation due to the bias current of NCA9306, a weak pull down resistor can be placed on V_{REF1} to ground to provide a path for the bias current to travel. The recommended pull down resistor is calculated by Equation 4 where 0.75 gives about 25% margin for error incase bias current increases during operation.

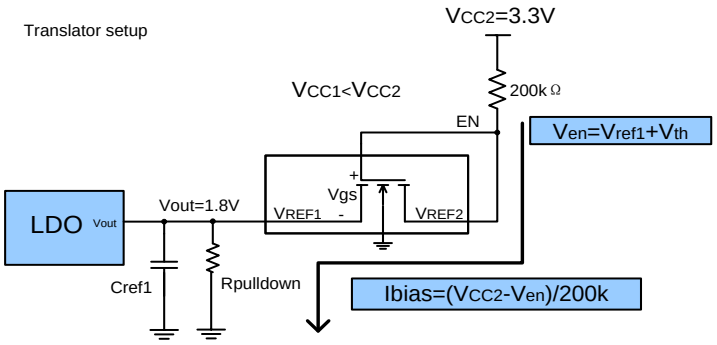


Figure 6.9 Example with Leakage current path when using an LDO

$$V_{en} = V_{REF1} + V_{th}$$

where

V_{th} is approximately 0.9 V (1)

$I_{bias} = (V_{CC2} - V_{en})/200k$ (2)

$R_{pulldown} = V_{OUT}/Ibias$ (3)

Recommended $R_{pulldown} = R_{pulldown}$ x 0.75 (4)

Current Limiting Resistance on VREF2

The resistor is used to limit the current between V_{REF2} and V_{REF1} (denoted as R_{CC}) and helps to establish the reference voltage on the enable pin. The 200k resistor can be changed to a lower value; however, the bias current proportionally increases as the resistor decreases.

$$I_{bias} = (V_{CC2} - V_{en})/R_{CC} \quad (5)$$

where

V_{th} is approximately 0.9V

$V_{en} = V_{REF1} + V_{th}$

Keep in mind R_{CC} should not be sized low enough that I_{CC} exceeds the absolute maximum continuous channel current specified in Equation 6.

$$R_{CC(min)} \geq (V_{CC2} - V_{en})/0.128 \quad (6)$$

where

V_{th} is approximately 0.9V

$V_{en} = V_{REF1} + V_{th}$

6.2. Functional Block Diagram

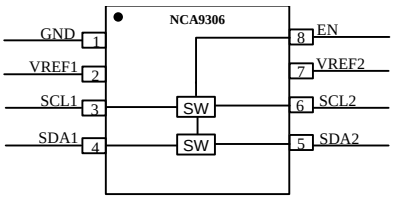


Figure 6.10 Block Diagram of NCA9306

6.3. Feature Description

Enable (EN) Pin

The NCA9306 device is a double-pole, single-throw switch in which the gate of the transistors is controlled by the voltage on the EN pin. In Figure 7.1, the NCA9306 device is always enabled when power is applied to V_{REF2}. In Figure 7.2, the device is enabled when a control signal from a processor is in a logic-high state.

Voltage Translation

The primary feature of the NCA9306 device is translating voltage from an I^2C bus referenced to V_{REF1} up to an I^2C bus referenced to V_{DPU}, to which V_{REF2} is connected through a 200-kΩ pullup resistor. Translation on a standard, open-drain I^2C bus is achieved by simply connecting pullup resistors from SCL1 and SDA1 to V_{REF1} and connecting pullup resistors from SCL2 and SDA2 to V_{DPU}.

7. Application Note

7.1. Application Information

General Applications of I2C

As with the standard I²C system, pullup resistors are required to provide the logic-high levels on the translator bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I²C devices in addition to SMBus devices. Standard-mode I2C devices only specify 3 mA in a generic I2C system where standard-mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used. When the SDA1 or SDA2 port is low, the clamp is in the ON state, and a low-resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is high, the SDA2 port is pulled to the pullup supply voltage of the drain (VDPU) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1-SCL2 channel also functions in the same way as the SDA1-SDA2 channel.

7.2. Typical Application

Figure 7.1 and Figure 7.2 show how these pullup resistors are connected in a typical application, as well as two options for connecting the EN pin.

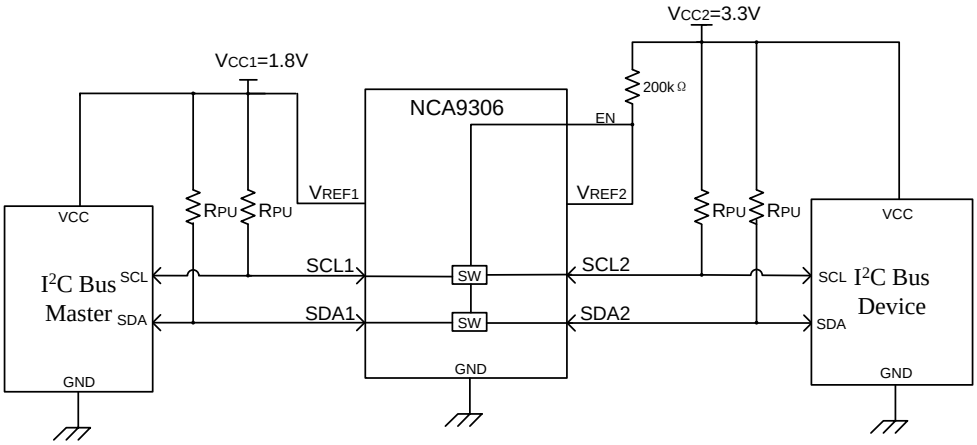


Figure 7.1 Typical Circuit (Switch Always Enabled)

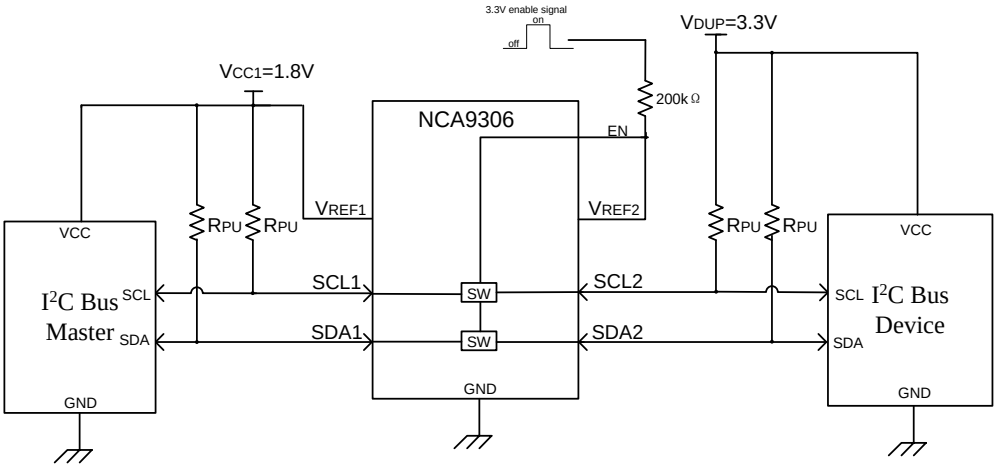


Figure 7.2 Typical Application Circuit (Switch Enable Control)

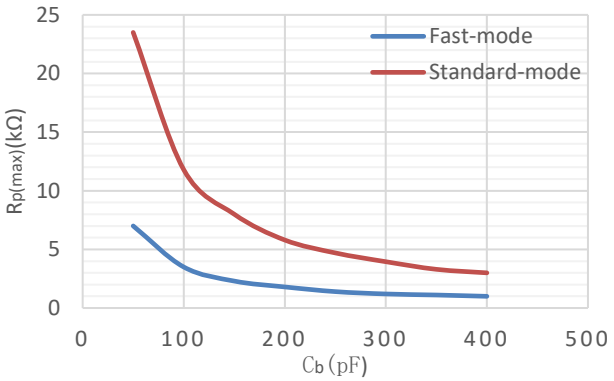
7.3. Detailed Design Procedure

Bidirectional Voltage Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{REF2} and both pins pulled to high-side V_{DPU} through a pullup resistor (typically 200 kΩ). This allows V_{REF2} to regulate the EN input. A 100-pF filter capacitor connected to VREF2 is recommended. The I^2C bus master output can be push-pull or open-drain (pullup resistors may be required) and the I^2C bus device output can be open-drain (pullup resistors are required to pull the SCL2 and SDA2 outputs to V_{DPU}). However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state capable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open-drain, no direction control is needed.

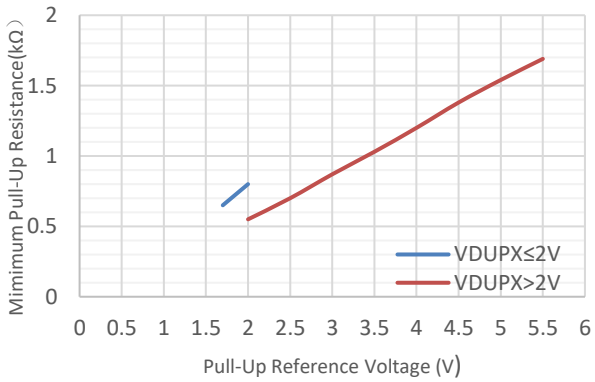
Sizing Pullup Resistors

Figure 7.3 and Figure 7.4 respectively show the maximum and minimum pullup resistance allowable by the I^2C specification for standard-mode (100 kHz) and fast-mode (400 kHz) operation.



Standard mode (f_{SCL}=100kHz,tr=1us)
Fast mode (f_{SCL}=400kHz,tr=300ns)

Figure 7.3 Maximum Pullup Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL}=0.2*V_{DPUX},I_{OL}=2mA when V_{DPUX}≤2V
V_{OL}=0.4V,I_{OL}=3mA when V_{DPUX}>2V

Figure 7.4 Minimum Pullup Resistance ($R_{p(min)}$) vs Pullup Reference Voltage (V_{DPUX})

8. Power Supply Recommendations

For supplying power to the NCA9306 device, the V_{REF1} pin can be connected directly to a power supply. The V_{REF2} pin must be connected to the V_{DPU} power supply through a 200-kΩ resistor. Failure to have a high impedance resistor between V_{REF2} and V_{DPU} results in excessive current draw and unreliable device operation. It is also worth noting, that in order to support voltage translation, the NCA9306 must have the EN and V_{REF2} pins shorted and then pulled up to V_{DPU} through a high-impedance resistor.

9. Layout

9.1. Layout Guidelines

For printed-circuit board (PCB) layout of the NCA9306 device, common PCB layout practices should be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other on leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. The 100-pF filter capacitor should be placed as close to V_{REF2} as possible. A larger decoupling capacitor can also be used, but a longer time constant of two capacitors and the 200-kΩ resistor results in longer turnon and turnoff times for the NCA9306 device.

These best practices are shown in Figure 9.1.

For the layout example provided in Figure 9.1, it would be possible to fabricate a PCB with only two layers by using the top layer for signal routing and the bottom layer as a split plane for power (VCC) and ground (GND). However, a four-layer board is preferable for boards with higher-density signal routing. On a four-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface-mount component pad, which must attach to VCC or GND, and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace must be routed to the opposite side of the board, but this technique is not demonstrated in Figure 9.1.

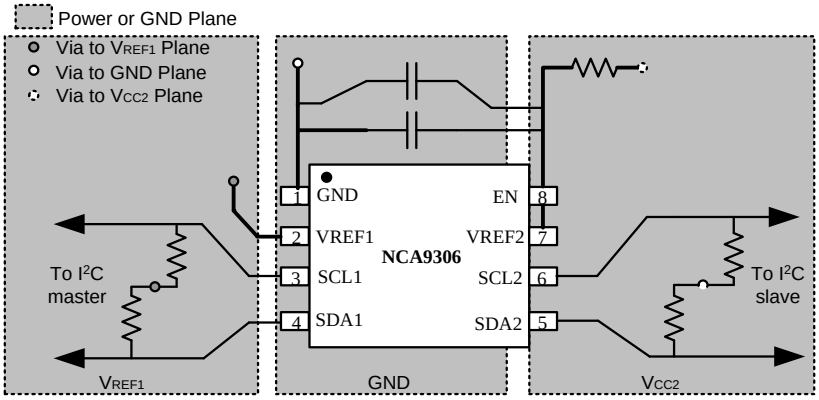
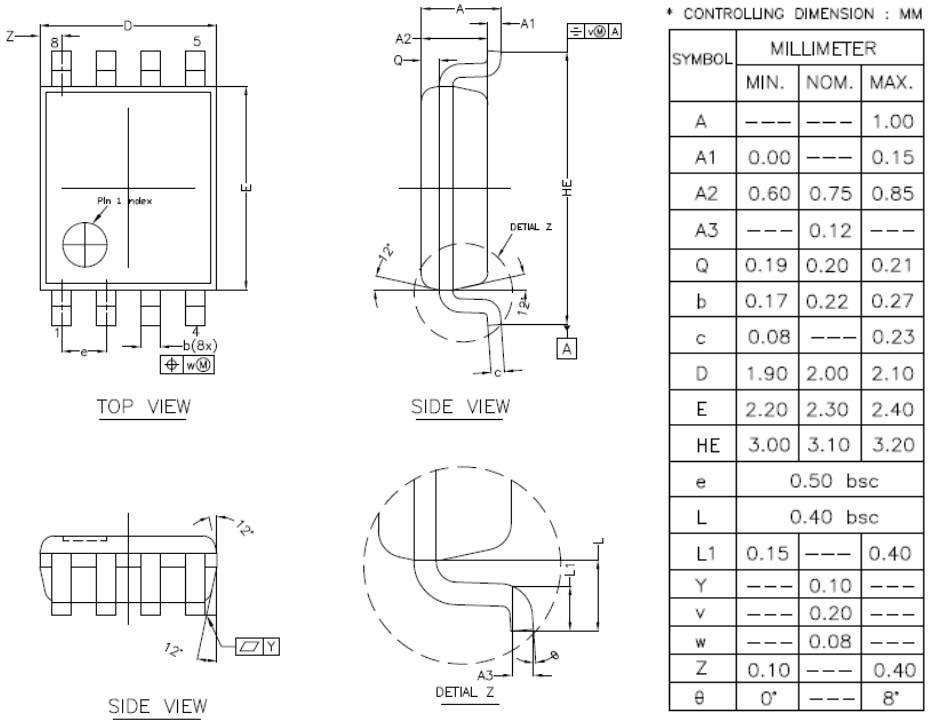


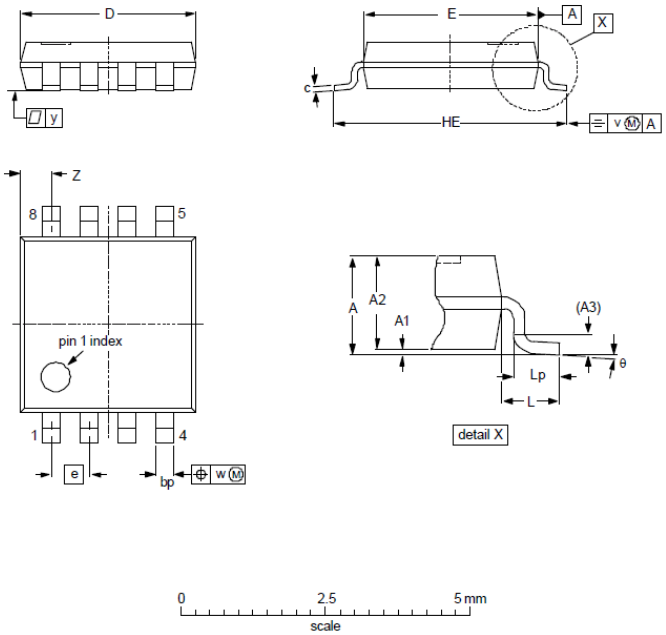
Figure 9.1 NCA9306 Layout Example

10. Package Information



SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.00
A1	0.00	---	0.15
A2	0.60	0.75	0.85
A3	---	0.12	---
Q	0.19	0.20	0.21
b	0.17	0.22	0.27
c	0.08	---	0.23
D	1.90	2.00	2.10
E	2.20	2.30	2.40
HE	3.00	3.10	3.20
e	0.50 bsc		
L	0.40 bsc		
L1	0.15	---	0.40
Y	---	0.10	---
v	---	0.20	---
w	---	0.08	---
Z	0.10	---	0.40
θ	0°	---	8°

Figure 10.1 VSSOP8 Package Shape and Dimension in millimeters and (inches)



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A1	A2	A3	bp	c	D(1)	E(1)	e	HE	L	Lp	v	w	y	Z(1)	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Figure 10.2 TSSOP8 Package Shape and Dimension in millimeters and (inches)

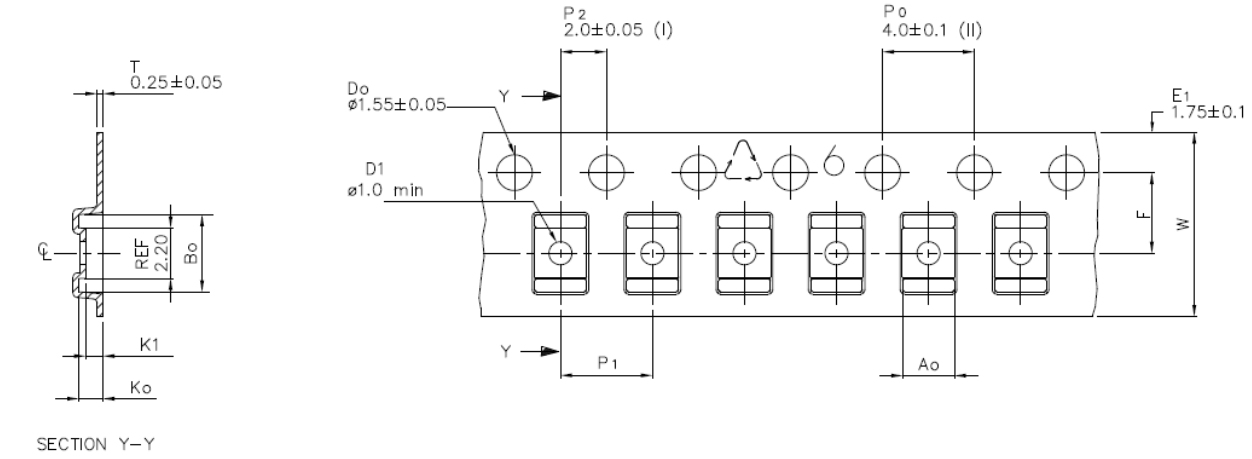
11. Order information

Part Number	*Pins*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*Package Qty*
NCA9306-DVSR	8	-40 to 85℃	1	VSSOP	VSSOP	3000
NCA9306-DTSHR	8	-40 to 85℃	1	TSSOP	TSSOP	3000

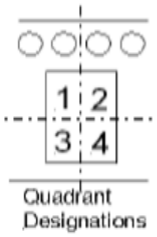
12. Documentation Support

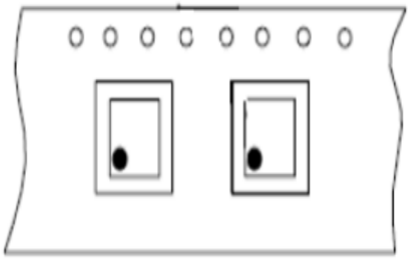
Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NCA9306	Click here	Click here	Click here	Click here

13. Tape and Reel Information



Ao	2.25 +/−0.1
Bo	3.35 +/−0.1
Ko	1.40 +/−0.1
K1	1.00 +/−0.1
F	3.50 +/−0.05
P1	4.00 +/−0.1
W	8.00 +/−0.1





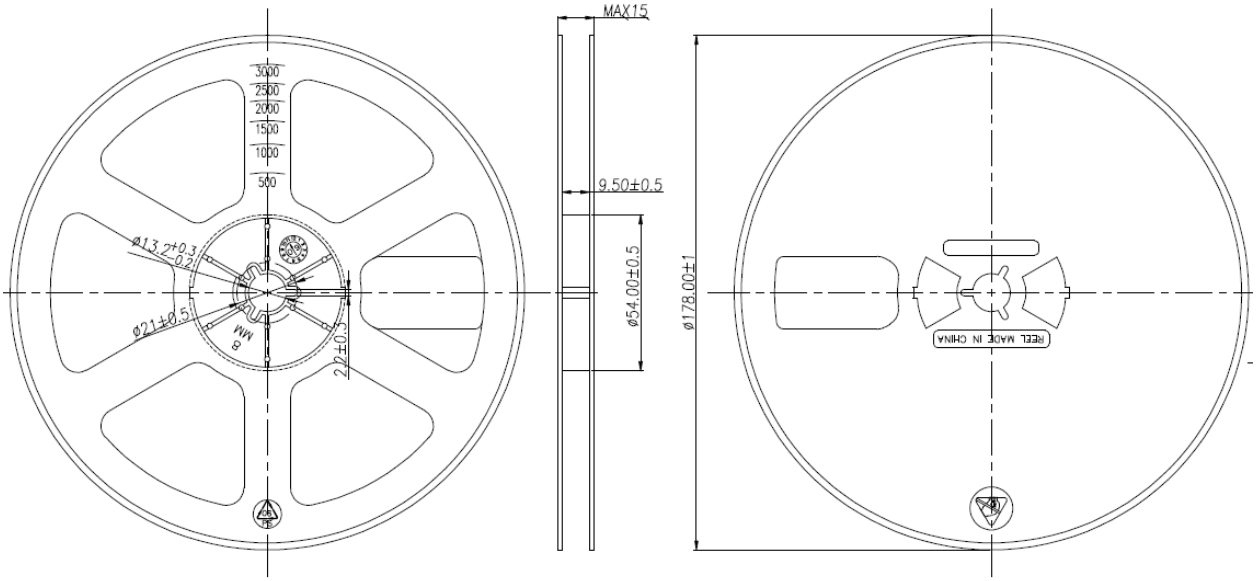
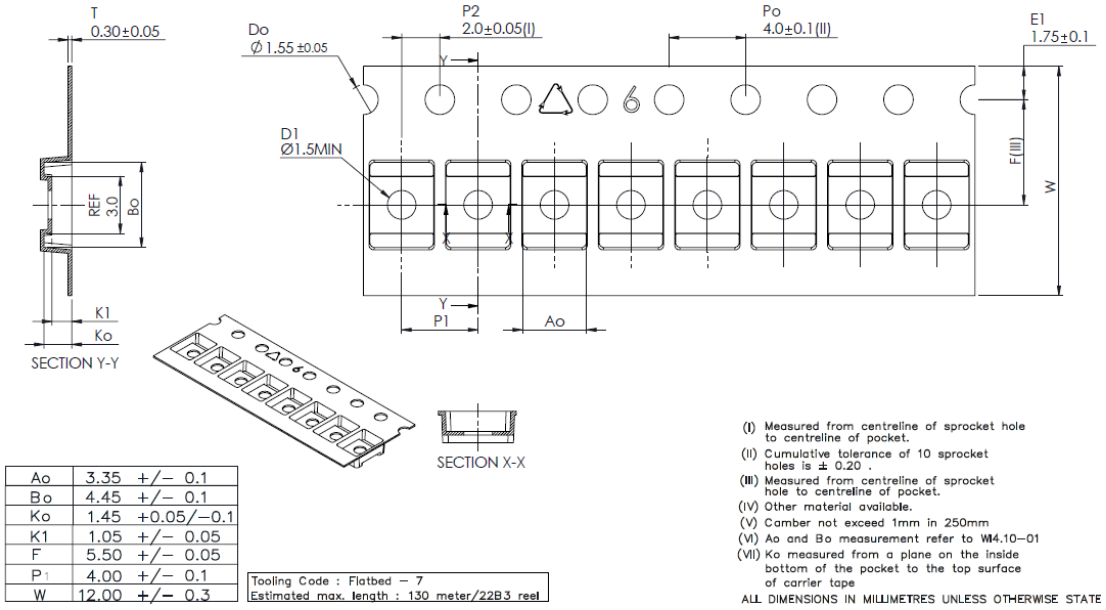


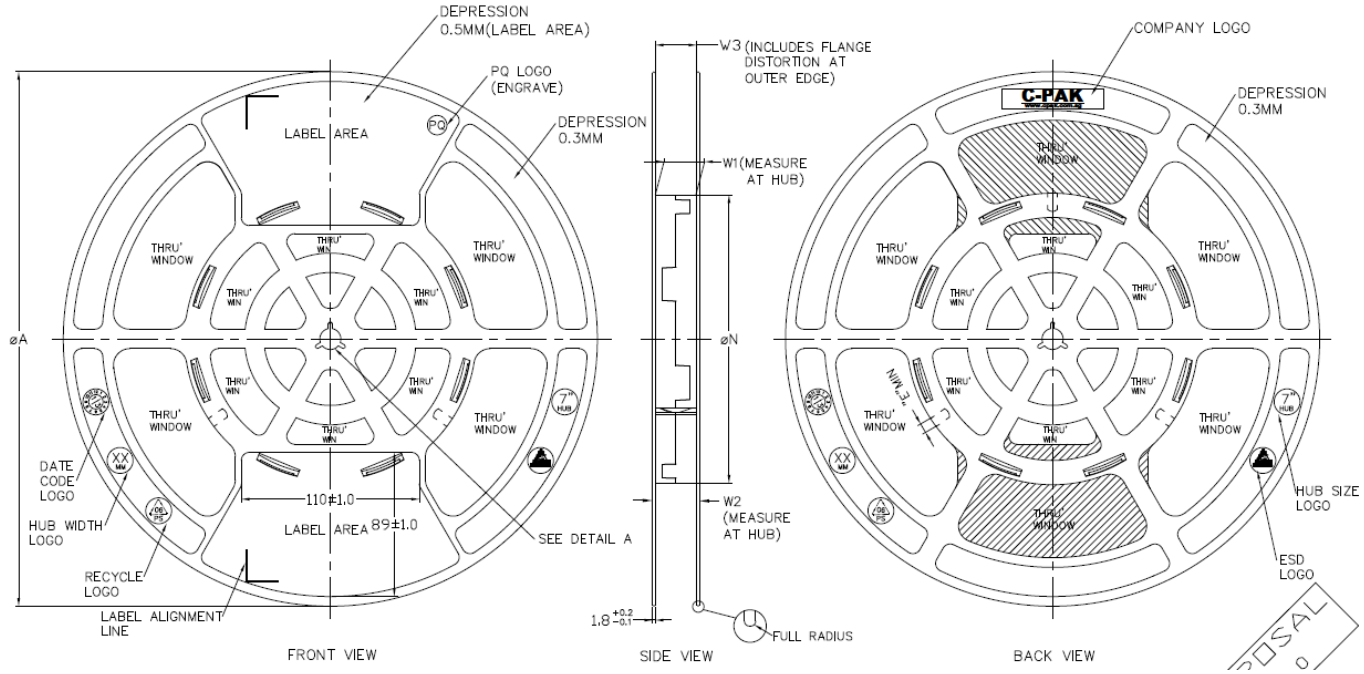
Figure 12.1 Tape and Reel Information of VSSOP8

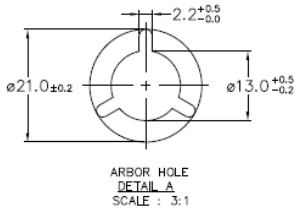


Ao	3.35	+/− 0.1
Bo	4.45	+/− 0.1
Ko	1.45	+0.05/−0.1
K1	1.05	+/− 0.05
F	5.50	+/− 0.05
P1	4.00	+/− 0.1
W	12.00	+/− 0.3

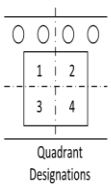
Tooling Code : Flatbed – 7
Estimated max. length : 130 meter/22B3 reel

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Camber not exceed 1mm in 250mm
(VI) Ao and Bo measurement refer to W4.10–01
(VII) Ko measured from a plane on the inside bottom of the pocket to the top surface of carrier tape
ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATE





PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.5	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.5 −0.0	38.4		5.5



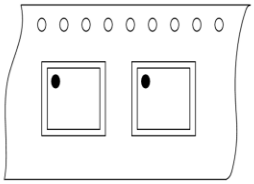


Figure 12.1 Tape and Reel Information of TSSOP8

14. Revision history

Revision	*Description*	*Date*
1.0	Initial version	2020/4/25
1.1	Added tape and reel information	2020/7/1

单击下面可查看定价，库存，交付和生命周期等信息

>>Novosense(纳芯微)