NSA2862X: General Sensor Conditioner for IoT

Datasheet (EN) 2.0

Product Overview

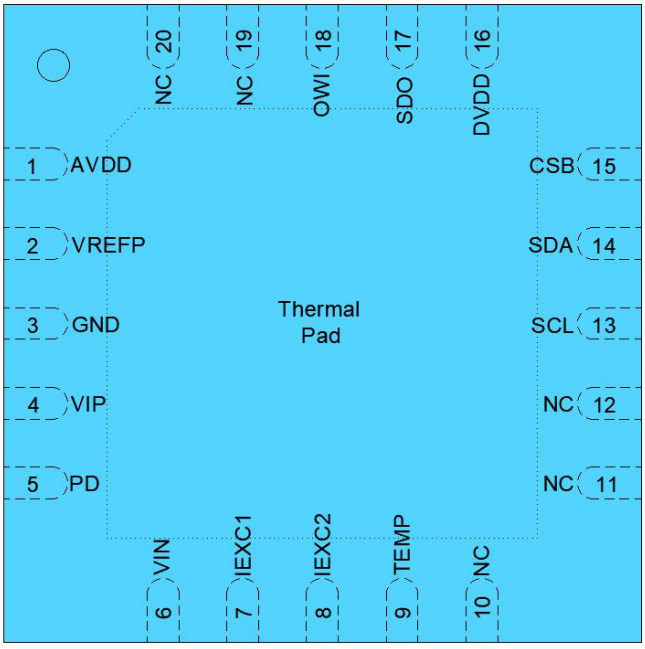
The NSA2862X is a highly integrated sensor conditioner dedicated for IoT applications. It can be used for resistive or voltage output sensors like resistive bridge pressure sensor, thermocouple, RTD etc. The NSA2862X integrates a 24-bit primary signal measurement channel, a 24-bit temperature measurement channel, sensor calibration logic, a pair of constant current sources and a 16-bit DAC. It can provide three kinds digital outputs (I2C, SPI and OWI). The high integrity enables very compact PCB design with very few external components. With the internal calibration algorithm built in the MCU, the NSA2862X supports to compensate the temperature drift of zero and span up to the 2nd order and also the linearity up to the 3rd order. The NSA2862X also has a standby mode in which only consumes less 100nA current. It is very suitable for ultra-low power sensor applications

Key Features

- Analog Functions
  - Ultra-low power: <10nA @25℃
  - Fast response time: 4ms
  - Low drift voltage reference
  - Instrumental amplifier with variable gain from 1X to 256X
  - 24-bit ADC for primary signal measurement
  - 24-bit ADC for temperature measurement
  - Internal and external temperature sensor supported
  - A pair of current sources
  - 16-bit DAC
- Digital Functions
  - 1X~8X digital gain
  - Multiple filter settings
  - Sensor calibration logic with built-in MCU
  - EEPROM
- Output
  - Special OWI communication
  - I2C
  - SPI (3 wires or 4 wires)
- Others
  - Package: QFN20 (4*4mm)
  - Operation temperature: -40℃~105℃

Applications

- Wireless Pressure sensors and transmitters
- Wireless Thermocouple transmitter
- Wireless RTD temperature transmitter
- Other low power sensors



Note: NC pins must be left floating.

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1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
AVDD Voltage	AVDDmax	-0.3		6.5	V	
Analog pins voltage		-0.3		AVDD+0.3	V	
Analog output current Limit				25	mA	
Digital pin voltage		-0.3		AVDD+0.3	V	25℃
ESD susceptibility	HBM	±2			kV	
	CDM	±500			V	
Maximum junction temperature	Tjmax			155	℃	
Storage temperature		-60		150	℃	
Operation temperature	T_{A_EXT}	-40		105	℃	Normal temperature range
	T_{A_ADV}	-40		85	℃	Best Performance Temp range
	T_{A_BST}	125		150	℃	Extended temperature range, For 500h max over life time

2.0 ELECTRICAL CHARACTERISTICS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply and Regulation						
Supply Voltage Range	AVDD	2.7	5	5.5	V	
DVDD LDO Output	DVDD	1.7	1.78	1.85	V	
Power On Reset	V_{POR_AVDD}		2.5		V	POR threshold as power up
	V_{POR_HYS}		0.1		V	POR Hysteresis
Operating Current (Sensor not included)	Iavdd_st		40		nA	Standby mode, -40℃
			6		nA	Standby mode, 25℃
			240		nA	Standby mode, 105℃
	Iavdd_wk		1.63		mA	Normal mode, Gain_P=1
	Iavdd_cmd		190		uA	Command mode
Internal pull up resistor	R_{PD}		68		kΩ	Only for PD pin

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Initial Time	Tinit		2.2		ms	Initial time after power on or exiting standby mode
Single Conversion Time	Tconv		1.5		ms	ODR_P=2400Hz
Response Time	Tresponse		4		ms	From initiating to data ready
Reference Voltage and Current Source						
Internal Bandgap Reference	VBG		1.200		V	Not measurable directly, proportional with AVDDJ VREF
VBG TC	VBG_TC		5	25	ppm/℃	-40℃~105℃
VREF Output(VREFP-VREFN)	VREF	3.585	3.605	3.625	V	VREF_LVL=0, 25℃
		2.441	2.455	2.469	V	VREF_LVL=1, 25℃
Load on VREF	R_{VREF}	0.5			Kohm	
VREF Current Limit	I_{VREF_limit}		20		mA	Short to Ground
Input Current When VREF Driven External	I_VREF_EXT		10		nA	VREF_DIS = 1
Current Source Outputs (Internal Reference Resistor)	IEXC1	0		750	uA	50uA/Step
	IEXC2	0		700	uA	50uA/Step, When IEXC2<3:0> ≠ 1111b
External Reference Resistor for Constant Current	R_{IEXC}	20	25	33	kohm	When IEXC2<3:0>=1111b
IEXC Temperature Drift (Internal Reference Resistor）	IEXC_TC		100		ppm/℃	
Mismatch of IEXCs (IEXC1<3:0>= IEXC2<3:0>)		-2%	-0.4%	2%		IEXC*<3:0> = 0001~0011
		-1%	-0.2%	1%		IEXC*<3:0> = 0100~0111
		-0.5%	-0.1%	0.5%		IEXC*<3:0> = 1000~1110
IEXC PSRR			1.2	4	uA/V	IEXC = 350uA
Headroom Voltage for Current Sources		0		AVDD-0.8	V	
IEXC RMS Noise, 0.1~100Hz				5	nA	IEXC = 500uA
Primary Signal Measurement Channel						
PGA Gain	GAIN	1		256		
PGA Gain Error	GAINP_ERR	0.05%		0.5%		Gain_P =1,2
		-0.1%		0.7%		Gain_P =4,6
		-0.3%		0.6%		Gain_P =8,12

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		-0.5%		0.5%		Gain_P =16,24
		-0.75%		0.25%		Gain_P =32,48
		-1.8%	-1%	0.4%		Gain_P =64,96,128,192,256
PGA Gain TC Drift	GAINP_TC		3		ppm/℃	
Offset	OFF			600	uV	Input referred, SYSTEM_CHOP_EN = 0
		-10	1	10	uV	Input referred，SYSTEM_CHOP_EN = 1
Offset TC	OFF_DRIFT		±5		nV/℃	Input referred SYSTEM_CHOP_EN = 1
PADC Resolution	RES_{RAW}		24		Bits	
PADC Output Data Rate	ODR_P	10		2400	Hz	
ENOB of Primary Channel	ENOB_P	Refer to Table4.1			Bits	Depends on PGAIN and ODR_P
Integral nonlinearity	INL			15	ppm of FS	
Input CMRR of Primary Channel	CMRR		120		dB	
PSRR of Primary Channel	PSRR	90	120		dB	
Temperature Measurement Channel (Internal and External Temperature Sensor)						
TADC Resolution	RES_T	24			Bit	
TADC GAIN	GAIN_T	1		4		1,2,4
TADC Output Data Rate	ODR_T	10		2400	Hz	
TADC ENOB	ENOB_P	Refer to Table 4.2,4.3				
Error of Internal Temperature Sensor			±1.5	±3	℃	-40 to 125 ℃
TEMP Input Impedance			1		Gohm	
Analog Input Pins						
Analog Input Voltage	VIP, VIN	GND+0.4		AVDD-1.2	V	PGA on (Gain>2)
		GND+0.1		AVDD-0.1	V	PGA off, Buffer on
		GND-0.1		AVDD+0.1	V	PGA off, Buffer off

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Differential Input Voltage Range	V_{range}		±VREF /GAIN		V	VREF:ADC Reference Voltage
VINP,VINN Input Pin Leakage	$I_{leakage}$		±1		nA	DIAG_ON=0，25℃
Diagnostic and Alarm						
Burnout Current	I_{diag}		100		nA	
Fault Alarm High	FAULT_HIGH	98%			VDD	
Fault Alarm Low	FAULT_LOW			2%	VDD	
OSC						
ADC Clock	FOSC_MOD		614.4		kHz	
Clock Rate Error	FOSC_ERR	-2%		1%		-40~125℃
EEPROM						
Programming Temperature	T_{EEP}	-40		105	℃	
Programming Supply Voltage	VEE	3		5.5	V	
Time for EEPROM programming	t_{EEP}		0.8	1	s	
Endurance			5000			
Date Retention		10			Years	@150℃
Serial Interface						
Communication Data Rate	Fsclk			10	MHz	SPI Interface
				400	kHz	I2C Interface
				50	kHz	OWI Interface

3.0 REGISTER DESCRIPTION

The register map of theNSA2862X includes two parts, normal registers and EEPROM registers. The normal registers include data registers and some control registers, while the EEPROM registers are mainly configuration registers and calibration coefficients. All EEPROM registers should be written by external interface on command mode (register 'CMD' = '0x00').

3.1. NORMAL REGISTERS

IF_CTRL(R/W)

Addr	Bit	Register name	Default	Description
0x00	7，0	SDO_ACTIVE	1'b1	0: SPI3-wire 1: SPI4-wire （SDO as serial output）
	6，1	LSB_FIRST	1'b0	0: SPI MSB first 1: SPI LSB first
	5，2	SOFTRESET	1'b0	Set either of these two bits to 1 to reset the chip. Return to 0 after

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				reset.

STATUS (Read only)

Addr	Bit	Register name	Default	Description
0x02	7 – 3	ERROR_CODE<4:0>	5'b00000	x1xxxb: VIP open or short to VREF xx1xxb: VIP short to GND xxx1xb: VIN open or short to VREF xxxx1b: VIN short to GND
	2	CRC_ERR	1'b0	1: CRC error detected during EEPROM loading; When CRC error is asserted, EEPROM register bits 'OWI_DIS', 'OWI_AC_EN', 'OWI_WINDOW,' 'JFET_DIS', 'VREF_DIS', 'EEPROM_LOCK' are forced to 0.
	1	LOADING_END	1'b0	1: EEPROM loading end flag
	0	DRDY	1'b0	1: Set after a new data updated and automatically cleared after a register reading to PDATA/TDATA or before the next data's coming.

PDATA (Read only, Primary channel data register)

Addr	Bit	Register name	Default	Description
0x06	7 – 0	PDATA<23:16>	0x00	Signed，2's complement: When'RAW_P'= 1, stores the ADC output of primary channel, When'RAW_P'=0, stores the calibrated primary channel data.
0x07	7 – 0	PDATA<15:8>	0x00	
0x08	7 – 0	PDATA<7:0>	0x00	

TDATA (Read only, temperature channel data register)

Addr	Bit	Register name	Default	Description
0x09	7 – 0	TDATA<23:16>	0x00	Signed，2's complement: When 'RAW_T' = 1, stores the ADC output of temperature channel, When 'RAW_T'= 0, stores the calibrated temperature data, LSB = 1/2^16℃. Real Temperature =TDATA/2^16+25 ℃
0x0a	7 – 0	TDATA<15:8>	0x00	
0x0b	7 – 0	TDATA<7:0>	0x00	

COMMAND (R/W, command register)

Addr	Bit	Register name	Default	Description
0x30	7 – 0	CMD<7:0>	0x03	0x00: command mode, all EEPROM can be written only in command mode. 0x01/0x02: Single mode 0x03: Continuous mode 0x33: Enter EEPROM Program Mode

QUIT_OWI (Write only)

Addr	Bit	Register name	Default	Description

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0x61	7 – 0	QUIT_OWI <7:0>	0x00	Write'0x5D' to this register to quit OWI communication If 'QUIT_OWI_CNT' =0x00, quit OWI communication permanently. If 'QUIT_OWI_CNT' is not 0x00, quit OWI mode temporary with a certain time and then get back to OWI mode.

QUIT_OWI_CNT (R/W)

Addr	Bit	Register name	Default	Description
0x62	7 – 0	QUIT_OWI_CNT<7:0>	0x00	Time for temporary quit OWI communication Mode. 0x00：Quit forever，0x01：50ms，0x02：100ms … 0xFF：12.8s

EE_PROG (R/W)

Addr	Bit	Register name	Default	Description
0x6a	7 – 0	EE_PROG<7:0>	0x00	Write '0x7E' or '0xFE' to this register to start EEPROM Programming. Automatically cleared to '0x00' after programming finished.

VDD_CHECK (R/W)

Addr	Bit	Register name	Default	Description
0x70	0	VDD_CHECK	1'b0	Write '1' to force VDD/2 as the input of temperature ADC

3.2. EEPROM REGISTERS

SYS_CONFIG1 (R/W)

Addr	Bit	Register name	Default	Description
0xa1	7	CAL_MODE	1'b0	0: one segment calibration with the 2nd order temperature coefficients 1: two segment calibration with the 1st order temperature coefficients.
	6	BURNOUT_EN	1'b0	1: enable the 100nA burnout current sources.
	5	Reserved	1'b0	Reserved
	4	Reserved	1'b0	Reserved
	3	OWI_AC_EN	1'b0	0: Single-port OWI communication mode 1: Dual-port OWI communication mode
	2	OWI_WINDOW	1'b0	0: OWI can be entered during a 10ms~80ms window after power up or soft reset 1: infinite window, OWI can be entered any time after power up
	1	OWI_DIS	1'b0	1: OWI disabled (Won't be effective until next power on reset or soft reset after EEPROM is programmed)
	0	Reserved	1'b0	Reserved

SYS_CONFIG2 (R/W)

Addr	Bit	Register name	Default	Description
0xa2	7	JFET_DIS	1'b1	1: Disable JFET regulator (Recommends to set to "1")

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	6	JFET_LVL	1'b0	0: JFET regulator outputs 5V. 1:JFET regulator outputs 3.3V
	5	VREF_DIS	1'b0	1: Disable reference buffer and reference voltage can be forced externally
	4	VREF_LVL	1'b0	0: VREFP = 3.6V 1: VREFP = 2.45V
	3	T_OUT_EN	1'b0	1: when not in OWI mode, TADC data outputs through OWI pin in PWM format
	2 - 0	Reserved	3'b111	Reserved, shall be set to 3'b111

Current_EXC (R/W)

Addr	Bit	Register name	Default	Description
0xa3	7 – 4	IEXC1<3:0>	4'b0000	IEXC1/2: set IEXC1 and IEXC2 current value or mode 0000: Disabled 0001: 50uA 0010: 100uA … 1110: 700uA 1111 for IEXC1, 750uA; 1111 for IEXC2: use external reference resistor
	3 – 0	IEXC2<3:0>	4'b0000	

PCH_Config1 (R/W)

Addr	Bit	Register name	Default	Description
0xa4	7 – 4	GAIN_P<3:0>	4'b0000	Primary Channel Gain 0000:1X, 0001:2X, 0010:4X, 0011:6X, 0100:8X, 0101:12X, 0110:16X, 0111:24X, 1000:32X, 1001:48X, 1010:64X, 1011:96X, 1100:128X, 1101:192X, 1110:256X, 1111:1X and disable buffer.
	3 – 0	ODR_P<3:0>	4'b0000	PADC output data rate setting 0000:2.4KHz, 0001: 1.2KHz, 0010: 600Hz, 0011: 300Hz, 0100: 150Hz, 0101:75Hz, 0110:37.5Hz, 0111:18.75Hz, 1000:12Hz(with 60Hz notch), 1001:10Hz (with 50Hz notch), 1010~1101: Reserved, 1110~1111:PADC disabled

PCH_Config2 (R/W)

Addr	Bit	Register name	Default	Description
0xa5	7 – 6	Reserved	2'b00	Reserved
	5 – 3	Reserved<2:0>	3'b000	Reserved, shall be 3'b000
	2	SYS_CHOP_EN	1'b0	0: disable system chopping 1: enable system chopping
	1	INPUT_SWAP	1'b0	1: swap the polarity of inputs of PADC
	0	RAW_P	1'b0	0: update calibrated sensor data into 'PDATA' register. 'DAC_DATA' will be set by internal calibration logic. 1: update raw primary ADC data into 'PDATA' register after conversion, and allow DAC to be set externally;

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TCH_Config (R/W)

Addr	Bit	Register name	Default	Description
0xa6	7	EXT_TEMP	1'b0	0: internal temperature sensor selected 1: external temperature sensor selected (TEMP pin as external temperature sensor input)
	6 – 5	GAIN_T<1:0>	2'b00	Gain for temperature channel 00:1X, 01:2X, 10/10:4X
	4 – 1	ODR_T	4'b0000	TADC output data rate，similar as ODR_P 0000:2.4KHz, 0001: 1.2KHz, 0010: 600Hz, 0011: 300Hz, 0100: 150Hz, 0101:75Hz, 0110:37.5Hz, 0111:18.75Hz, 1000:12Hz(with 60Hz notch), 1001:10Hz (with 50Hz notch), 1010~1101: Reserved, 1110~1111:TADC disabled. When TADC disabled, the negative reference voltage (VREFN) for PADC is driven externally through TEMP pin
	0	RAW_T	1'b0	1: store the direct TADC output into 'TDATA' register 0: store the calibrated TADC data into 'TDATA' register.

CLAMPH (R/W)

Addr	Bit	Register name	Default	Description
0xa7	7 – 0	Reserved	0x00	Reserved

CLAMPL (R/W)

Addr	Bit	Register name	Default	Description
0xa8	7 – 0	Reserved	0x00	Reserved

OFFSET0 (R/W)

Addr	Bit	Register name	Default	Description
0xa9	7 – 0	OFF0<15:8>	0x00	Sensor Calibration coefficient, offset at T0. LSB=1/2^15. RANGE (-1，+1)
0xaa	7 – 0	OFF0<7:0>	0x00	

CTC1 (R/W)

Addr	Bit	Register name	Default	Description
0xab	7 – 0	CTC1<15:8>	0x00	Sensor Calibration coefficient, CAL_MODE=0: the 1st order temperature coefficient of offset. LSB=1/2^22. RANGE(-0.00781, +0.00781) CAL_MODE=1: the 1st order temperature coefficient of offset for segment 0.LSB=1/2^22. RANGE (-0.00781, +0.00781)
0xac	7 – 0	CTC1<7:0>	0x00	

CTC2 (R/W)

Addr	Bit	Register name	Default	Description
0xad	7 – 0	CTC2<15:8>	0x00	Sensor Calibration coefficient, CAL_MODE=0: the 2nd order temperature coefficient of offset. LSB=1/2^29, RANGE (-6.1e-5, 6.1e-5) CAL_MODE=1: the 1st order temperature coefficient of offset for
0xae	7 – 0	CTC2<7:0>	0x00	

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				segment 1, LSB=1/2^22. RANGE (-0.00781, +0.00781)

S0 (R/W)

Addr	Bit	Register name	Default	Description
0xaf	7 – 0	S0<15:8>	0x00	Sensor calibration coefficient, sensitivity at T0. LSB=1/2^15 (unsigned), RANGE(0， 2)
0xb0	7 – 0	S0<7:0>	0x00	

STC1 (R/W)

Addr	Bit	Register name	Default	Description
0xb1	7 – 0	STC1<15:8>	0x00	Sensor Calibration coefficient, CAL_MODE=0: the 1st order temperature coefficient of sensitivity. LSB=1/2^22. RANGE(-0.00781, +0.00781) CAL_MODE=1: the 1st order temperature coefficient of sensitivity for segment 0. LSB=1/2^22. RANGE (-0.00781, +0.00781)
0xb2	7 – 0	STC1<7:0>	0x00	

STC2 (R/W)

Addr	Bit	Register name	Default	Description
0xb3	7 – 0	STC2<15:8>	0x00	Sensor Calibration coefficient. CAL_MODE=0: the 2nd order temperature coefficient of sensitivity. LSB=1/2^29, RANGE (-6.1e-5, 6.1e-5) CAL_MODE=1: the 1st order temperature coefficient of sensitivity for segment 1, LSB=1/2^22. RANGE (-0.00781, +0.00781)
0xb4	7 – 0	STC2<7:0>	0x00	

KS (R/W)

Addr	Bit	Register name	Default	Description
0xb5	7 – 0	KS<15:8>	0x00	Sensor calibration coefficient, the 2nd order nonlinearity coefficient, LSB=1/2^15, RANGE(-1， +1)
0xb6	7 – 0	KS<7:0>	0x00	

KSS (R/W)

Addr	Bit	Register name	Default	Description
0xb7	7 – 0	KSS<15:8>	0x00	Sensor calibration coefficient, the 3rd order nonlinearity coefficient, LSB=1/2^16, RANGE (-0.5， +0.5)
0xb8	7 – 0	KSS<7:0>	0x00	

SPARE (R/W)

Addr	Bit	Register name	Default	Description
0xb9	7 – 0	Spare0 <7:0>	0x00	User defined
0xba	7 – 0	Spare1 <7:0>	0x00	
0xbb	7 – 0	Spare2 <7:0>	0x00	
0xb9	7 – 0	Spare3 <7:0>	0x00	
0xba	7 – 0	Spare4 <7:0>	0x00	
0xbb	7 – 0	Spare5 <7:0>	0x00	

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T0 (R/W)

Addr	Bit	Register name	Default	Description
0xbf	7 – 0	T0<7:0>	0x00	Sensor calibration coefficient, reference temperature point, Real reference temperature, REAL_T0 = T0 + 25, LSB=1. RANGE(-128，+127)

KTS (R/W)

Addr	Bit	Register name	Default	Description
0xc0	7 – 0	KTS<7:0>	0x00	Sensor calibration coefficient, the 2nd order nonlinearity coefficient for external temperature sensor, LSB=1/2^7, RANGE(-1，+1)

MTO (R/W)

Addr	Bit	Register name	Default	Description
0xc1	7 – 0	MTO<15:8>	0x00	Sensor calibration coefficient, offset coefficient of external temperature sensor , MTO: LSB=1/2^15, RANGE (-1，+1)
0xc2	7 – 0	MTO<15:8>	0x00	

KT (R/W)

Addr	Bit	Register name	Default	Description
0xc3	7 – 0	KT<15:8>	0x00	Sensor calibration coefficient: sensitivity coefficient of external temperature sensor, KT: LSB=1/2^12, RANGE (-8，+8)
0xc4	7 – 0	KT<15:8>	0x00	

SPARE (R/W)

Addr	Bit	Register name	Default	Description
0xc5	7 – 0	Spare6 <7:0>	0x00	User defined
0xc6	7 – 0	Spare7 <7:0>	0x00	
0xc7	7 – 0	Spare8 <7:0>	0x00	
0xc8	7 – 0	Spare9 <7:0>	0x00	

PADC_OFF (R/W)

Addr	Bit	Register name	Default	Description
0xc9	7 – 0	PADC_OFF<23:16>	0x00	PADC calibration coefficient: PADC offset, LSB=1/2^23，RANGE (-1，+1)
0xca	7 – 0	PADC_OFF<15:8>	0x00	
0xcb	7 – 0	PADC_OFF<7:0>	0x00	

PADC_GAIN (R/W)

Addr	Bit	Register name	Default	Description
0xcc	7 – 0	PADC_GAIN<15:8>	0x00	PADC calibration coefficient: PADC gain, LSB=1/2^16，RANGE (-0.5, +0.5)
0xcd	7 – 0	PADC_GAIN<7:0>	0x00	

P0 (R/W)

Addr	Bit	Register name	Default	Description

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0xce	7 – 0	P0 <7:0>	0x00	Sensor calibration coefficient: reference pressure point for nonlinearity calibration, LSB=1/2^7, RANGE((-1, 1)

SPARE (R/W)

Addr	Bit	Register name	Default	Description
0xcf	7 – 0	SPARE10<7:0>	0x00	SPARE Register 1
0xd0	7 – 0	SPARE11<7:0>	0x00	SPARE Register 2
0xd1	7 – 0	SPARE12<7:0>	0x00	SPARE Register 3
0xd2	7 – 0	SPARE13<7:0>	0x00	SPARE Register 4
0xd3	7 – 0	SPARE14<7:0>	0x00	SPARE Register 5
0xd4	7 – 0	SPARE15<7:0>	0x00	SPARE Register 6
0xd5	7 – 0	SPARE16<7:0>	0x00	SPARE Register 7
0xd6	7 – 0	SPARE17<7:0>	0x00	SPARE Register 8

DIG_GAIN (R/W)

Addr	Bit	Register name	Default	Description
0xd7	7-6	DIG_GAIN<1;0>	2'b00	ADC digital gain 00:1X, 01:2X, 10:4X, 11:8X
	5–0	Reserved	6'b000000	Reserved

RESERVED

Addr	Bit	Register name	Default	Description
0xd8	7-0	RESERVED		NOVOSENSE Information

EEPROM_LOCK (R/W)

Addr	Bit	Register name	Default	Description
0xd9	7	EEPROM_LOCK	1'b0	1: EEPROM lock，set 1 and then EEPROM can't be programmed. (Won't be effective until next power on reset or soft reset after EEPROM is programmed)
	6 – 0	Part ID (read only)	7'b0000001	NOVOSENSE chip ID.

4.0 FUNCTION DESCRIPTION

The NSA2862X is a highly integrated sensor conditioner like Wheatstone bridge pressure sensor, thermocouple and RTD. The chip incorporates four parts: analog front-end module, digital module, power supply module and serial interfaces. The block diagram of the NSA2862X is shown in Figure 4.1.

Analog front-end module includes a primary signal measurement channel with an instrumental amplifier followed by a 24-bit ∑Δ ADC, a temperature measurement channel with also a 24-bit ∑Δ ADC, for precision sensor signal measurement.

The digital module is composed of registers, EEPROM, control logic, and a built-in MCU. The sensor calibration algorithm is implemented with the built-in MCU and can supports up to 2ndorder temperature drift compensation of offset and sensitivity for the sensor. It can also compensate the nonlinearity of sensor output up to 3rd order. The configuration parameters and coefficients for

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calibration are stored at in the EERPOM of 57 bytes.

The power supply module includes a low drift voltage reference, a sensor voltage driver and a pair of current sources. The NSA2862X supports three serial interfaces: SPI, I2C and OWI, writing and reading registers of configuration, calibration coefficients and data.

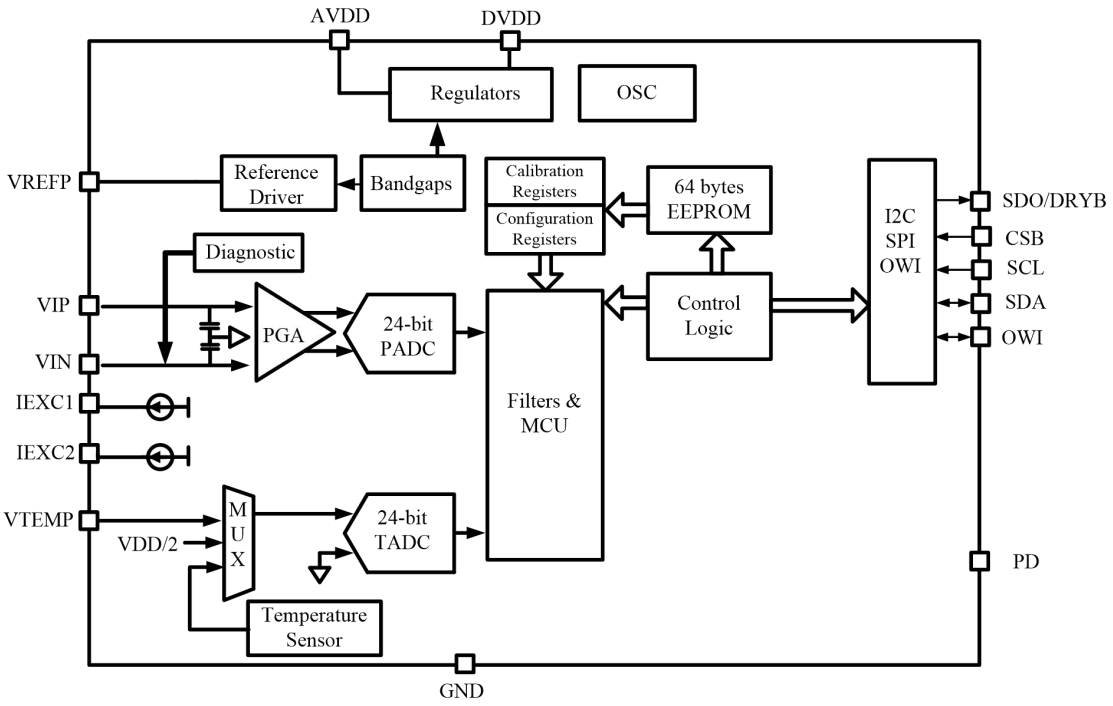

Figure 4.1 Block diagram of the NSA2862X

4.1. WORKING MODE

The NSA2862X has five different working modes: standby mode, single mode, continuous mode, command mode and programming mode. User can choose alternate mode by writing different values in COMMAND register CMD<7:0> or setting the PD pin voltage level.

4.1.1. Standby mode (PD = High)

When PD pin is high, the NSA2862X enters standby mode. In this mode, it only consumes less than 100 Na current. The NSA2862X enters single mode after PD pin voltage transits to low.

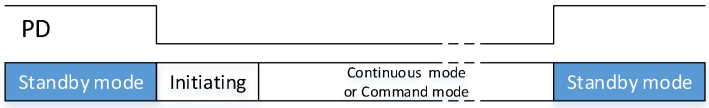

图 4.2 Enter standby mode and exit

4.1.2. Single mode (CMD<7:0> = 0x01/0x02)

The NSA2862X can enter single mode from standby mode by setting PD pin voltage to low. Writing 0x01 to CMD<7:0> can also make NSA2862X enter single mode. In this mode, the chip will enter command mode after data conversion being completed once. CMD<7:0> will return to 0x00 simultaneously. The conversion time of single mode depends on ODR_P and ODR_T settings.

Table 4.1 Conversion time VS ODR

ODR (Hz)	2400	1200	600	300	150	75	37.5	20	10
Tconv (ms)	1.53	1.96	2.77	4.44	7.78	14.5	27.9	54.7	101.6

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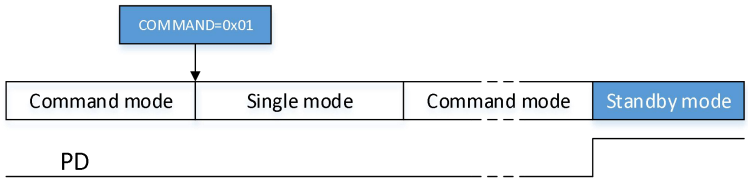

图 4.3 Enter single mode and exit

After transiting to command mode from standby mode, the data registers PDATA and TDATA will keep the results of last conversion in single mode.

4.1.3. Continuous mode (CMD<7:0> = 0x03)

Writing 0x03 to CMD<7:0> will make NSA2862X enter continuous mode. In this mode, the primary signal ADC channel and temperature ADC channel will refresh the PDATA and TDATA registers at a stated ODR continuously. Writing 0x00 to CMD<7:0> can make NSA2862X exit continuous mode.

If RAW_P or RAW_T is set to 1, the ADC conversion results will be put into the 'PDATA' or 'TDATA' directly. Otherwise, the embedded MCU will use the latest temperature data to calibrate primary ADC channel output data every time its measurement completed. .

NSA2862X's shadow register mechanism can guarantee the validity of data. User will not read the incorrect data due to data updating in communication process.

While reading PDATA or TDATA registers, the 3 bytes data must be read sequentially in one read transfer.

4.1.4. Command mode (CMD<7:0> = 0x00)

In this mode, access to all configuration registers is allowable and the chip keeps in a relative low power state.

4.1.5. Programming mode (CMD<7:0> = 0x33)

In this mode, EEPROM can be programmed. Please refer to chapter 4.5 for detailed information about EEPROM operation.

4.2. ANALOG FRONT-END MODULE 1： PRIMARY SIGNAL CHANNEL

The primary signal measurement channel includes an instrumental PGA, 24-bit sigma-delta ADC (PADC) followed by digital filters.

4.2.1. PGA+PADC

The PGA is a gain programmable instrumental amplifier, with its gain configurable to 1X， 2X， 4X， 6X , 8X, 16X, 24X, 32X, 48X, 64X, 96X, 128X, 196X, 256X. The NSA2862X has built-in RFI filter for RFI immunity enhancement.

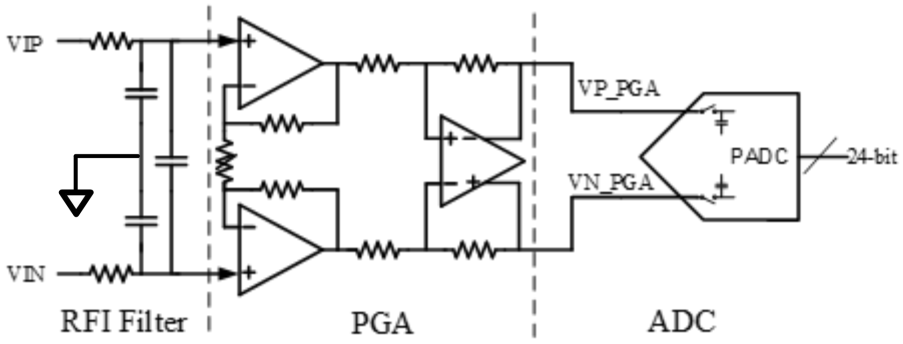

Figure4.2 Primary signal channel (PGA+ADC)

The PADC performs the analog to digital conversion. The output of the ADC is digital filtered with 24-bit resolution. The reference voltage of the ADC is VREF, and the allowable differential input range is ±VREF/GAIN_P. The PADC output can be expressed by the following equation：

$$PDATA_{RAW} = \frac{VIP - VIN}{VREF} * GAIN\_P * 2^{23}$$

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PDATA$_{RAW}$ can be read out from 'PDATA' registers (Reg0x06-Reg0x08) only when 'RAW_P' is set to 1, otherwise, the built-in MCU calibrates the sensor using the calibration coefficients and temperature data stored in 'TDATA' and put the calibrated digital output of the primary channel onto the 'PDATA' registers.

4.2.2. The input common-mode voltage of PGA

The PGA is of differential input and differential output. The output voltages of the PGA can be express as:

$$VP\_PGA = VCMin + GAIN\_P * VDin / 2$$

$$VN\_PGA = VCMin - GAIN\_P * VDin / 2$$

, in which VCMin and VDin are the common-mode voltage and differential voltage of the PGA input voltage. To avoid the saturation of the amplifiers, both VP_PGA and VN_PGA should meet the follow limitation:

AGND+0.1V<VP(N)_PGA<AVDD-0.1V

From above, the input common-mode voltage should satisfy following limitation:

AGND+0.1V+GAIN_P*VDin(max)/2 < VCMin < AVDD-0.1V-GAIN_P*VDin(max)/2

Besides, the input of the PGA amplifiers is PMOS transistor so the PGA input should meet:

VIP(N) < AVDD -1V

For voltage-driven bridge sensors, the common-mode voltage of its output is usually close to VREF/2. One can easily meet the limitation by choosing a proper 'GAIN_P' and make VDin(max) <0.8*VREF/GAIN_P. '0.8' here is considered to give some margin for the sensor sensitivity and the amplifier voltage swing. For current-driven sensors, more careful settings is needed to maximize the dynamic range of the PADC.

4.2.3. Digital filter

The bandwidth and output data rate (ODR) of the digital filter can be set by 'ODR_P'. ODR can be set from 2.4 KHz to 2.5 Hz. The lower ODR, the lower noise the PADC output will have, in the cost of slower time response. Table 4.1 shows the effective number of bits (ENOB) of PADC output with different ODR_P settings. The relationship of ENOB with RMS noise is:

$$ENOB_{RMS} = 24 - \log_2(RMS_{ADC})$$

RMS$_{ADC}$ is the RMS value of ADC output noise in LSB. The relationship between RMS ENOB (ENOB$_{RMS}$) and noise free ENOB (ENOB$_{NF}$) is shown as below:

$$ENOB_{NF} = ENOB_{rms} - 2.7$$

Table 4.2 ENOB$_{RMS}$ of PADC under different ODR settings (VREF=4V, 'SYS_CHOP_EN'=0)

	GAIN														
ODR (Hz)	1	2	4	6	8	12	16	24	32	48	64	96	128	192	256
2400	17.9	18.0	17.8	17.8	17.8	17.6	17.8	17.7	17.6	17.5	17.3	16.9	16.5	16.1	15.6
1200	18.3	18.4	18.3	18.3	18.2	18.2	18.2	18.0	18.0	17.8	17.5	17.2	16.8	16.3	16.0
600	18.7	18.6	18.5	18.7	18.6	18.6	18.6	18.4	18.4	18.1	17.9	17.6	17.1	16.7	16.3
300	19.0	18.9	19.0	19.0	18.8	18.9	18.8	18.8	18.6	18.6	18.3	18.0	17.6	17.1	16.7
150	19.7	19.5	19.7	19.6	19.6	19.6	19.6	19.4	19.3	19.0	18.9	18.5	18.0	17.6	17.2
75	20.7	20.9	20.6	20.6	20.7	20.6	20.4	20.1	20.1	19.8	19.5	19.0	18.6	18.1	17.7
37.5	21.2	21.4	21.1	21.1	21.0	21.0	21.0	20.8	20.7	20.3	20.0	19.6	19.2	18.7	18.3
18.75	21.8	21.9	21.5	21.7	21.6	21.6	21.4	21.3	21.2	20.8	20.5	20.1	19.7	19.2	18.8
10*	22.3	22.3	22.0	22.1	22.1	22.1	22.0	21.8	21.6	21.2	21.0	20.5	20.1	19.6	19.2

*For ODR of 10Hz, two filter settings can be selected but with the same ENOB$_{RMS}$

*When ODR_P=10Hz, the 50 or 60Hz notch filter will be activated. User can choose the proper notch filter for different applications. The error of the clock rate is designed to be less than 1% to minimize the effect to notch filter ability.

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4.2.4. System Chopping

When 'SYS_CHOP_EN' =1, the system chopping mode of primary signal channel is enabled. When this mode is used, the input-referred offset of the primary signal channel can be very small. Meanwhile, the system chopping can also improve the immunity of RFI/EMI. ENOB will be 0.5-bit higher when system chopping is enabled with the actual ODR is about half of the setting ODR_P when ODR_P <=600Hz. For ODR_P >600Hz, the actual ODR is 1/4 of setting ODR_P at minimum.

4.3. ANALOG MODULE 2: TEMPERATURE MEASUREMENT CHANNEL

The temperature measurement channel is to measure the working temperature of the sensor for the temperature compensation of the sensed signal. This channel works independently of the primary channel. The NSA2862X supports both internal temperature sensor and external temperature sensor, selected by register bit 'EXT_TEMP' bit. The temperature sensor's output is digitized by a 24-bit ADC (TADC) and also digital filtered. The ODR setting of the temperature measurement channel is the same as the primary signal channel, set by 'ODR_T'. When the temperature difference between the sensor element and the NSA2862X chip is acceptable, internal temperature sensor can be used. Otherwise, a proper external temperature measurement scheme should be chosen, such as diode, RTD, NTC or the bridge resistor itself, etc. Through different 'RAW_T' setting, either the direct TADC data or the calibrated temperature data can be read from 'TDATA' registers.

4.3.1. Internal temperature sensor

The internal temperature sensor is factory calibrated, with its calibration coefficients stored at EEPROM registersreg0xC1, reg0xC2 and reg0xC3. When 'RAW_T' is set to 0 and 'GAIN_T' is set to 4X, the NSA2862X can provide a temperature reading in degree Celsius, in the format of

$$T = TDATA / 2\text{^}16 + 25\ ℃$$

For example, 'TDATA=0x1FF24B' corresponding to 56.95°C. The relationship between the noise of the internal temperature sensor and 'ODR_T' setting is shown in Table 4.2.

Table 4.3 RMS Noise of Internal Temperature Sensor under different ODR_T

ODR (Hz)	2400	1200	600	300	150	75	37.5	18.75	10
RMS Noise in ℃	0.0079	0.0060	0.0045	0.0038	0.0032	0.0020	0.0015	0.0011	0.0008

4.3.2. External temperature sensor

When external temperature sensor mode is selected, the temperature sensing signal input from the TEMP pin is buffered for TADC conversion. The reference voltage of the TADC is also VREF. The gain of the TADC can be 1X, 2X and 4X. The relationship between $TDATA_{RAW}$ and the temperature input is

$$TDATA_{RAW} = VTEMP * GAIN\_T / VREF * 2^{23}$$

When RAW_T = 0, the built-in MCU calibrated the offset, sensitivity and nonlinearity of the measured temperature signal. Please refer to application note: *AN: Sensor Calibration for the NSA2862X* for the detail of the calibration description. The external temperature sensing can be done in many ways, including NTC, RTD, diode and sensor bridge resistance itself. Figure 4.3 gives an example using a low TC drift resistor to sense the bridge resistance, which is usually proportional to the temperature of the sensor element. In case the bridge sensor is current driven, the bridge voltage can be used as temperature sensing input directly.

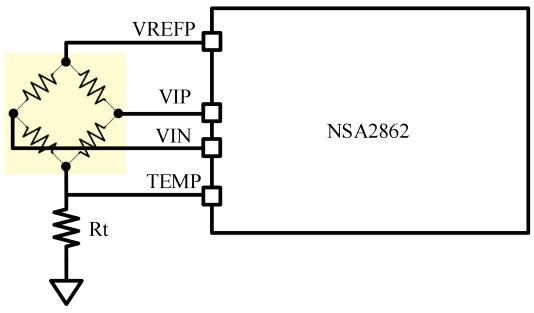

Figure 4.3 External temperature sensing using sensor bridge and a reference resistor

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The output data rate of TADC can be set by 'ODR_T', similar as the primary signal channel. The relationship between ODR_T and the ENOB of TADC is shown in Table 4.3.

Table 4.4 ENOB of TADC under different ODR_T (External temperature sensor mode)

ODR_T (HZ)	ENOB		
	GAIN_T=1	GAIN_T=2	GAIN_T=4
2400	17.7	17.5	16.9
1200	18.1	17.9	17.2
600	18.5	18.1	17.2
300	18.8	18.3	17.4
150	19.1	18.5	17.6
75	19.5	18.9	18.0
37.5	19.4	18.6	17.6
18.75	19.9	18.7	18.1
10	20.2	19.4	18.5

4.4. POWER MANAGEMENT AND SENSOR DRIVE

The NSA2862X internally includes a precision bandgap reference with very low temperature drift, less than 0.1% during full temperature range (-40~85˚C). This reference voltage is used in the constant voltage or current driving circuits for sensors, JFET regulator, clock generator and ADC/DAC etc.

4.4.1. Sensor Driver

4.4.1.1. Constant Voltage Drive

The VREFP pin can provide a constant voltage to drive the bridge sensors, which is also the reference voltage for PADC and TDAC (in external Temperature Sensor Mode). The constant driving voltage can be selected either 4V or 2.5V via the EERPOM register bit 'VREF_LVL'. When' VREF_DIS' = 1, VREFP pin can be driven from the external reference voltage.

When TADC is activated (ODR_T≠1111b), the negative reference voltage (VREFN) for PADC is internally connected to GND and When TADC is disabled (ODT_T = 1111b), the negative reference voltage (VREFN) for PADC is driven externally through TEMP pin.

4.4.1.2. Constant Current Drive

A pair of constant current sources is available for current-driven pressure sensors, RTD sensors and external diode temperature sensors. The constant driving current can be configured with internal or external reference resistor as shown in Figure 4.10. When 'IEXC2' ≠1111b, an internal reference resistor is used and the current output through IEXC1 and IEXC2 pins are separately configured by 'IEXC1' and 'IEXC2' with the mismatch less than 1%.

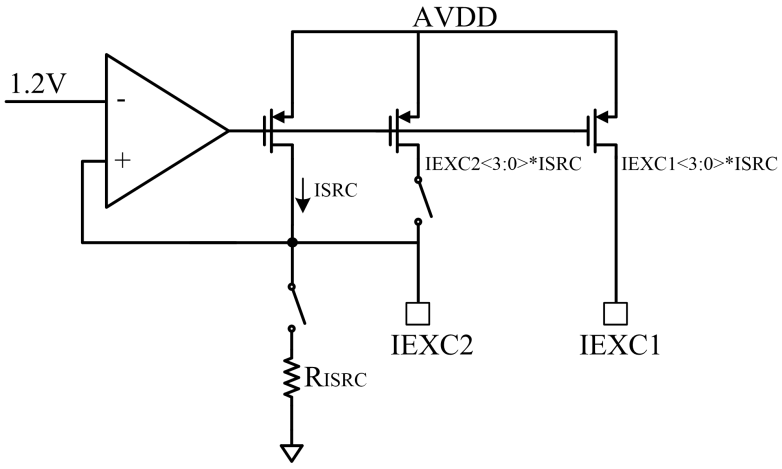

Figure 4.10 Constant Current Driver

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When 'IEXC2'=1111b, external reference resistor is applied at IEXC2 pin instead of internal reference resistor. The temperature drift of current source will be smaller when using accurate reference resistor externally. The current source is only available at IEXC1 pin, which is equal to IEXC1<3:0>*1.2V/R_{ISRC_EXT} .

4.4.2. Internal LDO

A 1.8V LDO is integrated in the NSA2862X to provide power supply for the internal digital circuits. A 100nF decoupling capacitor should be connected at DVDD pin externally.

4.4.3. Power on Reset

A POR block is integrated in the NSA2862X for power on reset and EEPROM loading. When AVDD<2.5V, the chip is in reset state. After AVDD > 2.5V, the POR output is released and EEPROM is loaded afterwards. The POR circuits have 100mV hysteresis, that is, the chip won't go into the reset state again until the AVDD is dropped as low as 2.4V.

4.5. BUILD-IN MCU CORE AND CONTROL LOGICS

4.5.1. EEPROM

57 bytes EEPROM is contained in the NSA2862X to store the chip configurations and sensor calibration coefficients.

4.5.1.1. Loading

The contents of the EEPROM will be loaded into the EEPROM registers automatically after power up or soft-reset with the CRC checking. If the calculated CRC result does not match with what stored in the EEPROM, the 'CRC_ERROR' bit will be set and the analog output state will be decided according to the fault diagnostic and alarm configurations. Another status register bit 'LOADING_END' will be set after the loading completes.

4.5.1.2. Programming

Writing EEPROM registers will not program the EEPROM directly. The contents of the EEPROM registers will be programmed into the EEPROM by following sequence:

1. Set the register byte 'COMMAND' (Reg0x30) with 0x33, to enter EEPROM programming mode;
2. Writing the register byte 'EE_PROG' (Reg0x6A) with 0x7E or 0xFE, to start EEROM programming.

When 0x7E is used, the built-in MCU will first compare the register contents with the EEPROM contents, and only erase and program the bytes with the difference. If 0xFE is used, all EEPROM contents will be erased and then programmed. The programming time is different in these two modes. It is recommended to use 0x7E for programming.

During EEPROM programming, a new CRC check code will be generated according to the contents of the EEPROM registers and will be programmed to the EEPROM simultaneously. The content of the 'EE_PROG' register will automatically come back to 0x00 to indicate the programming is done. A re-powering up or soft-reset is needed to reload the EEPROM contents back to the EEPROM registers to check the programmed value.

4.5.1.3. Lock and Unlock

The EEPROM inside the NSA2862X can be locked by setting the 'EEPROM_LOCK' bit then programming it into the EEPROM. After locked, the EEPROM cannot be programmed again, and only a special EVA-kits provided by NOVOSENSE can unlock it.

4.5.2. Build-in MCU Core

The NSA2862X is integrated with a built-in MCU core, which performs the signal processing, sensor calibration, EEPROM loading and programming etc. The MCU's program code is pre-stored in the internal ROM, which cannot be modified by customers. Please contact NOVOSENSE if a customized MCU program code is needed.

4.5.3. Calibration

The calibration flow inside the NSA2862X is divided into two steps. The first is the DAC calibration, which can erase the offset and sensitivity error induced by the DAC block during voltage or current output mode. The other is sensor calibration, which can compensate the sensor with offset, sensitivity, up to the 2nd order offset temperature drift, up to the 2nd order sensitivity temperature drift, up to the 3rd order non-linearity, and the totally calibration error is less than 0.1% of the full span. Please refer to application note *AN: Sensor Calibration for the NSA2862X* for details

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4.6. FAULT DETECTION AND ALARM

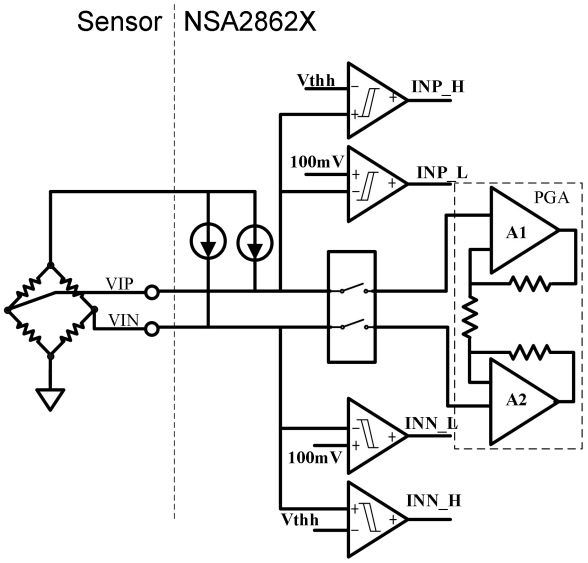

Figure 4.13 Fault diagnostic

4.6.1. Fault Detection

Setting register bit 'BURNOUT_EN'1 enables the fault diagnostics. When diagnostics is enabled, a pair of 100nA burnout current sources is applied to the input of the primary signal channel. Four comparators will be activated to monitor the input voltages. Two comparators compare the input voltage to 100mV and the other two comparators compare the input voltages to upper limit level VTHH. VTHH depends on register bit 'VREF_DIS'. If 'VREF_DIS' = 0, VTHH = VREF-100mV, otherwise VTHH = AVDD-1.1V. If any of the comparator output is asserted, fault is detected and reported in the 'STATUS' register (reg0x02).

4.6.2. Alarm

If any fault is detected, the error status will be written in STATUS register (register address = 0x02).

5.0 SERIAL INTERFACE

Three different serial interfaces (OWI, SPI and I2C) are supported in the NSA2862X to configure registers, program EEPROM and pulling measured data. When register bit 'OWI_WINDOW' = 0, the time between 2.5ms and 20ms after powering up is defined as the OWI entering window. If a special 24 bits OWI entering pattern is detected via OWI pin in this window, the chip enters OWI communication mode, otherwise enters I2C or SPI communication mode. Then, CSB pin is used to further select between I2C and SPI methods, high voltage level or floating indicates the I2C method, low voltage level indicates the SPI method. When 'OWI_WINDOW' = 1, the OWI window becomes infinite length.

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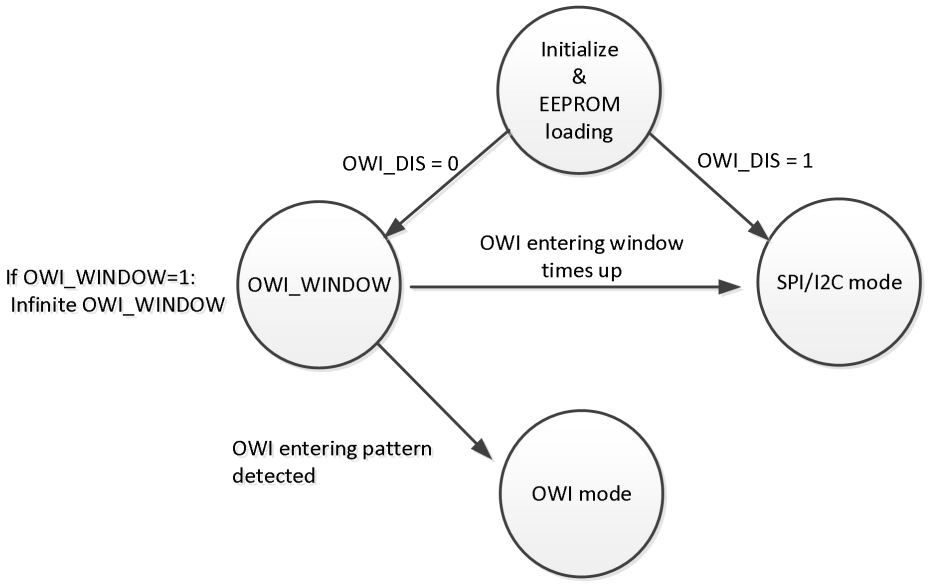

Figure 5.1 Definition of serial communication mode

5.1. OWI PROTOCOL

The NOVOSENSE self-owed One Wire Interface (OWI) protocol is integrated in the NSA2862X. This protocol identifies the data bit transferred by the duty cycle of one rising-to-rising period. Duty cycle more than 5/8 means a logical 1, and less than 3/8 means a logical 0.

5.1.1. Timing Spec

Table5.1: OWI Timing Spec

Symbol	*Description*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*
t_{period}	OWI bit period		20		700	Us
t_{pulse_0}	Duty cycle for 0		1/8	1/4	3/8	t_{period}
t_{pulse_1}	Duty cycle for 1		5/8	3/4	7/8	t_{period}
t_{start}	Start low pulse time		20		4000	Us
t_{stop}	Stop condition time		2			t_{period}

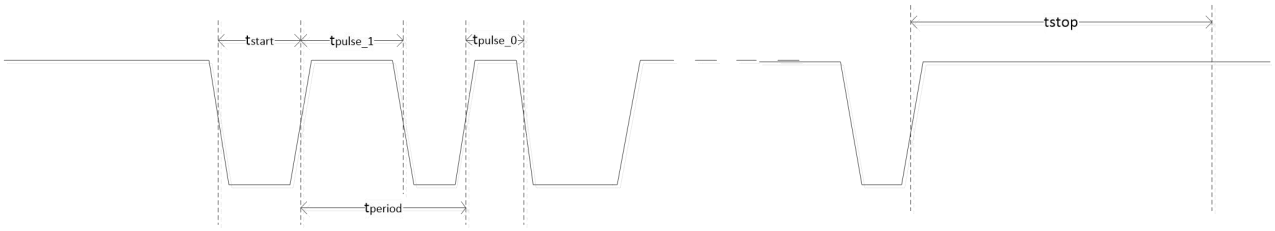

Figure 5.2 OWI Timing

5.1.2. Enter OWI Mode

If 'OWI_WINDOW' = 0, the time between 2.5ms and 20ms after powering up is OWI entering window. If a special 24 bits OWI entering pattern (0xB5A6C0, as shown below) is detected via OWI pin in this window, the chip enters OWI communication mode. Under this setting, the OUT pin is disabled during the OWI window and OWI mode; the OWI pin and the OUT pin can be shorted together to support 3-wire sensor products.

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If 'OWI_WINDOW' = 1, the OWI window's length becomes infinite, the OUT pin is activated during OWI window and OWI mode, and the OWI pin and OUT pin cannot be shorted together.

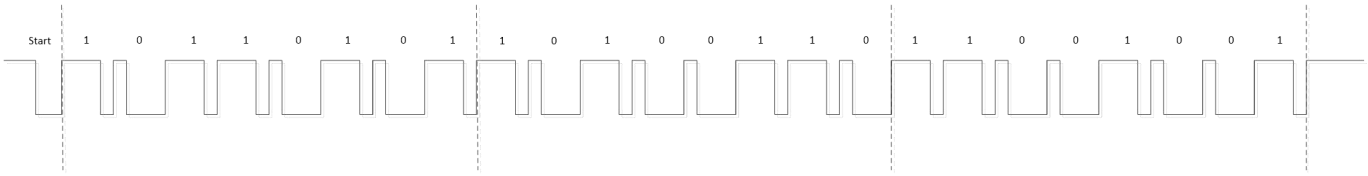

Figure 5.3 OWI Entering Pattern

In OWI communication, the bit period is determined by the period of the last bit of OWI entering pattern, and cannot be changed during the entire communication, so the bit period during OWI communication should keep the same as the OWI entering pattern.

5.1.3. OWI Protocol

The OWI protocol used is defined as follows:

a) Idle State

During inactivity of the bus, OWI line is pulled-up to high voltage level.

b) Start Condition

When OWI line is in idle state a low pulse (return to high) with a pulse width between20us to 4ms indicates a start condition. Every command has to be initiated by a start condition sent by the master. The master can only generate the start condition when the OWI line is in idle state.

c) Stop Condition

After the write or read operation ends, the bus comes back to the idle state automatically. During any time of a transmission, the bus can be set back to the idle state by forcing the OWI line constant high or low voltage level for at least two times of the bit period (tperiod)

d) Addressing

After the start condition, the master sends the addressing information, consisting of an 8-bit register address (MSB first), 2-bit byte number (NO. bits) and a read/write–bit (0–write, 1–read). The register address indicates which register you will write into or read from; the byte number indicates how many bytes will write/read continuously: 00: 1 byte, 01: 2 bytes, 10: 3 bytes, 11: 4 bytes; the read/write-bit indicates it a read operation (0) or write operation (1).

e) Write Operation

During transmission from master to slave (WRITE), the read/write bit is followed by 1/2/3/4 bytes (according to the byte NO. bits) transmitted data (MSB first), and the addressed register and follows will be refreshed to the written data after a stop condition.

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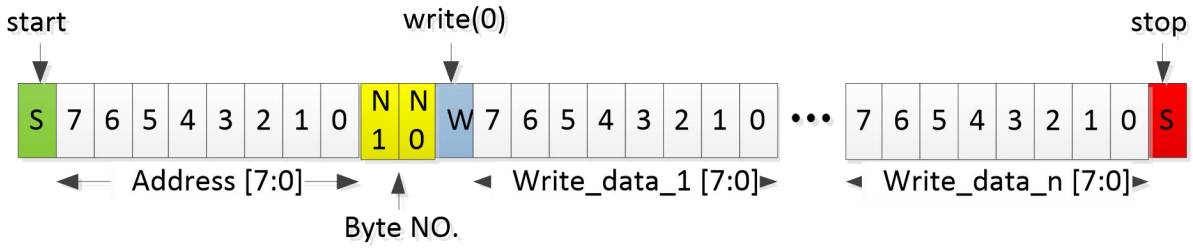

Figure 5.4 OWI Write Operation

f) Read Operation

During transmission from slave to master (READ), the master should set its OWI port as input after the read/write bit is sent, then the slave begins to transmit 1/2/3/4 bytes (according to the byte NO. bits) data (MSB first), which is contented in the addressed register and follows. Each data bytes include 8 bits of data and 2 bits of parity check code C1 and C0.

C1 = Read_data[7] ^ Read_data[5] ^ Read_data[3] ^ Read_data[1];

C0 = Read_data[6] ^ Read_data[4] ^ Read_data[2] ^ Read_data[0];

The master can check the transmission with the parity check code. After all data bytes transmitted, the slave goes back to idle state automatically.

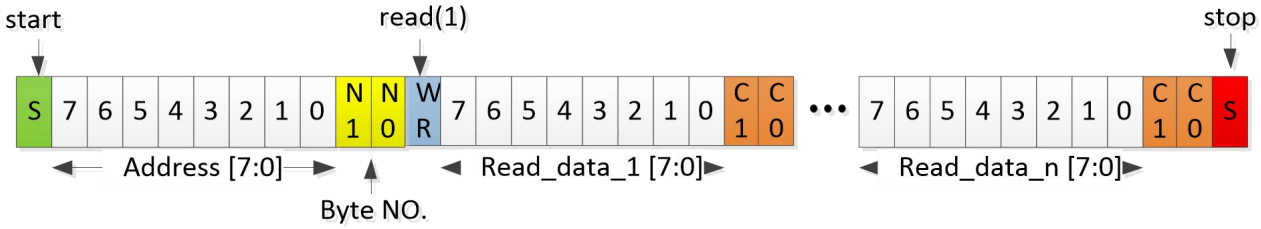

Figure 5.5 OWI Read Operation

5.1.4. Pins and configurations

Two pins (OWI and OUT) and two register bits (OWI_AC_EN and OWI_WINDOW) are related to the OWI communication. Different applications can be supported via different configurations. Please refer to Table5.2 for details.

OWI_AC_EN: 0, single-port communication method with the OWI pin used for both input and output port, which is typically used in 0-5V analog output products. 1, dual-port communication method with the OWI pin as the slave input port and the OUT pin as the slave output port; this method is typically used in the 0-10V and 4-20mA products

OWI_WINDOW: 0, OWI mode should be entered between a 10ms and 80ms window after powering up. 1, the window is infinite and the OWI mode can be entered any time after powering up.

Table5.2 Pin configurations for OWI communications

OWI_AC_EN	*OWI_WINDOW*	*Windows*	*Input Port*	*Output Port*	*Output Mode*	*OUT pin state mode*	*Shorten OUT and OWI*	*Typical Applications*
0	0	10ms-80ms	OWI	OWI	OD	Hz	Supported	3-wire modules with 0～5V output (Short OUT and OWI pins)，external pull-up resistor is needed
0	1	Infinite	OWI	OWI	OD	Signal Output	Not Supported	Cases that signal out and OWI communication are used simultaneously, external pull-up resistor is needed.
1	0	10ms-80ms	OWI	OUT	Push-Pull	OWI output	Supported	3-wire modules with 0-10V output, 2-wire modules with 4-20mA output. 0-5V output modules with big load capacitor
1	1	Infinite	OWI	OUT	Push-Pull	OWI output	Supported	Isolated Transmitter using OWI/OUT pins for Isolated communication

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5.1.5. Quit OWI communication

Writing Reg0x61 with 0x5d during OWI mode can temporarily or permanently quit the OWI communication for output voltage or current measuring. The register byte 'OWI_QUIT_CNT' is used to set the quit time with the LSB = 50ms (0x00 means permanently quit), and the chip will be back into OWI mode again after the quit time's up.

5.2. SPI INTERFACE

5.2.1. Interface specification

Table5.3 SPI interface specifications

Symbol	*Parameter*	*Condition*	*Min*	*Max*	*Unit*
f_{sclk}	Clock frequency	Max load on SDIO or SDO = 25pF		10	MHz
t_{sclk_l}	SLCK low pulse		20		Ns
t_{sclk_h}	SLCK high pulse		20		
T_{sdi_setup}	SDI setup time		20		Ns
T_{sdi_hold}	SDI hold time		20		Ns
T_{sdo_od}	SDO/SDI output delay	Load = 25pF		30	Ns
		Load = 250pF		40	Ns
T_{csb_setup}	CSB setup time		20		Ns
T_{csb_hold}	CSB hold time		40		Ns

The figure below shows the definition of the SPI timing given in Table 5.3

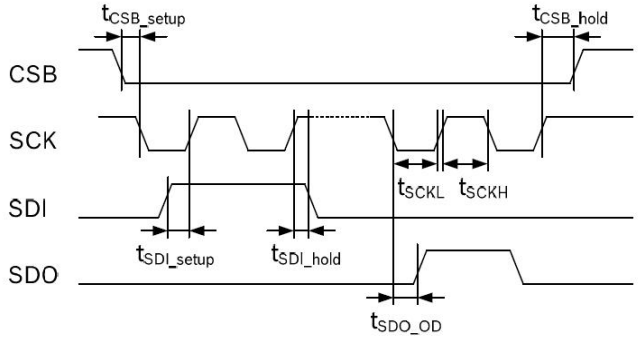

Figure 5.8 SPI timing diagram

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of framing. Once the beginning of the frame has been determined, timing is straightforward. The first phase of the transfer is the instruction phase, which consists of 16 bits followed by data that can be of variable lengths in multiples of 8 bits. If the device is configured with CSB tied low, framing begins with the first rising edge of SCLK.

The instruction phase is the first 16 bits transmitted. As shown in Figure 5.9, the instruction phase is divided into a number of bit fields.

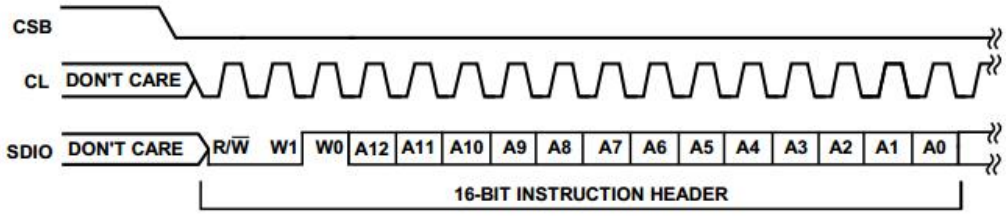

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Figure 5.9 Instruction Phase Bit Field

The first bit in the stream is the read/write indicator bit (R/W). When this bit is high, a read is being requested, otherwise indicates it is a write operation.

W1 and W0 represent the number of data bytes to transfer for either read or write (Table 5.4). If the number of bytes to transfer is three or less (00, 01, or 10), CSB can stall high on byte boundaries. Stalling on a non-byte boundary terminates the communications cycle. If these bits are 11, data can be transferred until CSB transitions high. CSB is not allowed to stall during the streaming process.

The remaining 13 bits represent the starting address of the data sent. If more than one word is being sent, sequential addressing is used, starting with the one specified, and it either increments (LSB first) or decrements (MSB first) based on the mode setting.

Table5.4 W1 and W0 settings

W1:W0	*Action*	*CSB stalling*
00	1 byte of data can be transferred.	Optional
01	2 bytes of data can be transferred.	Optional
10	3 bytes of data can be transferred.	Optional
11	4 or more bytes of data can be transferred. CSB must be held low for entire sequence; otherwise, the cycle is terminated.	No

Data follows the instruction phase. The amount of data sent is determined by the word length (Bit W0 and Bit W1). This can be one or more bytes of data. All data is composed of 8-bit words.

Data can be sent in either MSB-first mode or LSB-first mode (by setting ‘LSB_first’ bit). On power up, MSB-first mode is the default. This can be changed by programming the configuration register. In MSB-first mode, the serial exchange starts with the highest-order bit and ends with the LSB. In LSB-first mode, the order is reversed. (Figure 5.10)

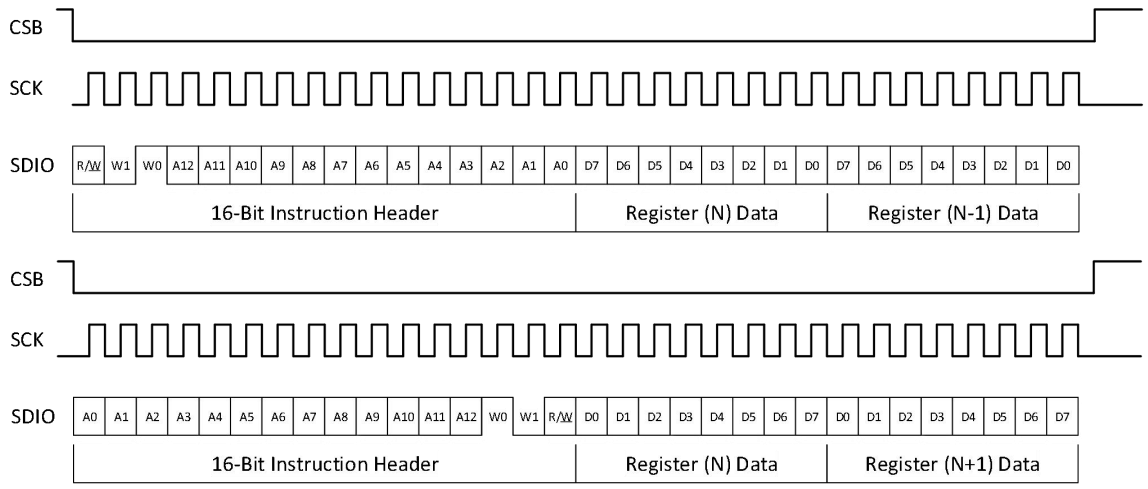

Figure 5.10: MSB First and LSB First Instruction and Data Phases

Register bit ‘SDO_active’ is responsible for activating SDO on devices. If this bit is cleared, then SDO is inactive and read data is routed to the SDIO pin. If this bit is set, read data is placed on the SDO pin. The default for this bit is 1, making SDO active.

5.3. I2C INTERFACEE

I2C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The I2C device address of NSA2300 is shown below. The LSB bit of the 7bits device address is configured via SDO/ADDR pin.

Table5.5 I2C Address.

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A7	A6	A5	A4	A3	A2	A1	W/R
1	1	0	1	1	0	1	0/1

Table5.6 Electrical specification of the I2C interface pins

Symbol	*Parameter*	*Condition*	*Min*	*Max*	*Unit*
f_{scl}	Clock frequency			400	kHz
t_{LOW}	SCL low pulse		1.3		Us
t_{HIGH}	SCL high pulse		0.6		Us
t_{SUDAT}	SDA setup time		0.1		Us
t_{HDDAT}	SDA hold time		0.0		Us
t_{SUSTA}	Setup Time for a repeated start condition		0.6		Us
t_{HDSTA}	Hold time for a start condition		0.6		Us
t_{SUSTO}	Setup Time for a stop condition		0.6		Us
t_{BUF}	Time before a new transmission can start		1.3		Us

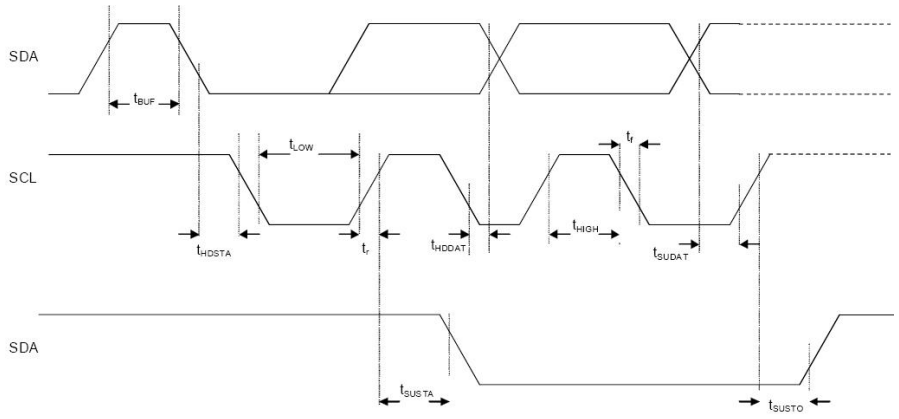

Figure 5.11 I2C Timing Diagram

The I2C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition, SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change value at SDA only when SCL is low.

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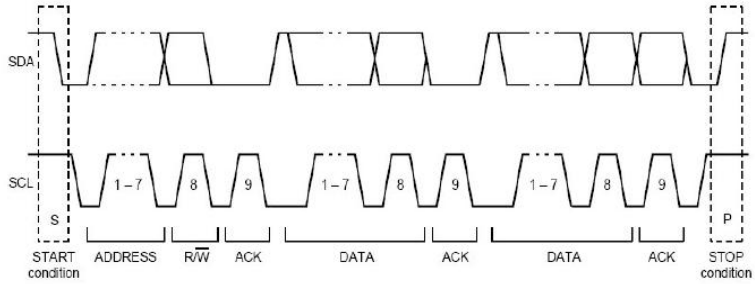

Figure 5.12 I2C Protocol

NSA2862X can support single byte and multiple bytes operation. The data format is shown in the figure below.

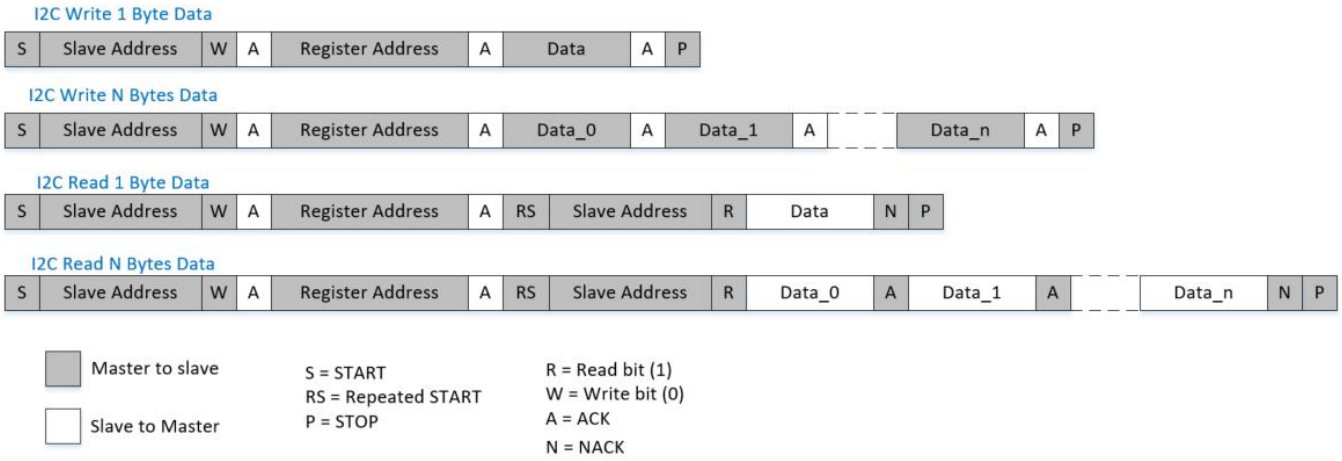

图 5.13 I2C Transfer Format

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6.0 PACKAGE INFORMATION

NSA2862X has only one package type: QFN20. The pin configuration is shown as below:

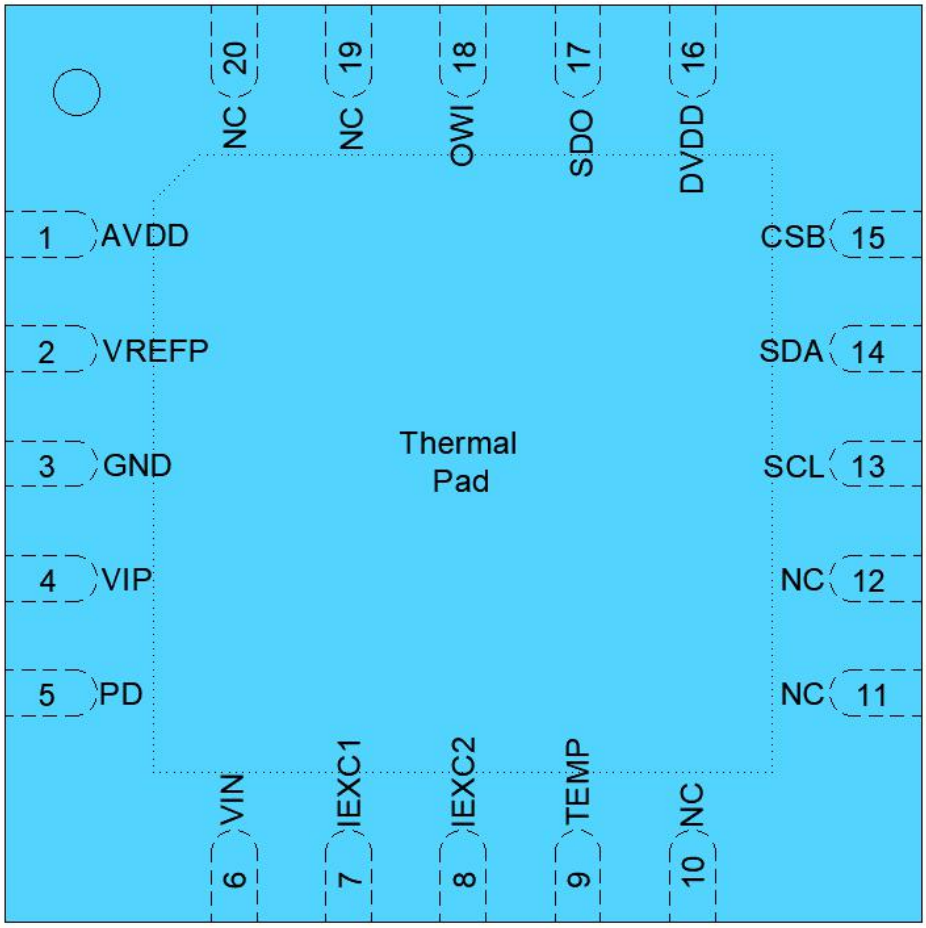

Figure 6.1 QFN20 package pin configuration

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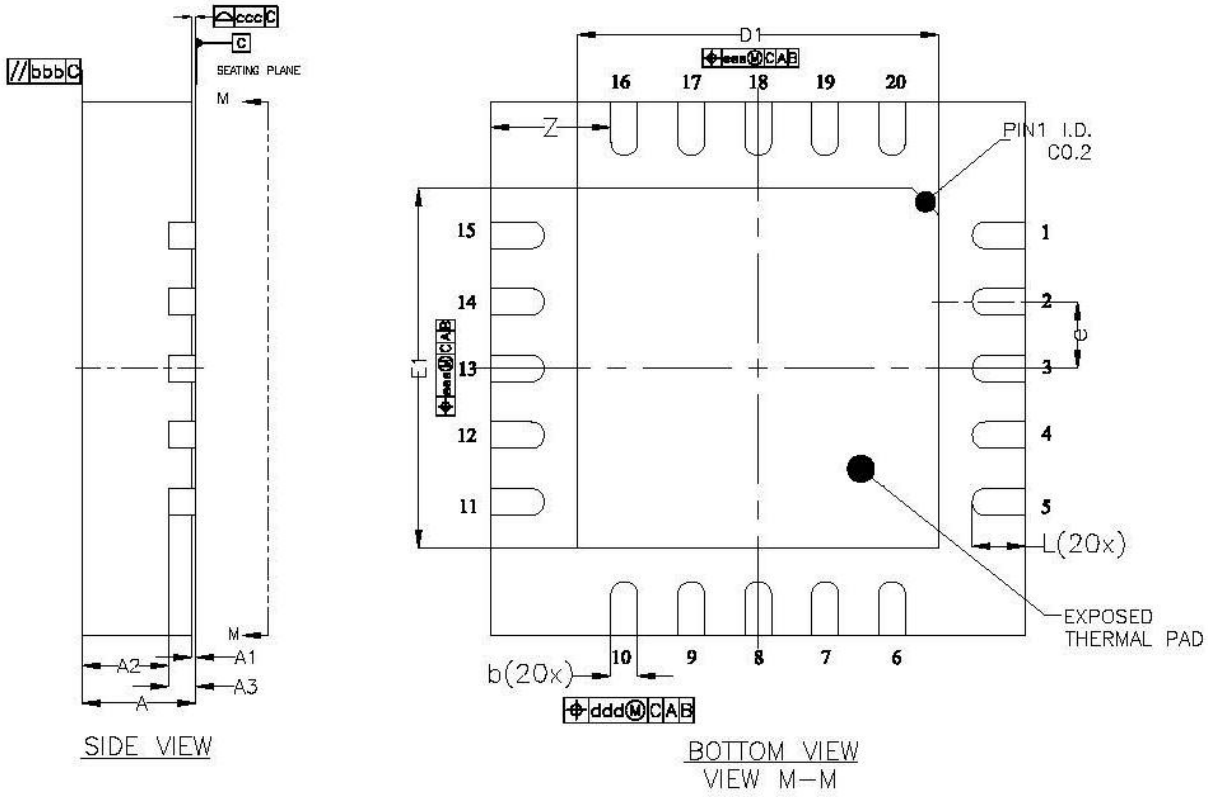

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

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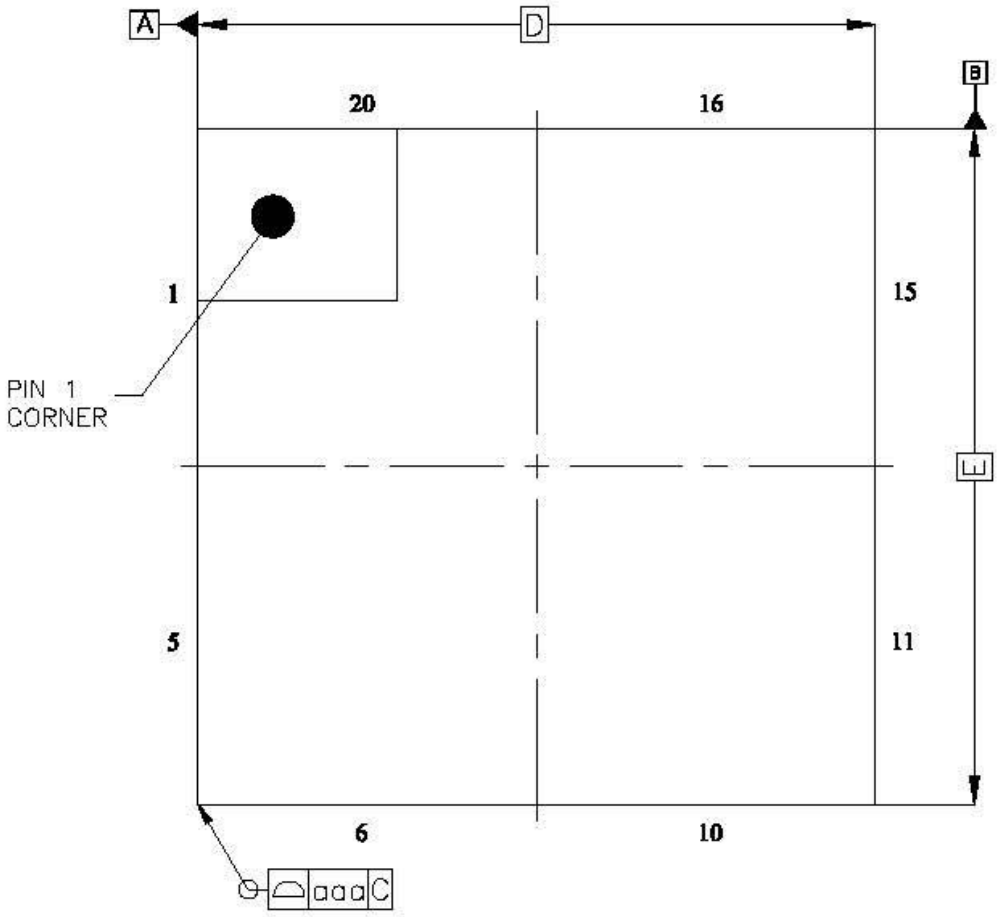

TOP VIEW

DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0.00	—	0.05
MOLD THICKNESS		A2	0.60	0.65	0.70
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.20	0.25
BODY SIZE	X	D	3.95	4.00	4.05
	Y	E	3.95	4.00	4.05
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	D1	2.65	2.70	2.75
	Y	E1	2.65	2.70	2.75
LEAD LENGTH		L	0.35	0.40	0.45
LEAD EDGE TO PKG EDGE		Z	0.9 REF		
Tolerance of form and position					
PACKAGE EDGE TOLERANCE	aaa		0.1		
MOLD FLATNESS	bbb		0.1		
COPLANARITY	ccc		0.08		
LEAD OFFSET	ddd		0.1		
EXPOSED PAD OFFSET	eee		0.1		

Figure 6.2 QFN20 Package

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Table6.1 QFN20 Pin Configuration and Description

Pin NO.	Pin Name	Type	Description
1	AVDD	Supply	Power Supply
2	VREFP	Analog	Reference Voltage Output/Input
3	GND	Supply	Ground
4	VIP	Analog	Analog input positive
5	PD	Analog	Power down input. High: standby mode Low: work mode
6	VIN	Analog	Analog input negative
7	IEXC1	Analog	1st constant current source
8	IEXC2	Analog	2nd constant current source
9	TEMP	Analog	External temperature sensor input (ODR_T≠1111b) External Negative Reference Voltage input (ODR_T=1111b)
10	NC	NC	Must be left floating
11	NC	NC	Must be left floating
12	NC	NC	Must be left floating
13	SCL	Digital Input	I2C/SPI clock signal
14	SDA	Digital I/O	I2C data signal (SDA) or SPI data signal (SDIO)
15	CSB	Digital Input	I2C/SPI mode selection pin, SPI chip selection
16	DVDD	Analog	1.8V DVDD digital LDO output
17	SDO	Digital Input	4-wire SPI date output
18	OWI	Digital Input	One-wire interface
19	NC	NC	Must be left floating
20	NC	NC	Must be left floating

7.0 TYPICAL APPLICATIONS

7.1. TYPICAL APPLICATION

As shown in the diagram below, the wireless sensor system consists of two modules: sensor module and control module. The sensor module includes sensor and NSA2862X. It is responsible for signal acquisition and conditioning. The control module includes low power MCU and wireless transceiver. It is responsible for data communication and system control. The MCU communicates with NSA2862X through 4 wires SPI interface. It can control the sensor module's power mode by PD pin.

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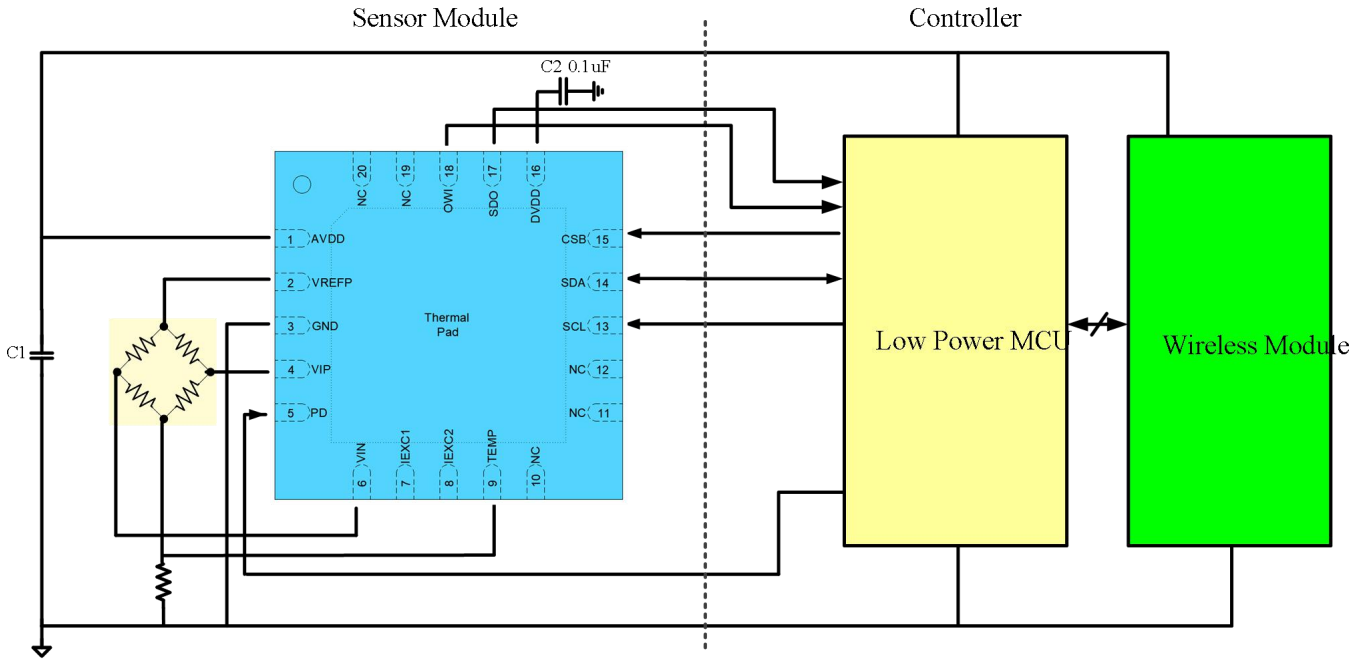

Fig7.1 Typical application diagram

8.0 TAPE/REEL INFORMATION

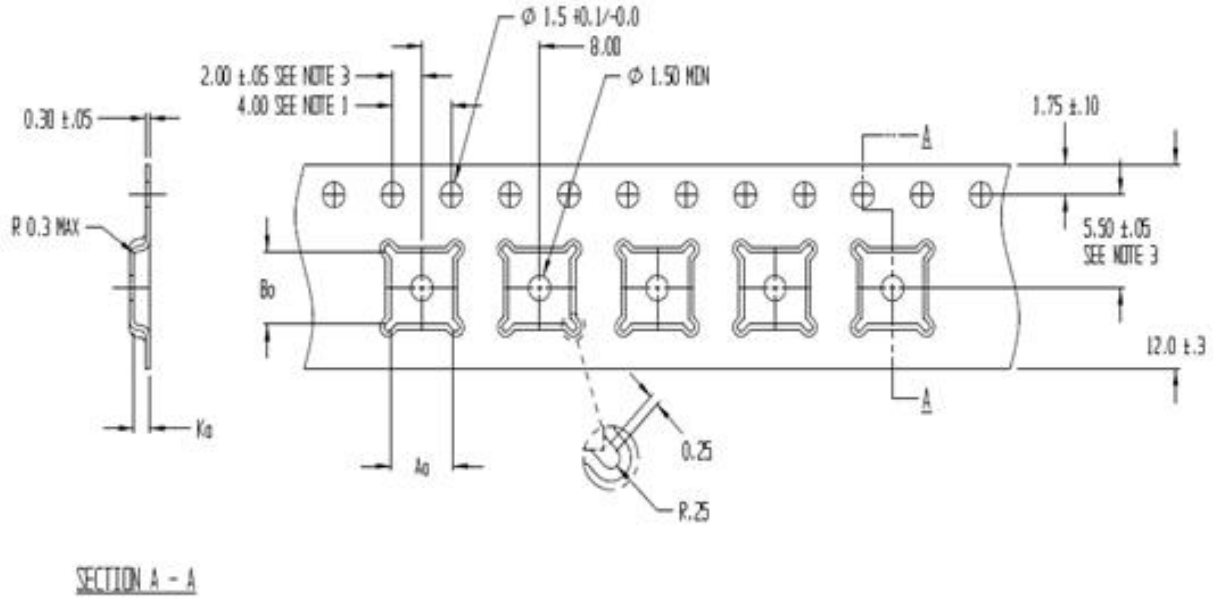

Figure 8.1 Tape/reel digram for QFN20

型号	封装类型	A0 (mm)	B0 (mm)	K0 (mm)	F (mm)	P1 (mm)	W (mm)
NSA2862X-DQNR	QFN20	4.25	4.25	1.1	5.50±0.05	8.00±0.1	16.0±0.3

There is no component at the head and the tail of each tape/reel, where the space is 50cm, as shown in the following figure,

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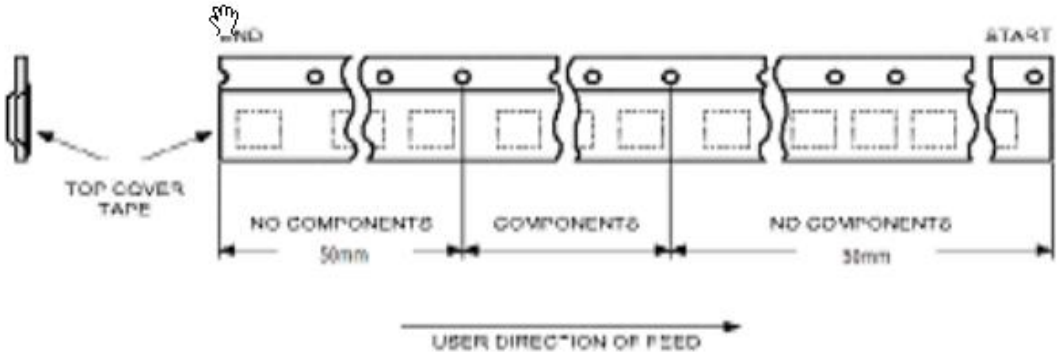
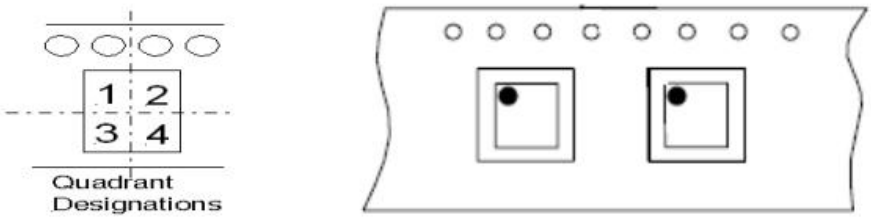


Pin 1 is located at the first quadrant，as shown in the following figure,



9.0 ORDER INFORMATION

Part No.	Unit	Description
NSA2862X-DQNR	2500ea/REEL	20 pin QFN20

10.0 REVISION HISTORY

Revision	Description	Date
1.0	Initial Version	2020/7/15
2.0	Correct some parameters for ver C,fix typo, remove data ready interrupt function of SDO and add more dexcription EEPROM programming.	2021/2/24

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