CBTL01023

3.3 V, one differential channel, 2 : 1 multiplexer/demultiplexer switch for PCI Express Gen3

Rev. 1 — 24 October 2011 Product data sheet

1. General description

CBTL01023 is a single differential channel, 2-to-1 multiplexer/demultiplexer switch for PCI Express Generation 3 (Gen3), or other high-speed serial interface applications. The CBTL01023 can switch one differential signal to one of two locations. Using a unique design technique, NXP has minimized the impedance of the switch such that the attenuation observed through the switch is negligible, and also minimized the channel-to-channel crosstalk, as required by the high-speed serial interface. CBTL01023 allows expansion of existing high speed ports for extremely low power.

2. Features and benefits

- Single bidirectional differential channel, 2 : 1 multiplexer/demultiplexer
- High-speed signal switching for PCIe Gen3 8 Gbit/s
- High bandwidth: 9 GHz at −3 dB
- Low insertion loss:
  - −0.6 dB at 100 MHz
  - −1.5 dB at 4.0 GHz
- Low off-state isolation: −30 dB at 4 GHz
- Low intra-pair skew: 5 ps typical
- V_{DD} operating range: 3.3 V ± 10 %
- Shutdown pin (XSD) for power-saving mode
  - Standby current less than 1 μA
- ESD tolerance:
  - 2000 V HBM
  - 1000 V CDM
- XQFN10 package

3. Applications

- Routing of high-speed differential signals with low signal attenuation
  - PCIe Gen3
  - DisplayPort 1.2
  - USB 3.0
  - SATA 6 Gbit/s

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
CBTL01023GM	XQFN10	plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.55 × 2.00 × 0.50 mm	SOT1049-3

5. Functional diagram

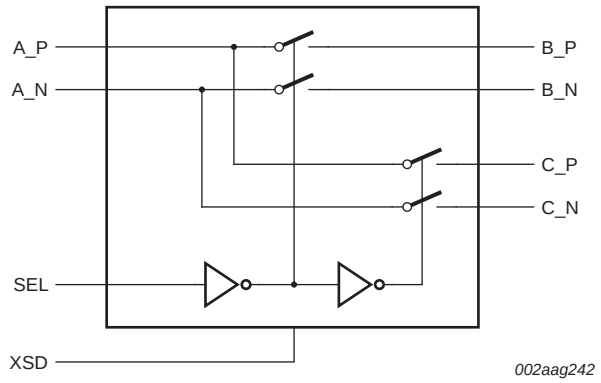
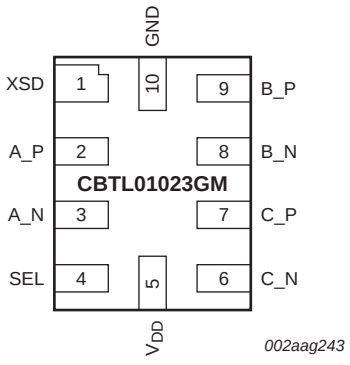


Fig 1. Functional diagram of CBTL01023

6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration for XQFN10

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
A_P	2	I/O	channel 0, port A differential signal input/output
A_N	3	I/O	
B_P	9	I/O	channel 0, port B differential signal input/output
B_N	8	I/O	
C_P	7	I/O	channel 0, port C differential signal input/output
C_N	6	I/O	
SEL	4	CMOS single-ended input	operation mode select SEL = LOW: A ↔ B SEL = HIGH: A ↔ C
XSD	1	CMOS single-ended input	Shutdown pin; should be driven LOW or connected to GND for normal operation. When HIGH, all paths are switched off (non-conducting high-impedance state), and supply current consumption is minimized.
V_{DD}	5	power	positive supply voltage, 3.3 V (± 10 %)
GND	10	power	supply ground

7. Functional description

Refer to Figure 1 “Functional diagram of CBTL01023”.

7.1 Function selection and shutdown function

The CBTL01023 provides a shutdown function to minimize power consumption when the application is not active, but power to the CBTL01023 is provided. The XSD pin (active HIGH) places all channels in high-impedance state (non-conducting) while reducing current consumption to near-zero. When XSD pin is LOW, the device operates normally.

Table 3. Function selection

X = Don’t care.

XSD	SEL	Function
HIGH	X	A_n, B_n and C_n pins are high-Z
LOW	LOW	A_n to B_n and vice versa
LOW	HIGH	A_n to C_n and vice versa

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.3	+4.6	V
T_{case}	case temperature			−40	+85	°C
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	2000	V
		CDM	[2]	-	1000	V

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3.0	3.3	3.6	V
V_I	input voltage		-	-	V_{DD}	V
T_{amb}	ambient temperature	operating in free air	−40	-	+85	°C

10. Static characteristics

Table 6. Static characteristics

V_{DD} = 3.3 V ± 10 %; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{DD}	supply current	operating mode; V_{DD} = max.; XSD = LOW	-	1.30	1.8	mA
		shutdown mode; V_{DD} = max.; XSD = HIGH	-	-	1	µA
I_{IH}	HIGH-level input current	V_{DD} = max.; V_I = V_{DD}	-	-	±5[2]	µA
I_{IL}	LOW-level input current	V_{DD} = max.; V_I = GND	-	-	±5[2]	µA
V_{IH}	HIGH-level input voltage	SEL, XSD pins	$0.65V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage	SEL, XSD pins	-	-	$0.35V_{DD}$	V
V_I	input voltage	differential pins	-	-	2.4	V
		SEL, XSD pins	-	-	V_{DD}	V
V_{IC}	common-mode input voltage		0	-	2	V
V_{ID}	differential input voltage	peak-to-peak	-	-	1.6	V

[1] Typical values are at V_{DD} = 3.3 V, T_{amb} = 25 °C, and maximum loading.

[2] Input leakage current is ±50 µA if differential pairs are pulled to HIGH and LOW.

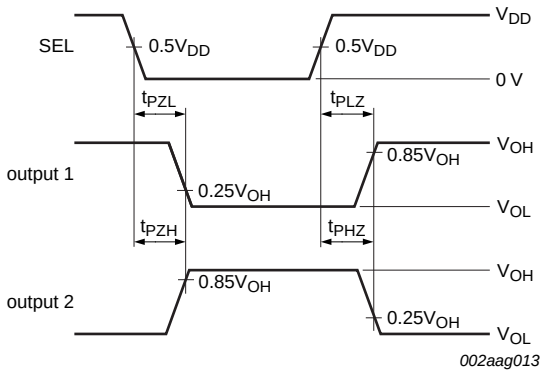
11. Dynamic characteristics

Table 7. Dynamic characteristics

V_{DD} = 3.3 V ± 10 %; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
DDIL	differential insertion loss	channel is OFF				
		f = 4 GHz	-	−30	-	dB
		f = 100 MHz	-	−65	-	dB
		channel is ON				
		f = 4 GHz	-	−1.5	-	dB
		f = 100 MHz	-	−0.6	-	dB
B_{-3dB}	−3 dB bandwidth		-	9	-	GHz
DDRL	differential return loss	f = 4 GHz	-	−7.5	-	dB
		f = 100 MHz	-	−24	-	dB
R_{on}	ON-state resistance	V_{DD} = 3.3 V; V_I = 2 V; I_I = 19 mA	-	6	-	Ω
$C_{io(on)}$	on-state input/output capacitance		-	1.5	-	pF
t_{PD}	propagation delay	from Port A to Port B, or Port A to Port C, or vice versa	-	60	-	ps
Switching characteristics						
$t_{startup}$	start-up time	supply voltage valid or XSD going LOW to channel specified operating conditions	-	-	10	ms
t_{PZH}	OFF-state to HIGH propagation delay		-	-	300	ns
t_{PZL}	OFF-state to LOW propagation delay		-	-	70	ns
t_{PHZ}	HIGH to OFF-state propagation delay		-	-	50	ns
t_{PLZ}	LOW to OFF-state propagation delay		-	-	50	ns
$t_{sk(dif)}$	differential skew time	intra-pair	-	5	-	ps

[1] Typical values are at V_{DD} = 3.3 V; T_{amb} = 25 °C, and maximum loading.



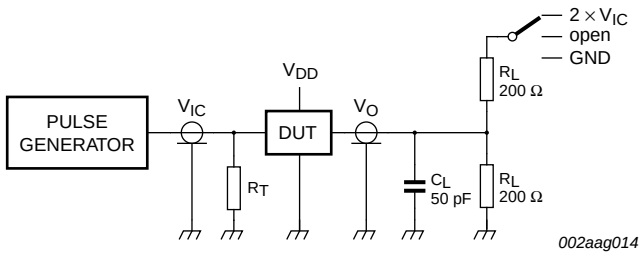
Output 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.

Output 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

The outputs are measured one at a time with one transition per measurement.

Fig 3. Voltage waveforms for enable and disable times

12. Test information



C_L = load capacitance; includes jig and probe capacitance.

R_T = termination resistance; should be equal to Z_o of the pulse generator.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 5 MHz; Z_o = 50 Ω; $t_r \leq 2.5$ ns; $t_f \leq 2.5$ ns.

Fig 4. Test circuitry for switching times

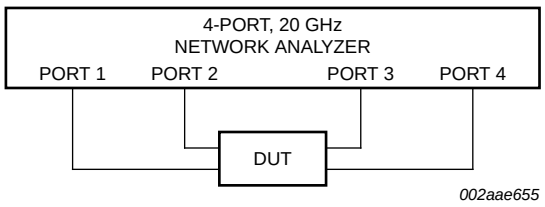


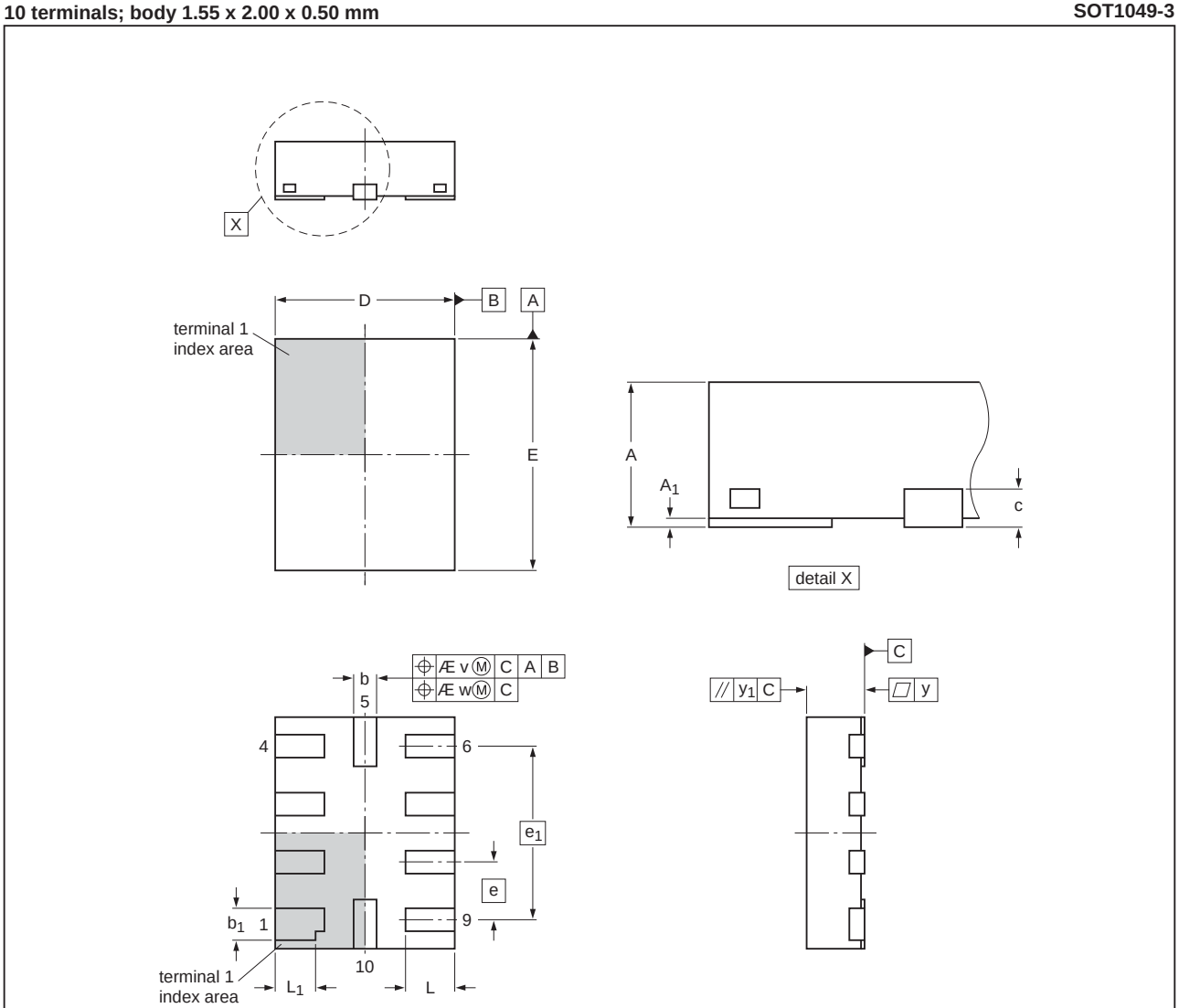
Fig 5. Test circuit

Table 8. Test data

Test	Load		Switch
	C_L	R_L	
t_{PLZ}, t_{PZL} (output on B side)	50 pF	200 Ω	2 × V_{IC}
t_{PHZ}, t_{PZH} (output on B side)	50 pF	200 Ω	GND
t_{PD}	-	200 Ω	open

13. Package outline

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.55 x 2.00 x 0.50 mm **SOT1049-3**



Dimensions

Unit(1)		A	A_1	b	b_1	c	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	max	0.5	0.05	0.25	0.33		1.65	2.1			0.48	0.40				
	nom			0.20	0.28	0.127	1.55	2.0	0.5	1.5	0.43	0.35	0.1	0.05	0.05	0.05
	min		0.00	0.15	0.23		1.45	1.9			0.38	0.30				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1049-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1049-3	- - -	MO255	- - -			~~10-12-06~~ 11-03-30

Fig 6. Package outline SOT1049-3 (XQFN10)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 7) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020C)

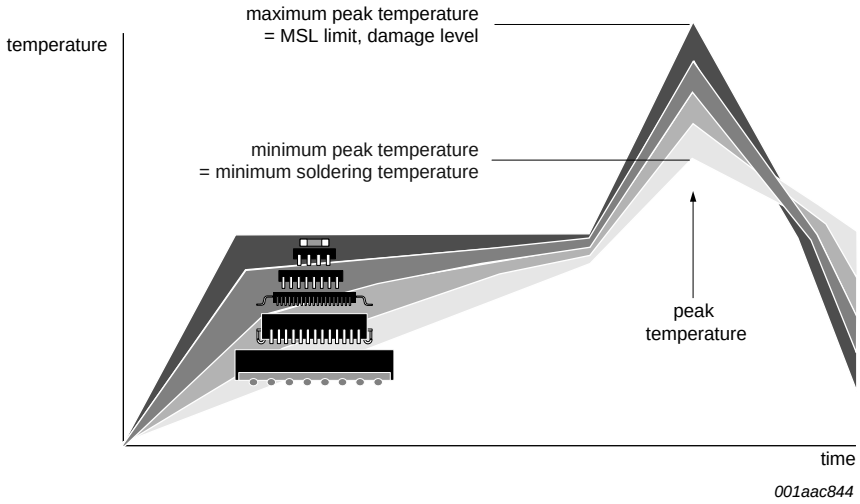
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 7.



MSL: Moisture Sensitivity Level

Fig 7. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged-Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
I/O	Input/Output
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PRR	Pulse Repetition Rate
SATA	Serial Advanced Technology Attachment
USB	Universal Serial Bus

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTL01023 v.1	20111024	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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19. Contents

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Date of release: 24 October 2011
Document identifier: CBTL01023