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MOSFET – Power, Single, N-Channel

100 V, 4.3 mΩ, 113 A



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NTMFS4D2N10MD

Features

- Shielded Gate MOSFET Technology
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Low Q_{RR} , Soft Recovery Body Diode
- Low Q_{OSS} to Improve Light Load Efficiency
- These Devices are Pb-Free, Halogen Free/BFR Free, Beryllium Free and are RoHS Compliant

Typical Applications

- Primary Switch in Isolated DC-DC Converter
- Synchronous Rectification (SR) in DC-DC and AC-DC
- AC-DC Adapters (USB PD) SR
- Load Switch, Hotswap, and ORing Switch
- BLDC Motor and Solar Inverter

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Value | Unit |
|--|----------------|-------------|------------------|
| Drain-to-Source Voltage | V_{DSS} | 100 | V |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V |
| Continuous Drain Current $R_{\theta JC}$ (Note 1) | I_D | 113 | A |
| Power Dissipation $R_{\theta JC}$ (Note 1) | | | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2) | I_D | 16.4 | A |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2) | | | |
| Pulsed Drain Current | I_{DM} | 763 | A |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ |
| Source Current (Body Diode) | I_S | 110 | A |
| Single Pulse Drain-to-Source Avalanche Energy ($I_{AV} = 18\text{ A}$) (Note 6) | E_{AS} | 486 | mJ |
| Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s) | T_L | 300 | $^\circ\text{C}$ |

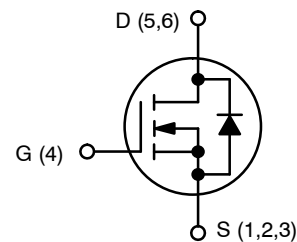
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

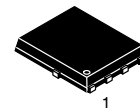
| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|---------------------------|
| Junction-to-Case – Steady State (Note 1) | $R_{\theta JC}$ | 0.95 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient – Steady State (Note 1) | $R_{\theta JA}$ | 45 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using 1 in² pad size, 1 oz. Cu pad.

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | I_D MAX |
|---------------|------------------|-----------|
| 100 V | 4.3 mΩ @ 10 V | 113 A |
| | 7.1 mΩ @ 6 V | |

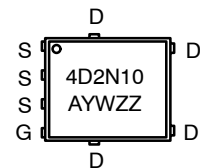


N-CHANNEL MOSFET



DFN5 (SO-8FL) CASE 488AA STYLE 1

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

| Device | Package | Shipping† |
|------------------|----------------|--------------------|
| NTMFS4D2N10MDT1G | DFN5 (Pb-Free) | 1500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMFS4D2N10MD

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-------------------|--|---------------------------|-----|-----|----------------------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 100 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | $I_D = 250\ \mu\text{A}$, ref to 25°C | | 60 | | mV/ $^\circ\text{C}$ |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$ | $T_J = 25^\circ\text{C}$ | | 1.0 | μA |
| | | | $T_J = 125^\circ\text{C}$ | | 100 | |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$ | | | 100 | nA |

ON CHARACTERISTICS (Note 3)

| | | | | | | |
|-----------------------------------|------------------|--|---|------|-----|----------------------|
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}, I_D = 239\ \mu\text{A}$ | 2 | | 4 | V |
| Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | $I_D = 239\ \mu\text{A}$, ref to 25°C | | -7.9 | | mV/ $^\circ\text{C}$ |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 46\text{ A}$ | | 3.8 | 4.3 | $\text{m}\Omega$ |
| | | $V_{GS} = 6\text{ V}, I_D = 23\text{ A}$ | | 5.7 | 7.1 | |
| Forward Transconductance | g_{FS} | $V_{DS} = 8\text{ V}, I_D = 46\text{ A}$ | | 105 | | S |
| Gate-Resistance | R_G | $T_A = 25^\circ\text{C}$ | | 0.97 | 1.6 | Ω |

CHARGES & CAPACITANCES

| | | | | | | |
|------------------------------|--------------|---|--|------|----|-------------|
| Input Capacitance | C_{ISS} | $V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$ | | 3100 | | pF |
| Output Capacitance | C_{OSS} | | | 800 | | |
| Reverse Transfer Capacitance | C_{RSS} | | | 23 | | |
| Output Charge | Q_{OSS} | $V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$ | | 63.4 | | nC |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 6\text{ V}, V_{DS} = 50\text{ V}, I_D = 46\text{ A}$ | | 25 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 46\text{ A}$ | | 40 | 60 | |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | 10 | | |
| Gate-to-Source Charge | Q_{GS} | | | 15 | | |
| Gate-to-Drain Charge | Q_{GD} | | | 6.7 | 10 | |
| Plateau Voltage | V_{GP} | | | 5.0 | | |

SWITCHING CHARACTERISTICS (Note 3)

| | | | | | | |
|---------------------|--------------|--|--|-----|--|----|
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 46\text{ A}, R_G = 6\ \Omega$ | | 21 | | ns |
| Rise Time | t_r | | | 9.5 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | 34 | | |
| Fall Time | t_f | | | 6.5 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

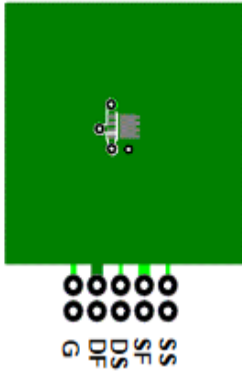
| | | | | | | | |
|-------------------------|----------|---|---------------------------|------|------|----|---|
| Forward Diode Voltage | V_{SD} | $V_{GS} = 0\text{ V}, I_S = 46\text{ A}$ | $T_J = 25^\circ\text{C}$ | | 0.85 | | V |
| | | | $T_J = 125^\circ\text{C}$ | | 0.73 | | |
| Reverse Recovery Time | t_{RR} | $V_{GS} = 0\text{ V}, di_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 23\text{ A}$ | | 23.1 | | ns | |
| Reverse Recovery Charge | Q_{RR} | | | 196 | | nC | |
| Reverse Recovery Time | t_{RR} | $V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 46\text{ A}$ | | 52.6 | | ns | |
| Reverse Recovery Charge | Q_{RR} | | | 66.1 | | nC | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

4. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

NTMFS4D2N10MD



a) 45°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 111°C/W when mounted on a minimum pad of 2 oz copper.

5. Pulse Test: pulse width < 300 μ s, duty cycle < 2%.
6. E_{AS} of 486 mJ is based on started $T_J = 25^\circ\text{C}$, $I_{AS} = 18\text{ A}$, $V_{DD} = 90\text{ V}$, $V_{GS} = 15\text{ V}$. 100% test at $I_{AS} = 51.5\text{ A}$.
7. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

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TYPICAL CHARACTERISTICS

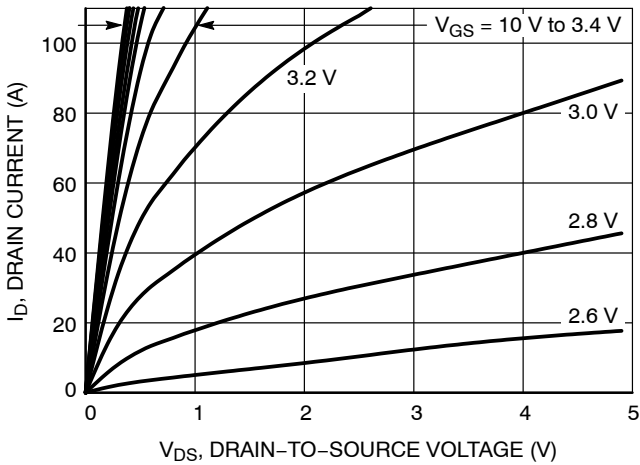


Figure 1. On-Region Characteristics

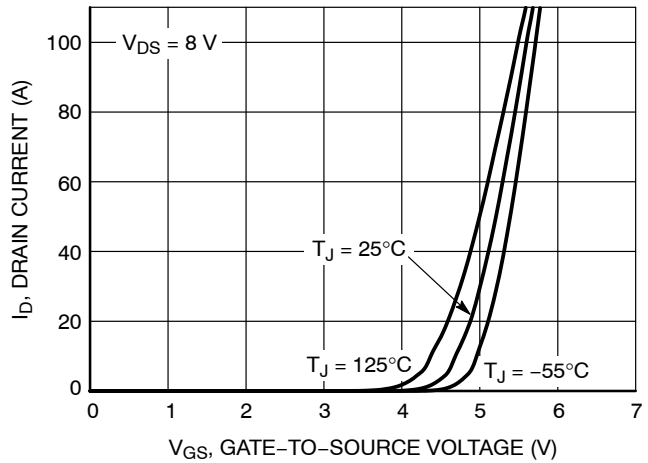


Figure 2. Transfer Characteristics

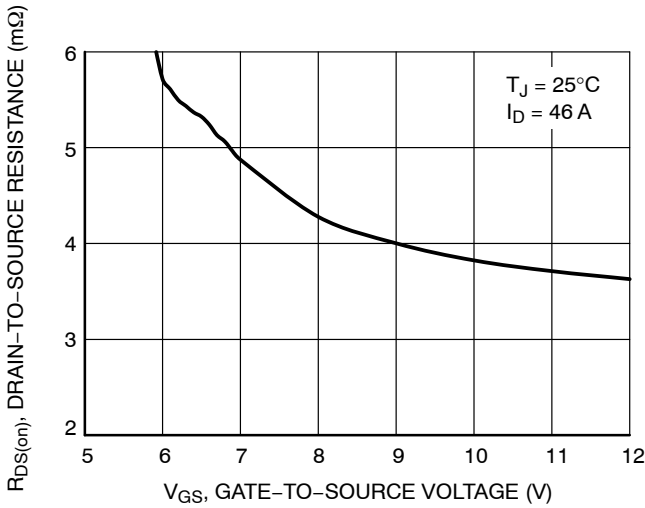


Figure 3. On-Resistance vs. Gate-to-Source Voltage

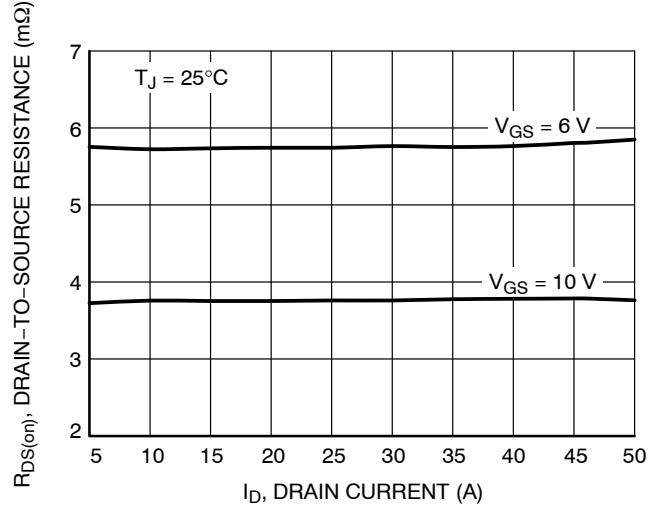


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

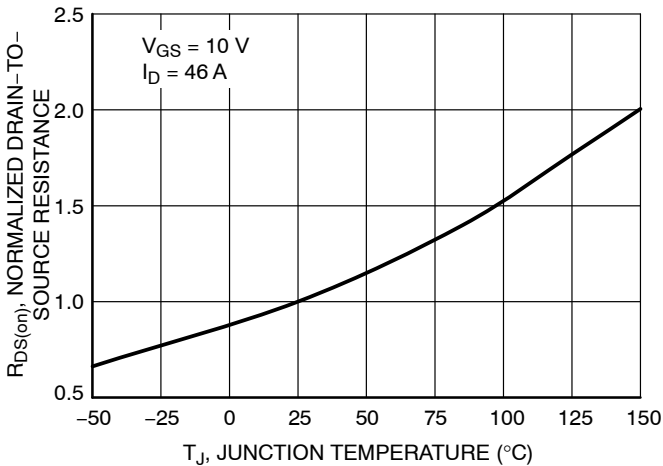


Figure 5. On-Resistance Variation with Temperature

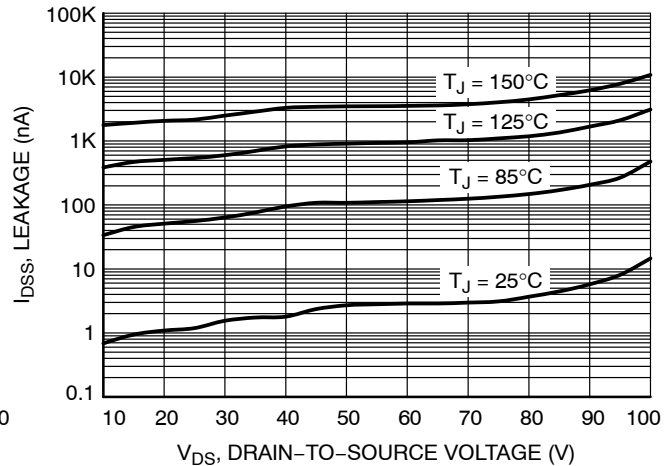


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

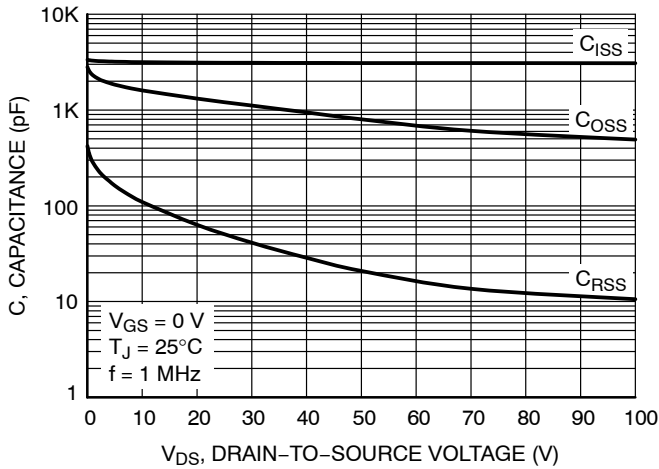


Figure 7. Capacitance Variation

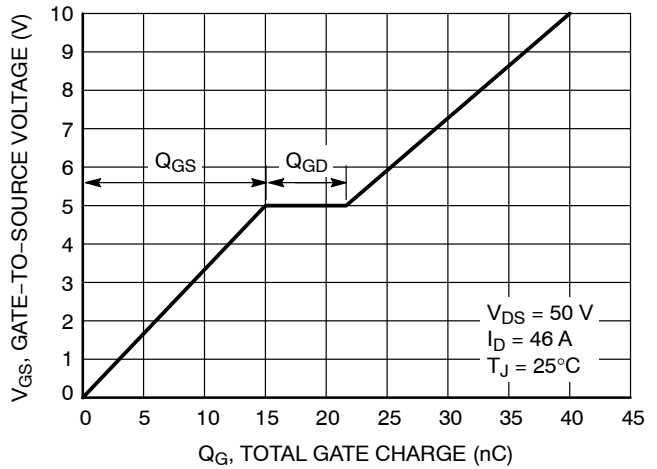


Figure 8. Gate-to-Source vs. Total Charge

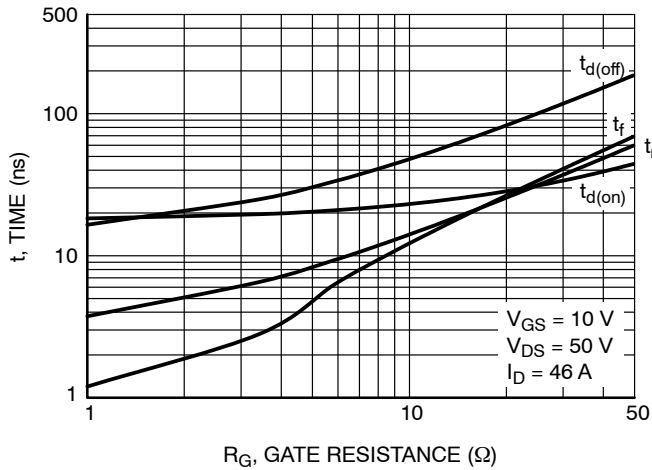


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

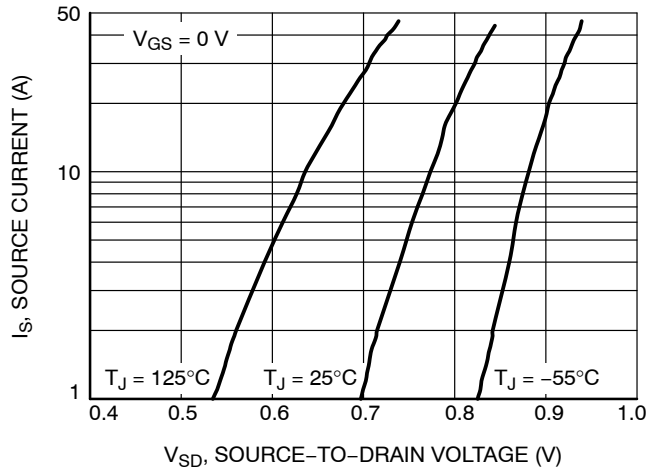


Figure 10. Diode Forward Voltage vs. Current

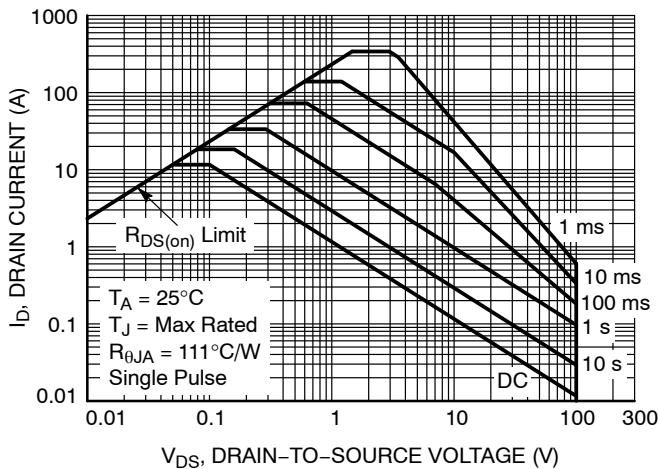


Figure 11. Maximum Rated Forward Biased Safe Operating Area

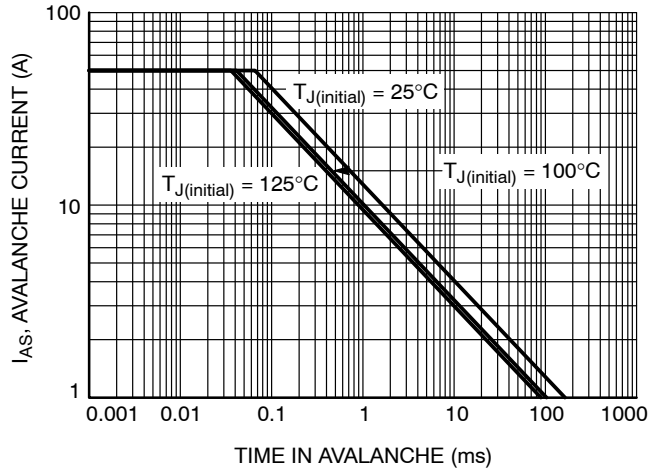


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

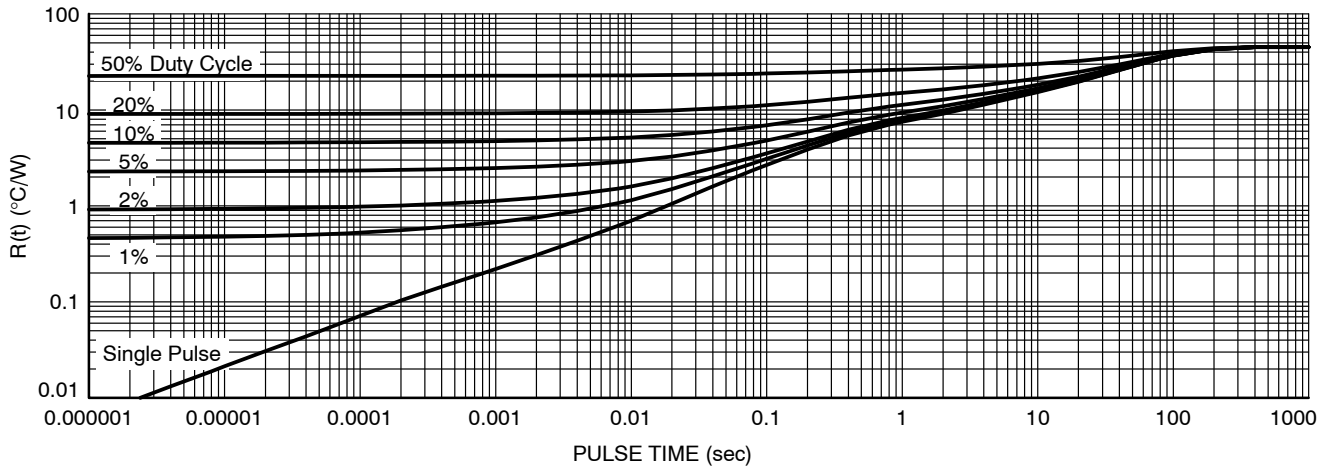


Figure 13. Thermal Characteristics

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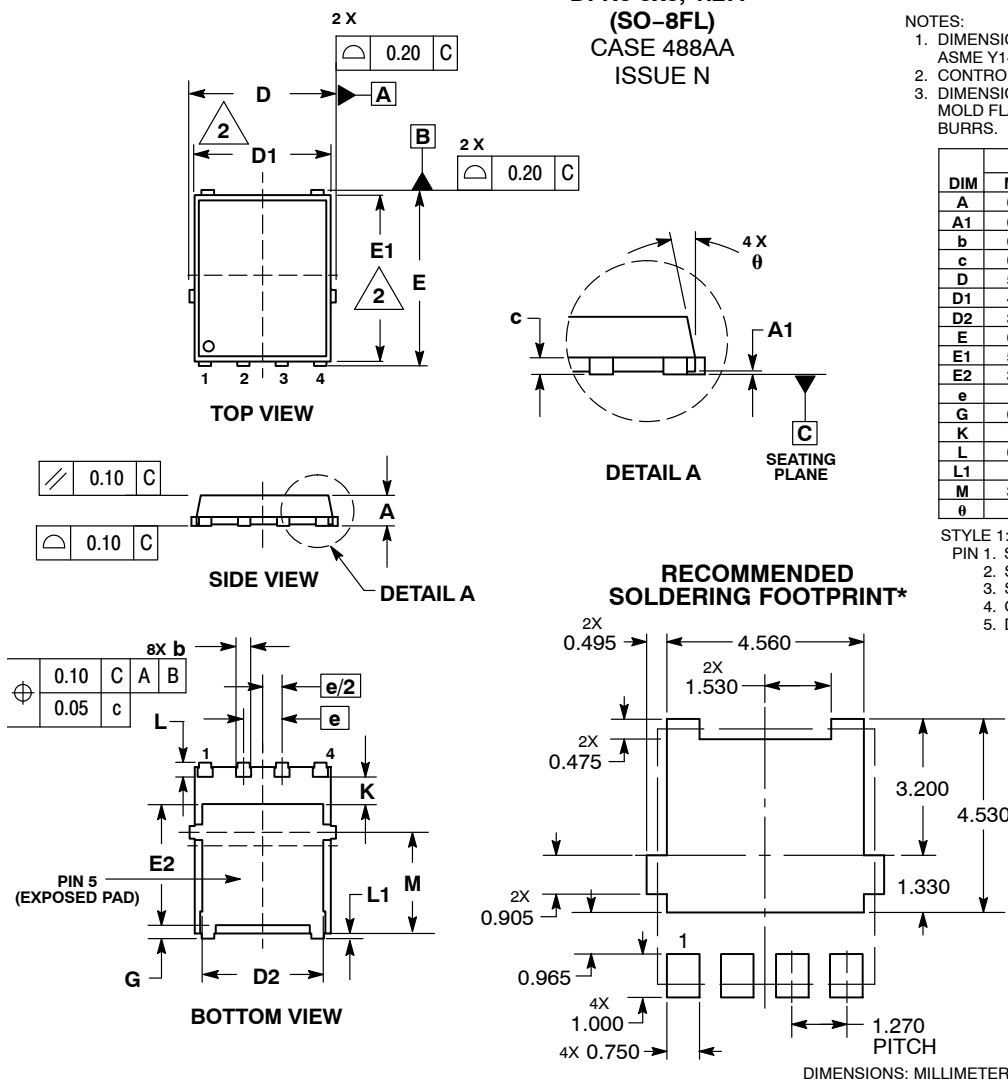
PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|------|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | --- | 0.05 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.23 | 0.28 | 0.33 |
| D | 5.00 | 5.15 | 5.30 |
| D1 | 4.70 | 4.90 | 5.10 |
| D2 | 3.80 | 4.00 | 4.20 |
| E | 6.00 | 6.15 | 6.30 |
| E1 | 5.70 | 5.90 | 6.10 |
| E2 | 3.45 | 3.65 | 3.85 |
| e | 1.27 BSC | | |
| G | 0.51 | 0.575 | 0.71 |
| K | 1.20 | 1.35 | 1.50 |
| L | 0.51 | 0.575 | 0.71 |
| L1 | 0.125 REF | | |
| M | 3.00 | 3.40 | 3.80 |
| θ | 0° | --- | 12° |

- STYLE 1:
1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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