NTJD4105C

MOSFET – Small Signal, Complementary, SC-88
20 V / -8.0 V, +0.63 A / -0.775 A

ON Semiconductor®

http://onsemi.com

Features

- Complementary N and P Channel Device
- Leading −8.0 V Trench for Low $R_{DS(on)}$ Performance
- ESD Protected Gate − ESD Rating: Class 1
- SC−88 Package for Small Footprint (2 x 2 mm)
- Pb−Free Packages are Available

Applications

- DC−DC Conversion
- Load/Power Switching
- Single or Dual Cell Li−Ion Battery Supplied Devices
- Cell Phones, MP3s, Digital Cameras, PDAs

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D Max
N−Ch 20 V	0.29 Ω @ 4.5 V	0.63 A
	0.36 Ω @ 2.5 V	
P−Ch −8.0 V	0.22 Ω @ −4.5 V	−0.775 A
	0.32 Ω @ −2.5 V	
	0.51 Ω @ −1.8 V	

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage		N−Ch	V_{DSS}	20	V
		P−Ch		−8.0	
Gate−to−Source Voltage		N−Ch	V_{GS}	±12	V
		P−Ch		±8.0	
Continuous Drain Current − Steady State (Based on $R_{\theta JA}$)	N−Ch	T_A = 25°C	I_D	0.63	A
		T_A = 85°C		0.46	
	P−Ch	T_A = 25°C		−0.775	
		T_A = 85°C		−0.558	
Continuous Drain Current − Steady State (Based on $R_{\theta JL}$)	N−Ch	T_A = 25°C		0.91	
		T_A = 85°C		0.65	
	P−Ch	T_A = 25°C		−1.1	
		T_A = 85°C		−0.8	
Pulsed Drain Current		tp ≤ 10 μs	I_{DM}	±1.2	A
Power Dissipation − Steady State (Based on $R_{\theta JA}$)		T_A = 25°C	P_D	0.27	W
		T_A = 85°C		0.14	
Power Dissipation − Steady State (Based on $R_{\theta JL}$)		T_A = 25°C		0.55	
		T_A = 85°C		0.29	
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)		N−Ch	I_S	0.63	A
		P−Ch		−0.775	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

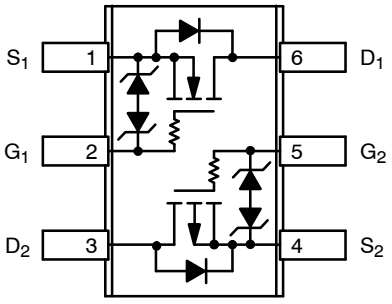
THERMAL RESISTANCE RATINGS (Note 1)

Junction−to−Ambient − Steady State	Typ	$R_{\theta JA}$	400	°C/W
	Max		460	
Junction−to−Lead (Drain) − Steady State	Typ	$R_{\theta JL}$	194	
	Max		226	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 oz Cu area = 0.9523 in sq.

SOT−363
SC−88 (6−LEADS)

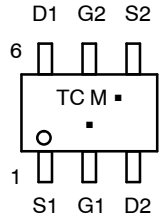


Top View

MARKING DIAGRAM & PIN ASSIGNMENT

1

SC−88/SOT−363
CASE 419B
STYLE 28



TC = Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Condition		Min	Typ	Max	Units
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	N	V_{GS} = 0 V	I_D = 250 μA	20	27		V
		P		I_D = −250 μA	−8.0	−10.5		
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$ / T_J	N				22		mV/ °C
		P				−6.0		
Zero Gate Voltage Drain Current	I_{DSS}	N	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 25 °C			1.0	μA
		P	V_{GS} = 0 V, V_{DS} = −6.4 V				1.0	
Gate−to−Source Leakage Current	I_{GSS}	N	V_{DS} = 0 V	V_{GS} = ±12 V			10	μA
		P		V_{GS} = ±8.0			10	
ON CHARACTERISTICS (Note 2)								
Gate Threshold Voltage	$V_{GS(TH)}$	N	V_{GS} = V_{DS}	I_D = 250 μA	0.6	0.92	1.5	V
		P		I_D = −250 μA	−0.45	−0.83	−1.0	
Gate Threshold Temperature Coefficient	$V_{GS(TH)}$ / T_J	N				−2.1		−mV/ °C
		P				2.2		
Drain−to−Source On Resistance	$R_{DS(on)}$	N	V_{GS} = 4.5 V I_D = 0.63 A			0.29	0.375	Ω
		P	V_{GS} = −4.5 V, I_D = −0.57 A			0.22	0.30	
		N	V_{GS} = 2.5 V, I_D = 0.40 A			0.36	0.445	
		P	V_{GS} = −2.5 V, I_D = −0.48 A			0.32	0.46	
		P	V_{GS} = −1.8 V, I_D = −0.20 A			0.51	0.90	
Forward Transconductance	g_{FS}	N	V_{DS} = 4.0 V I_D = 0.63 A			2.0		S
		P	V_{DS} = −4.0 V, I_D = −0.57 A			2.0		
CHARGES AND CAPACITANCES								
Input Capacitance	C_{ISS}	N	f = 1 MHz, V_{GS} = 0 V	V_{DS} = 20 V		33	46	pF
		P		V_{DS} = −8.0V		160	225	
Output Capacitance	C_{OSS}	N		V_{DS} = 20 V		13	22	
		P		V_{DS} = −8.0 V		38	55	
Reverse Transfer Capacitance	C_{RSS}	N		V_{DS} = 20 V		2.8	5.0	
		P		V_{DS} = −8.0 V		28	40	
Total Gate Charge	$Q_{G(TOT)}$	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 0.7 A			1.3	3.0	nC
		P	V_{GS} = −4.5 V, V_{DS} = −5.0 V, I_D = −0.6 A			2.2	4.0	
Threshold Gate Charge	$Q_{G(TH)}$	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 0.7 A			0.1		
		P	V_{GS} = −4.5 V, V_{DS} = −5.0 V, I_D = −0.6 A			0.1		
Gate−to−Source Charge	Q_{GS}	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 0.7 A			0.2		
		P	V_{GS} = −4.5 V, V_{DS} = −5.0 V, I_D = −0.6 A			0.5		
Gate−to−Drain Charge	Q_{GD}	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 0.7 A			0.4		
		P	V_{GS} = −4.5 V, V_{DS} = −5.0 V, I_D = −0.6 A			0.5		
SWITCHING CHARACTERISTICS (Note 3)								
Turn−On Delay Time	$t_{d(ON)}$	N	V_{GS} = 4.5 V, V_{DD} = 10 V, I_D = 0.5 A, R_G = 20 Ω			0.083		μs
Rise Time	t_r					0.227		
Turn−Off Delay Time	$t_{d(OFF)}$					0.786		
Fall Time	t_f					0.506		
Turn−On Delay Time	$t_{d(ON)}$	P	V_{GS} = −4.5 V, V_{DD} = −4.0 V, I_D = −0.5 A, R_G = 8.0 Ω			0.013		
Rise Time	t_r					0.023		
Turn−Off Delay Time	$t_{d(OFF)}$					0.050		
Fall Time	t_f					0.036		
DRAIN−SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	N	V_{GS} = 0 V, T_J = 25°C	I_S = 0.23 A		0.76	1.1	V
		P		I_S = −0.23 A		0.76	1.1	
		N	V_{GS} = 0 V, T_J = 125°C	I_S = 0.23 A		0.63		
		P		I_S = −0.23 A		0.63		
Reverse Recovery Time	t_{RR}	N	V_{GS} = 0 V, d_{IS}/d_t = 90 A/μs	I_S = 0.23 A		0.410		μs
		P		I_S = −0.23 A		0.078		

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL N−CHANNEL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

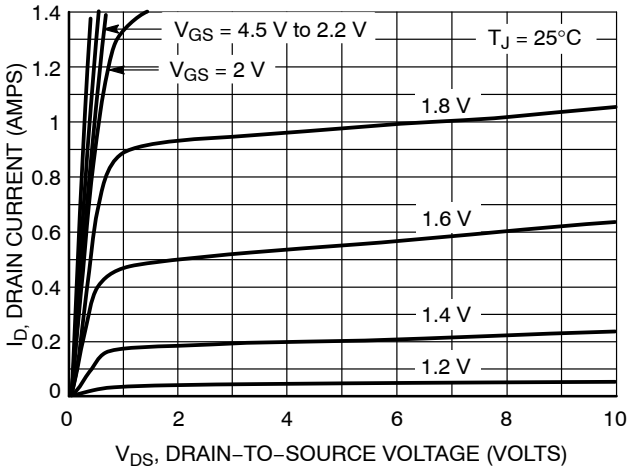


Figure 1. On−Region Characteristics

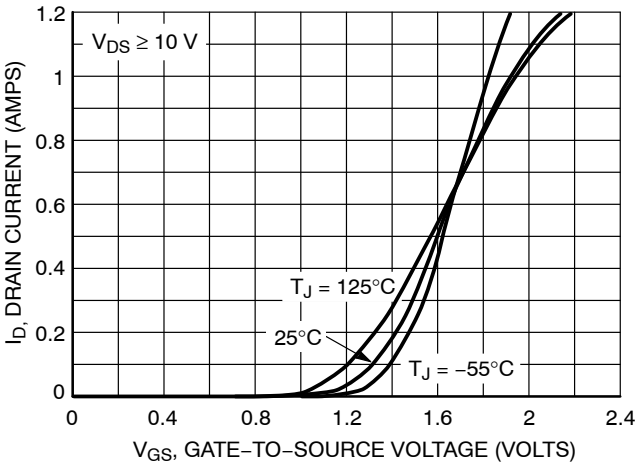


Figure 2. Transfer Characteristics

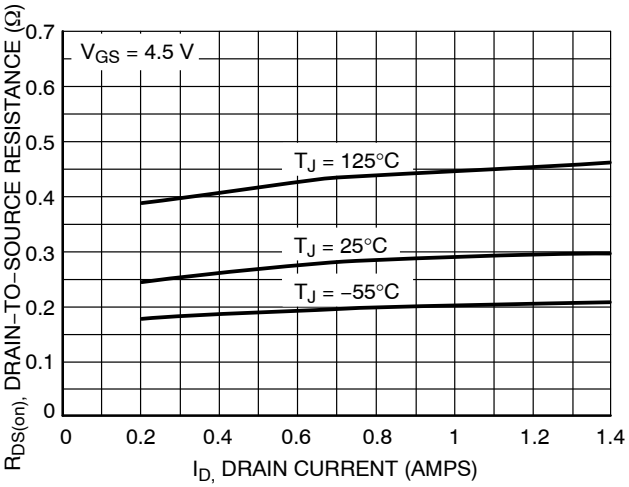


Figure 3. On−Resistance vs. Drain Current and Temperature

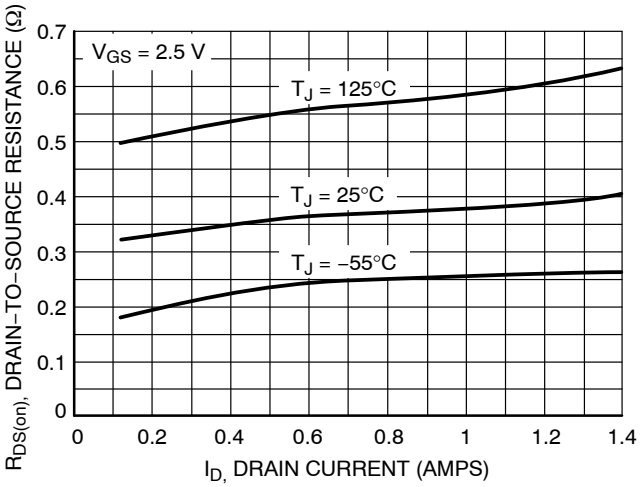


Figure 4. On−Resistance vs. Drain Current and Temperature

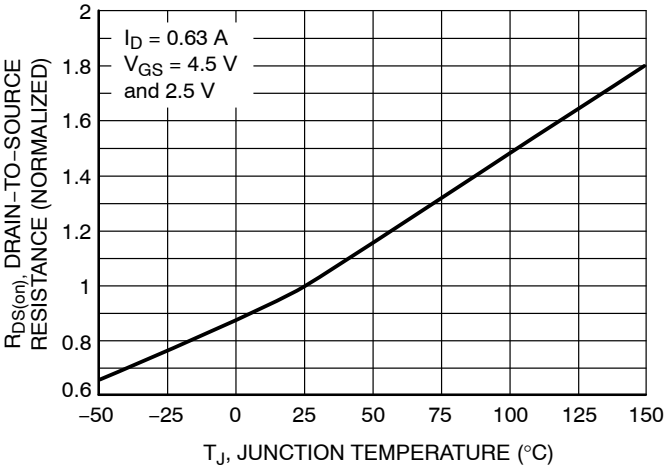


Figure 5. On−Resistance Variation with Temperature

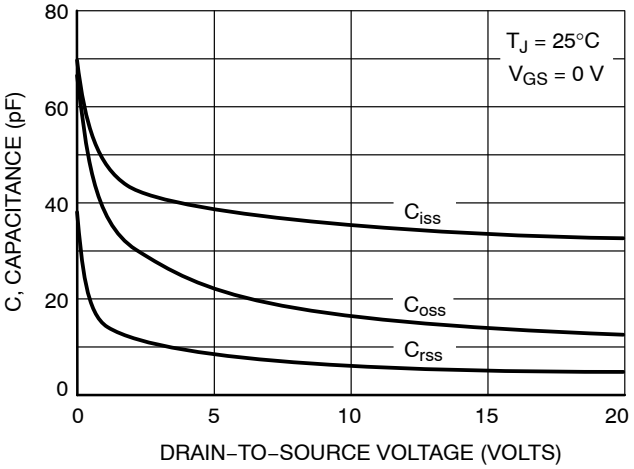


Figure 6. Capacitance Variation

TYPICAL N−CHANNEL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

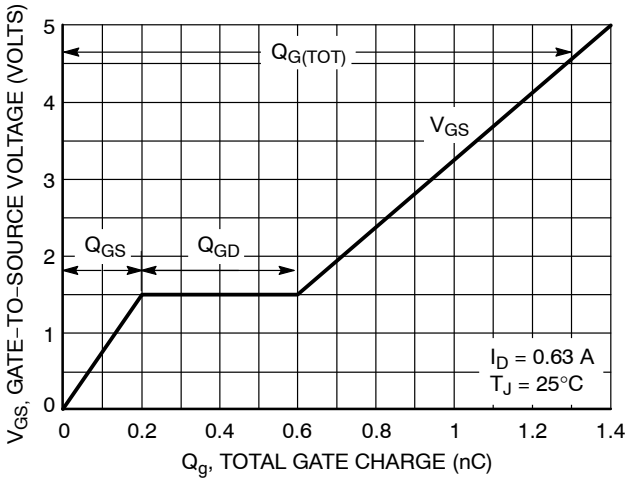


Figure 7. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

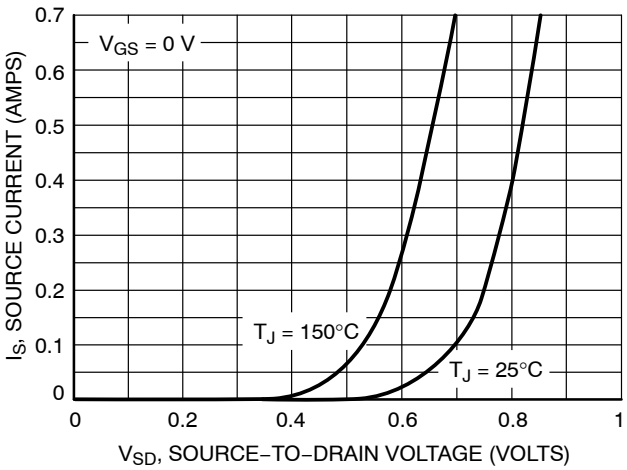


Figure 8. Diode Forward Voltage vs. Current

TYPICAL P−CHANNEL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

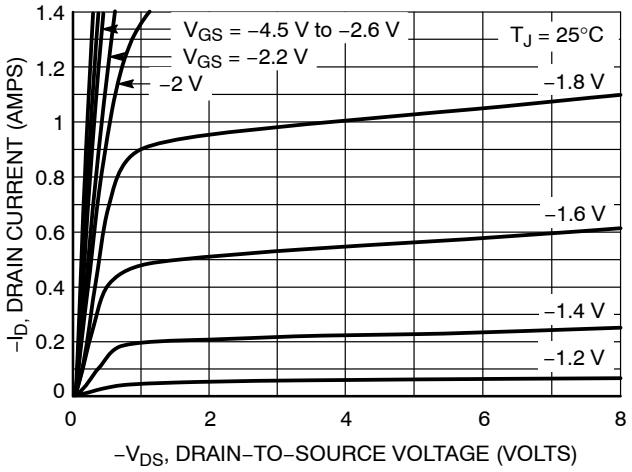


Figure 9. On−Region Characteristics

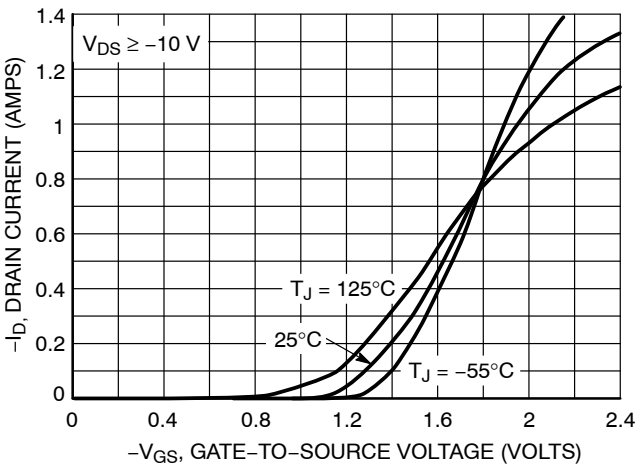


Figure 10. Transfer Characteristics

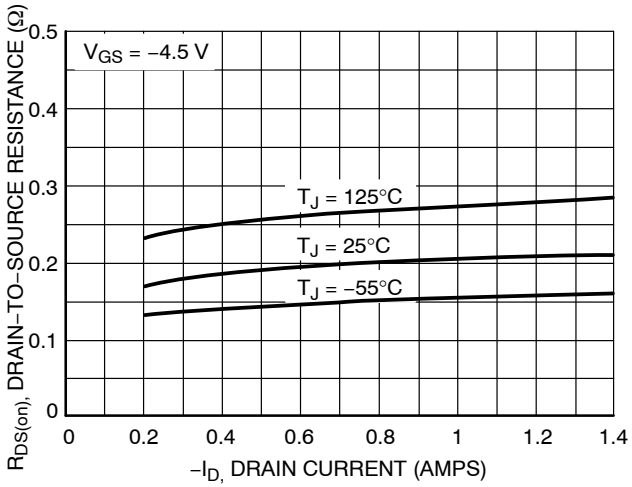


Figure 11. On−Resistance vs. Drain Current and Temperature

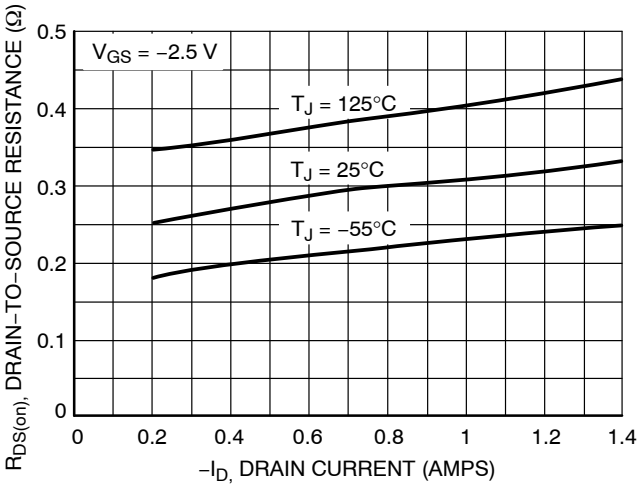


Figure 12. On−Resistance vs. Drain Current and Temperature

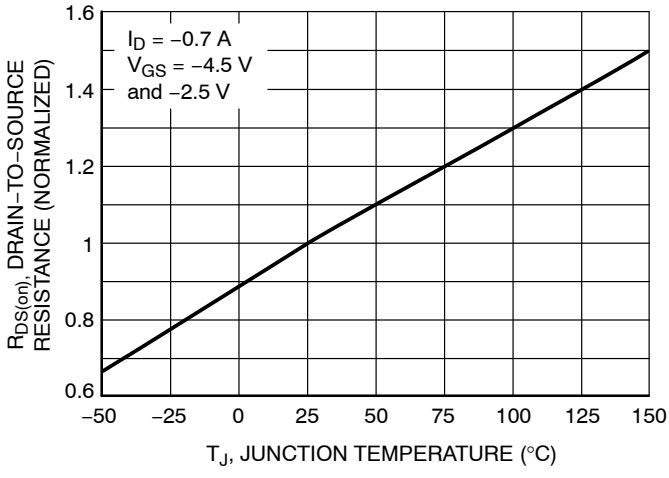


Figure 13. On−Resistance Variation with Temperature

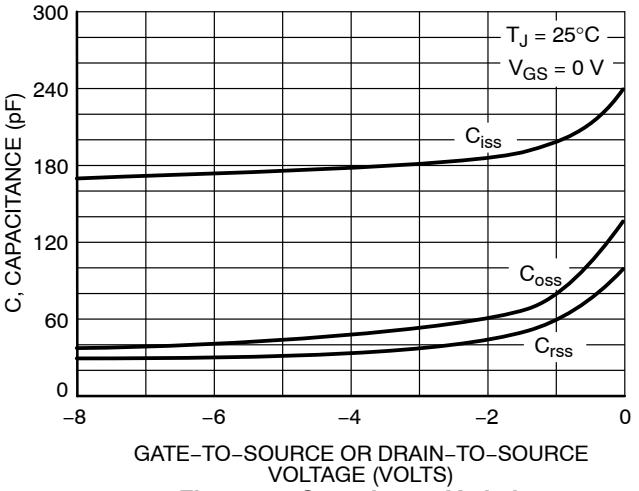


Figure 14. Capacitance Variation

TYPICAL P−CHANNEL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

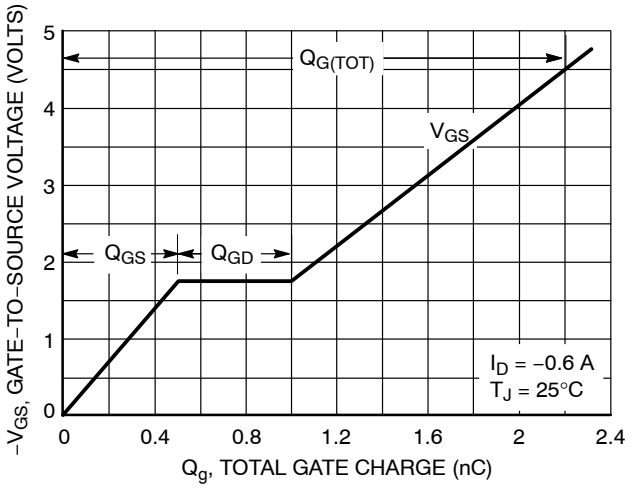


Figure 15. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

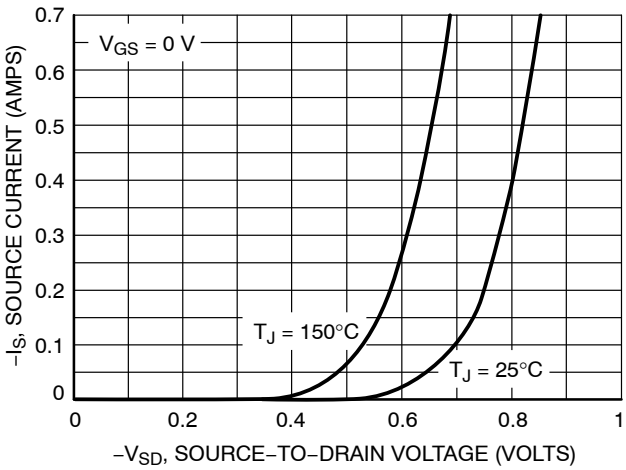


Figure 16. Diode Forward Voltage vs. Current

ORDERING INFORMATION

Device	Package	Shipping†
NTJD4105CT1	SOT−363	3000 / Tape & Reel
NTJD4105CT1G	SOT−363 (Pb−Free)	3000 / Tape & Reel
NTJD4105CT2	SOT−363	3000 / Tape & Reel
NTJD4105CT2G	SOT−363 (Pb−Free)	3000 / Tape & Reel
NTJD4105CT4	SOT−363	10,000 / Tape & Reel
NTJD4105CT4G	SOT−363 (Pb−Free)	10,000 / Tape & Reel

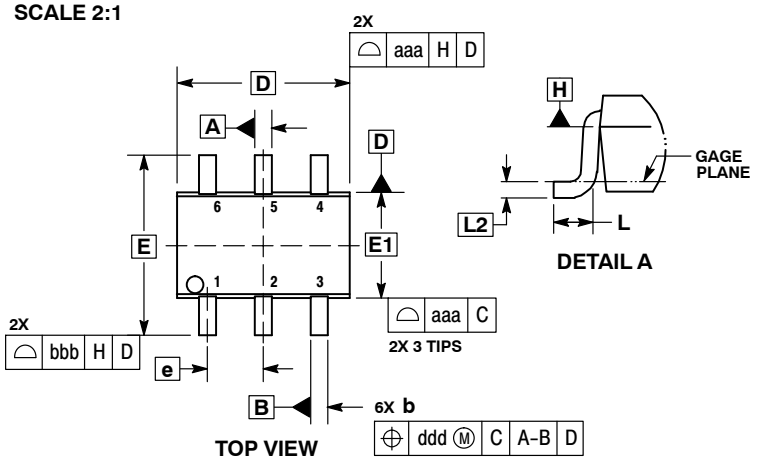
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

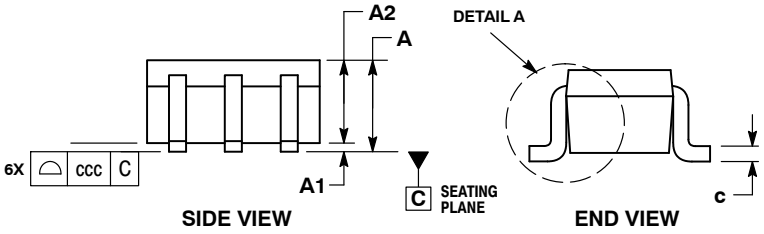
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

1
SCALE 2:1

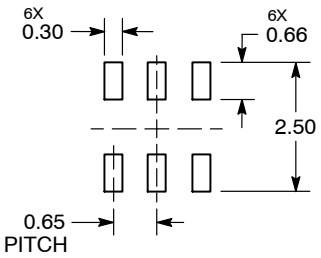




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	−−−	−−−	1.10	−−−	−−−	0.043
A1	0.00	−−−	0.10	0.000	−−−	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

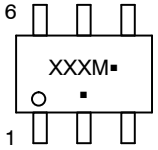
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42985B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SC−88/SC70−6/SOT−363**		**PAGE 1 OF 2**

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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