

NTR4101P, NTRV4101P

Trench Power MOSFET –20 V, Single P–Channel, SOT–23

Features

- Leading –20 V Trench for Low $R_{DS(on)}$
- –1.8 V Rated for Low Voltage Gate Drive
- SOT–23 Surface Mount for Small Footprint
- NTRV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Load/Power Management for Portables
- Load/Power Management for Computing
- Charging Circuits and Battery Protection

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	−20	V
Gate-to-Source Voltage			V_{GS}	±8.0	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	−2.4	A
		$T_A = 85^{\circ}\text{C}$		−1.7	
	$t \leq 10\text{ s}$	$T_A = 25^{\circ}\text{C}$		−3.2	
Power Dissipation (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	P_D	0.73	W
	$t \leq 10\text{ s}$			1.25	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	−1.8	A
		$T_A = 85^{\circ}\text{C}$		−1.3	
Power Dissipation (Note 2)		$T_A = 25^{\circ}\text{C}$	P_D	0.42	W
Pulsed Drain Current	$t_p = 10\text{ }\mu\text{s}$		I_{DM}	−18	A
ESD Capability (Note 3)	C = 100 pF, RS = 1500 Ω		ESD	225	V
Operating Junction and Storage Temperature			T_J , T_{STG}	−55 to 150	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	−2.4	A
Single Pulse Drain-to-Source Avalanche Energy ($V_{GS} = -8\text{ V}$, $I_L = -1.8\text{ Apk}$, $L = 10\text{ mH}$, $R_G = 25\text{ }\Omega$)			EAS	16	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

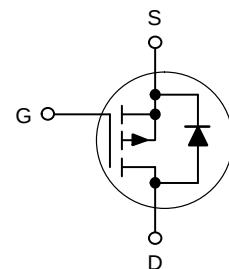


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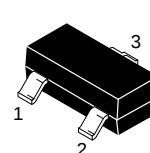
www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_D MAX
–20 V	70 m Ω @ –4.5 V	–3.2 A
	90 m Ω @ –2.5 V	
	112 m Ω @ –1.8 V	

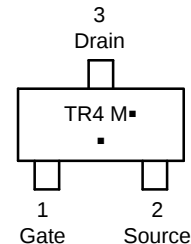
P–Channel MOSFET



MARKING DIAGRAM & PIN ASSIGNMENT



SOT–23
CASE 318
STYLE 21



TR4 = Device Code
M = Date Code
▪ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTR4101PT1G	SOT–23 (Pb–Free)	3000 / Tape & Reel
NTRV4101PT1G		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	170	°C/W
Junction-to-Ambient – $t < 10$ s (Note 1)	$R_{\theta JA}$	100	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	300	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size.
3. ESD Rating Information: HBM Class 0

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 4) ($V_{GS} = 0$ V, $I_D = -250$ μA)	$V_{(BR)DSS}$	-20			V
Zero Gate Voltage Drain Current (Note 4) ($V_{GS} = 0$ V, $V_{DS} = -16$ V)	I_{DSS}			-1.0	μA
Gate-to-Source Leakage Current ($V_{GS} = \pm 8.0$ V, $V_{DS} = 0$ V)	I_{GSS}			± 100	nA

ON CHARACTERISTICS

Gate Threshold Voltage (Note 4) ($V_{GS} = V_{DS}$, $I_D = -250$ μA)	$V_{GS(th)}$	-0.4	-0.72	-1.2	V
Drain-to-Source On-Resistance ($V_{GS} = -4.5$ V, $I_D = -1.6$ A) ($V_{GS} = -2.5$ V, $I_D = -1.3$ A) ($V_{GS} = -1.8$ V, $I_D = -0.9$ A)	$R_{DS(on)}$		70 90 112	85 120 210	m Ω
Forward Transconductance ($V_{DS} = -5.0$ V, $I_D = -2.3$ A)	g_{FS}		7.5		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	(V _{GS} = 0 V, f = 1 MHz, V _{DS} = -10 V)	C_{iss}		675		pF
Output Capacitance		C_{oss}		100		
Reverse Transfer Capacitance		C_{rss}		75		
Total Gate Charge	(V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -1.6 A)	$Q_{G(tot)}$		7.5	8.5	nC
Gate-to-Source Gate Charge	(V _{DS} = -10 V, I _D = -1.6 A)	Q_{GS}		1.2		nC
Gate-to-Drain "Miller" Charge	(V _{DS} = -10 V, I _D = -1.6 A)	Q_{GD}		2.2		nC
Gate Resistance		R_G		6.5		Ω

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	(V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -1.6 A, R _G = 6.0 Ω)	$t_{d(on)}$		7.5		ns
Rise Time		t_r		12.6		
Turn-Off Delay Time		$t_{d(off)}$		30.2		
Fall Time		t_f		21.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	(V _{GS} = 0 V, I _S = -2.4 A)	V_{SD}		-0.82	-1.2	V
Reverse Recovery Time	(V _{GS} = 0 V, dI _{SD} /dt = 100 A/ μs , I _S = -1.6 A)	t_{rr}		12.8	15	ns
Charge Time		t_a		9.9		ns
Discharge Time		t_b		3.0		ns
Reverse Recovery Charge		Q_{rr}		1008		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2\%$.
5. Switching characteristics are independent of operating junction temperature.

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

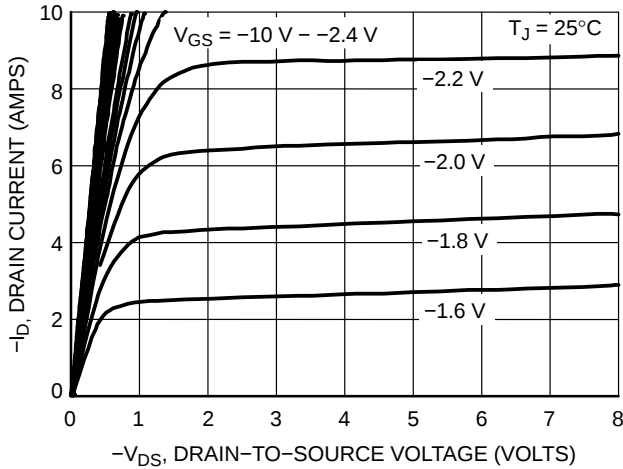


Figure 1. On-Region Characteristics

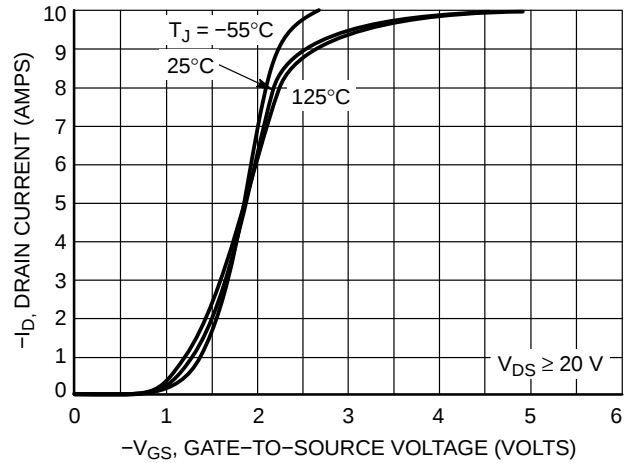


Figure 2. Transfer Characteristics

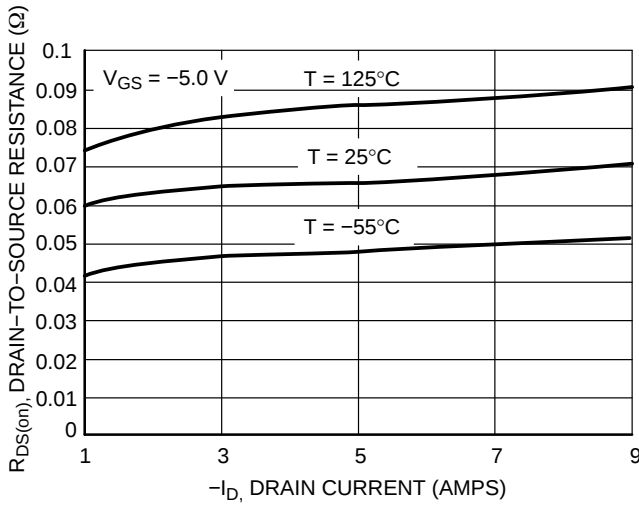


Figure 3. On-Resistance vs. Drain Current and Temperature

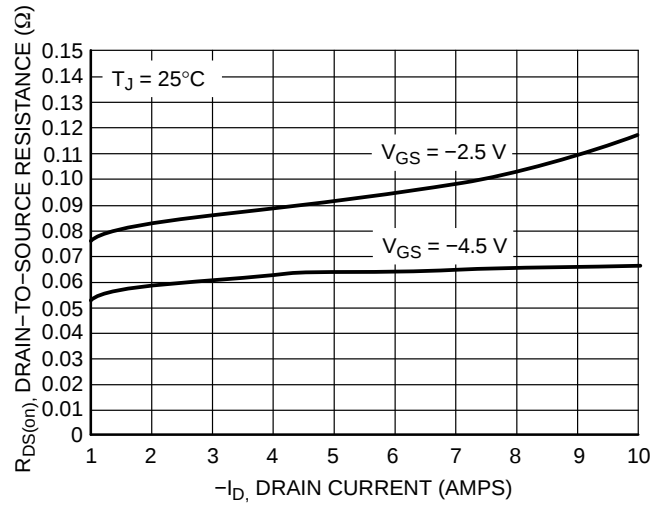


Figure 4. On-Resistance vs. Drain Current and Temperature

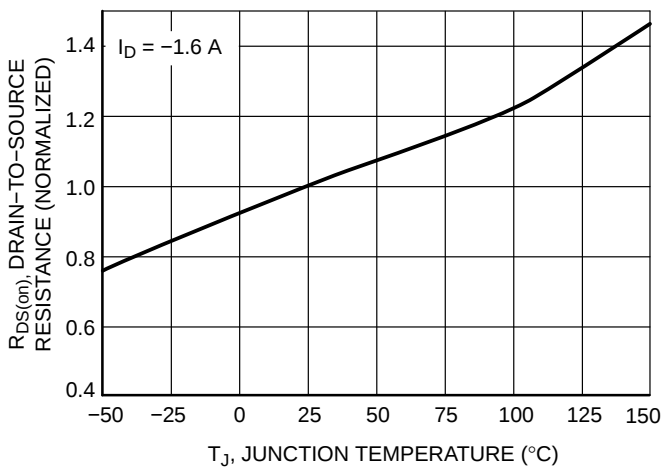


Figure 5. On-Resistance Variation with Temperature

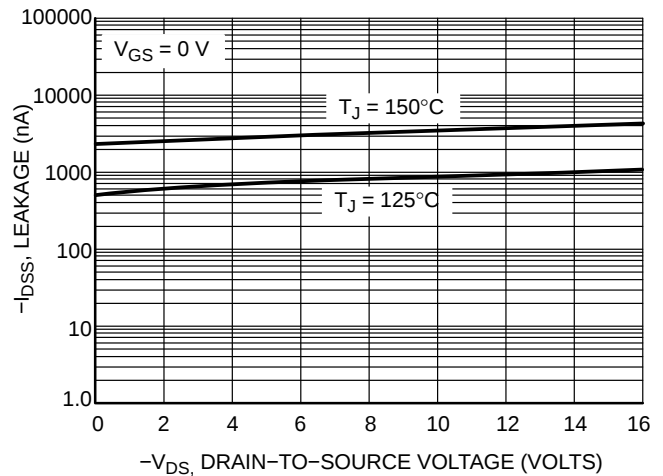


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

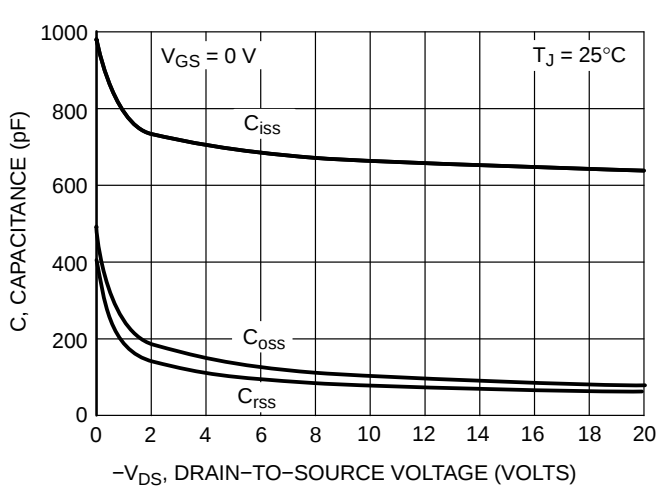


Figure 7. Capacitance Variation

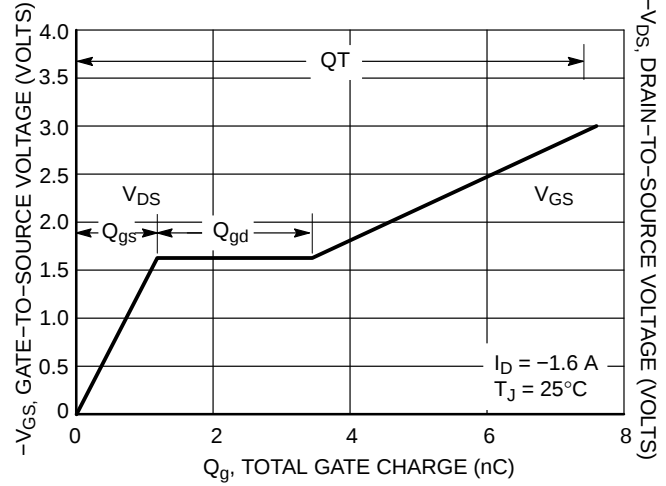


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Gate Charge

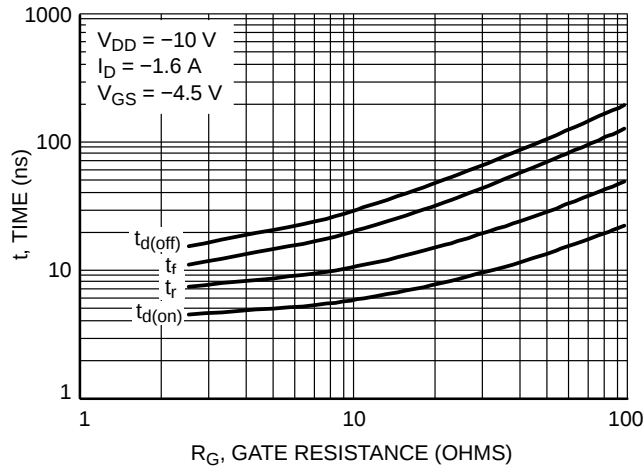


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

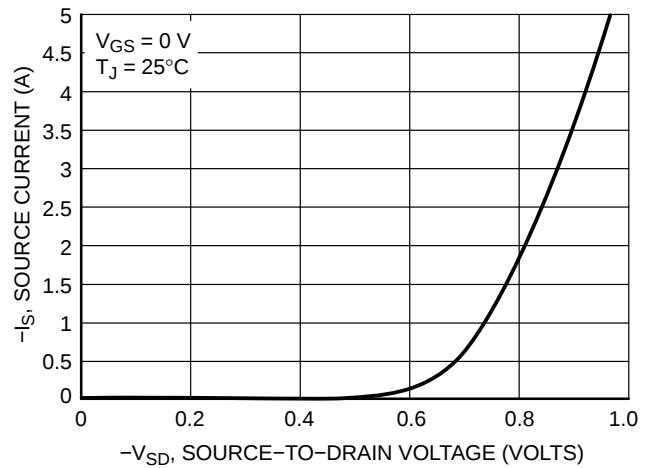


Figure 10. Diode Forward Voltage vs. Current

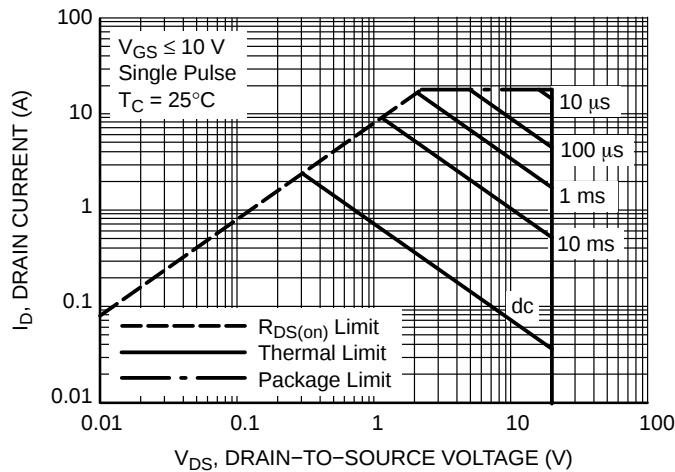
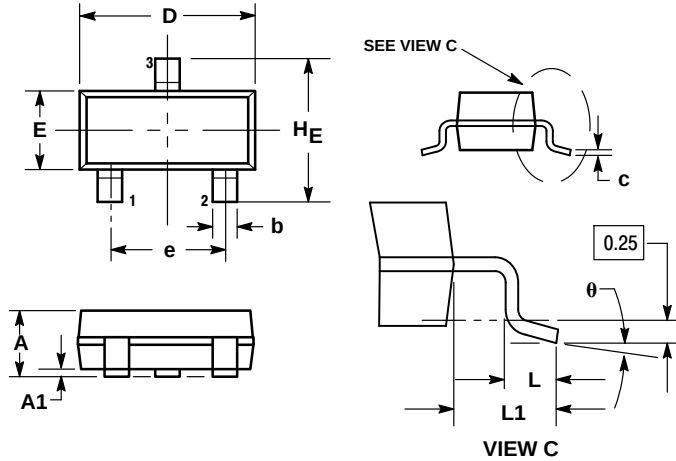


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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PACKAGE DIMENSIONS

SOT-23 (TO-236) CASE 318-08 ISSUE AP



NOTES:

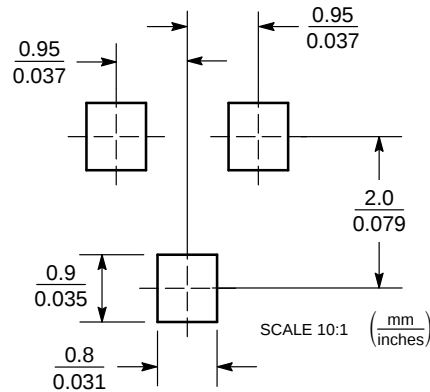
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH,

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

STYLE 12:

1. CATHODE
2. CATHODE
3. ANODE

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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