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FAIRCHILD
SEMICONDUCTOR®

November 2013

FDP33N25
N-Channel UniFET™ MOSFET
250 V, 33 A, 94 mΩ

Features

- $R_{DS(on)}$ = 94 mΩ (Max.) @ V_{GS} = 10 V, I_D = 16.5 A
- Low Gate Charge (Typ. 36.8 nC)
- Low C_{rss} (Typ. 39 pF)
- 100% Avalanche Tested

Applications

- PDP TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

TO-220
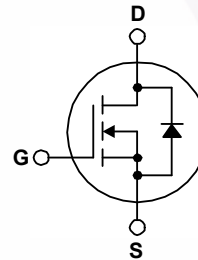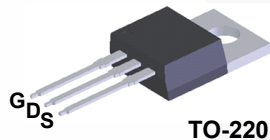
Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			FDP33N25	Unit
V_{DSS}	Drain-Source Voltage			250	V
I_D	Drain Current	- Continuous (T_C = 25°C)		33	A
		- Continuous (T_C = 100°C)		20.4	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	132	A
V_{GSS}	Gate-Source voltage			± 30	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	918	mJ
I_{AR}	Avalanche Current		(Note 1)	33	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	23.5	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)		235	W
		- Derate Above 25°C		1.89	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300	°C

Thermal Characteristics

Symbol	Parameter	FDP33N25	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.53	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP33N25	FDP33N25	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA, T_J = 25°C	250	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.25	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 250 V, V_{GS} = 0 V V_{DS} = 200 V, T_C = 125°C	-- --	-- --	1 10	µA µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 16.5 A	--	0.077	0.094	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 16.5 A	--	26.6	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1640	2135	pF
C_{oss}	Output Capacitance		--	330	430	pF
C_{rss}	Reverse Transfer Capacitance		--	39	59	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 125 V, I_D = 33 A, V_{GS} = 10 V, R_G = 25 Ω	--	35	80	ns
t_r	Turn-On Rise Time		--	230	470	ns
$t_{d(off)}$	Turn-Off Delay Time		--	75	160	ns
t_f	Turn-Off Fall Time	(Note 4)	--	120	250	ns
Q_g	Total Gate Charge	V_{DS} = 200 V, I_D = 33 A, V_{GS} = 10 V	--	36.8	48	nC
Q_{gs}	Gate-Source Charge		--	10	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4)	--	17	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	33	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	132	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 33 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 33 A, dI_F/dt =100 A/µs	--	220	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.71	--	µC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 1.35 mH, I_{AS} = 33 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 33 A, di/dt ≤ 200 A/µs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics
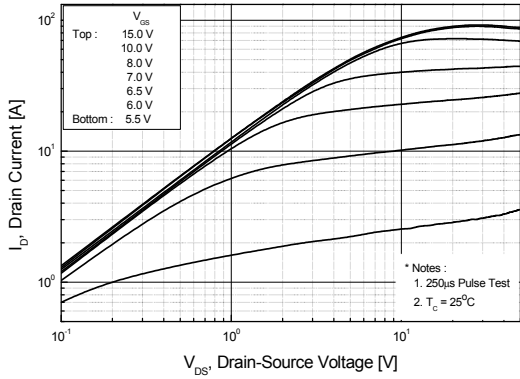
Figure 1. On-Region Characteristics

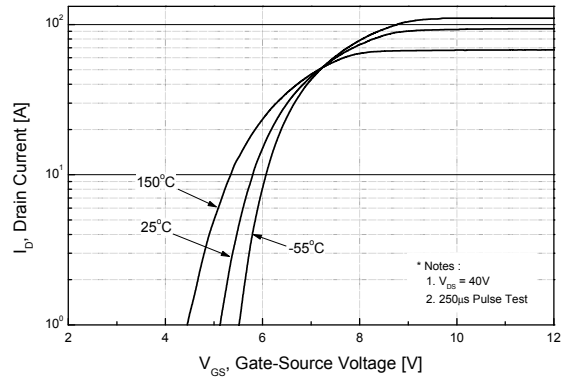

Figure 2. Transfer Characteristics

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage
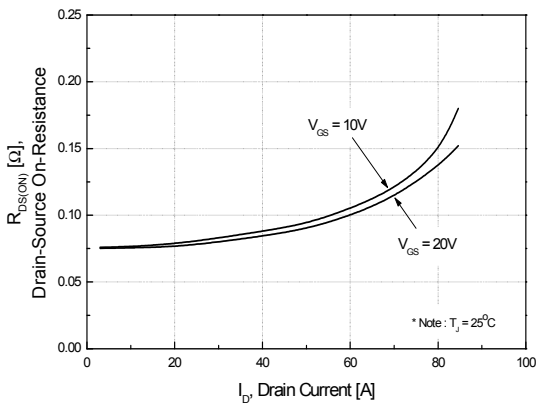

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue
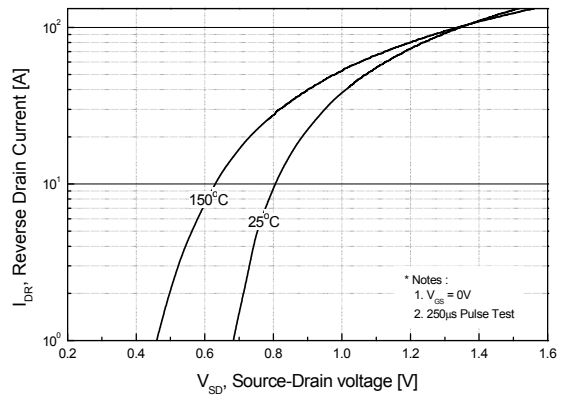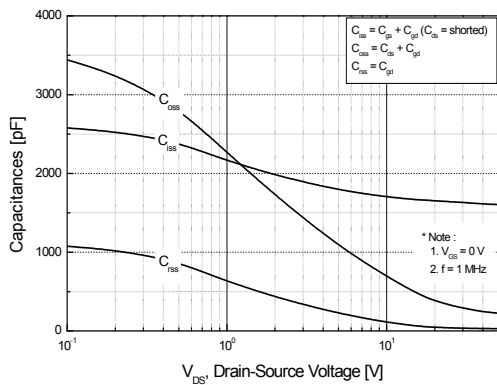

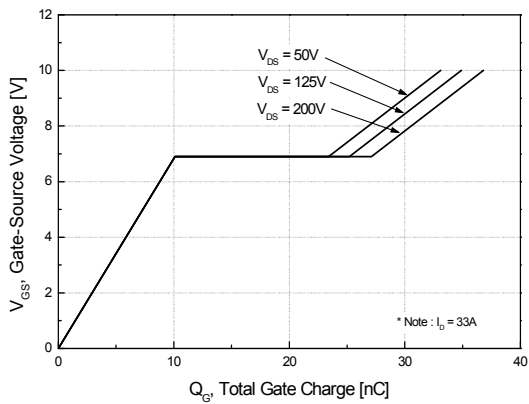### Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

Typical Performance Characteristics (Continued)
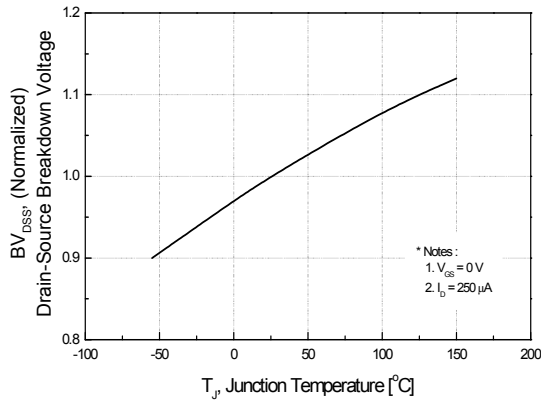
Figure 7. Breakdown Voltage Variation vs. Temperature

* Notes :
1. $V_{GS} = 0$ V
2. $I_D = 250 \mu A$

Figure 8. On-Resistance Variation vs. Temperature

* Notes :
1. $V_{GS} = 10$ V
2. $I_D = 16.5$ A
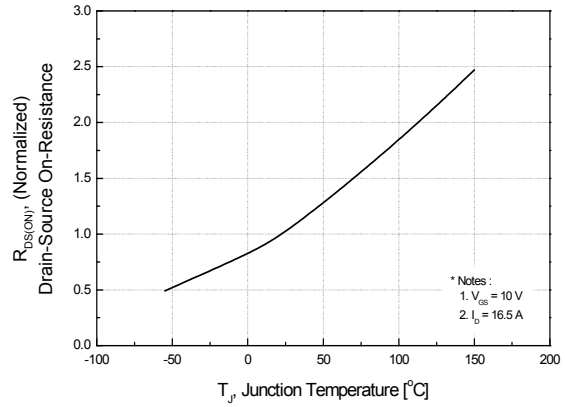
Figure 9. Maximum Safe Operating Area

Operation in This Area is Limited by $R_{DS(on)}$

10 μs
100 μs
1 ms
10 ms
100 ms
DC

* Notes :
1. $T_C = 25$ °C
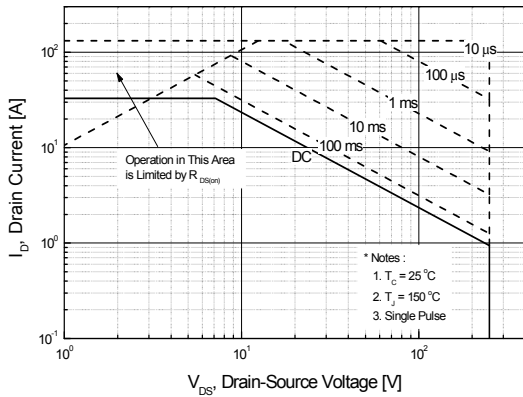2. $T_J = 150$ °C
3. Single Pulse

Figure 10. Maximum Drain Current vs. Case Temperature
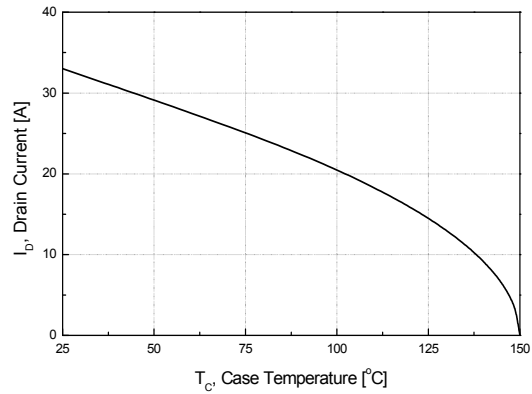
Figure 11. Transient Thermal Response Curve

D=0.5
0.2
0.1
0.05
0.02
0.01
single pulse

* Notes :
1. $Z_{\theta JC}(t) = 0.53$ °C/W Max.
2. Duty Factor, $D = t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$
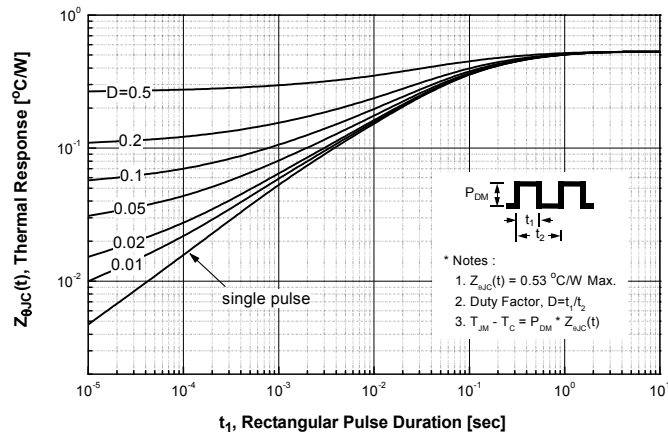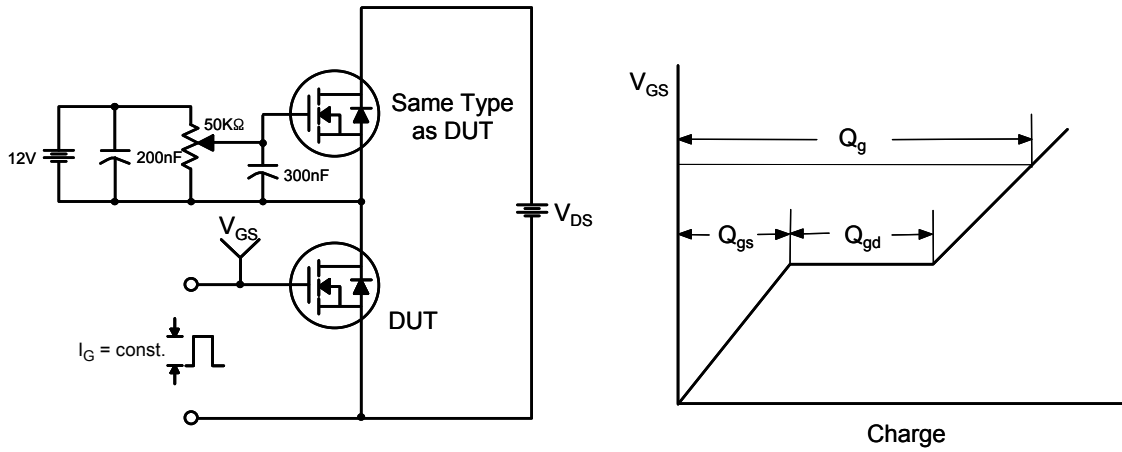
Figure 12. Gate Charge Test Circuit & Waveform
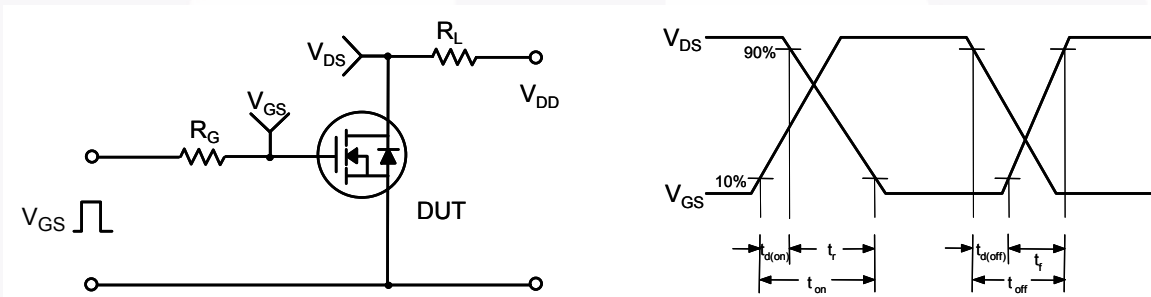
Figure 13. Resistive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \; \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$
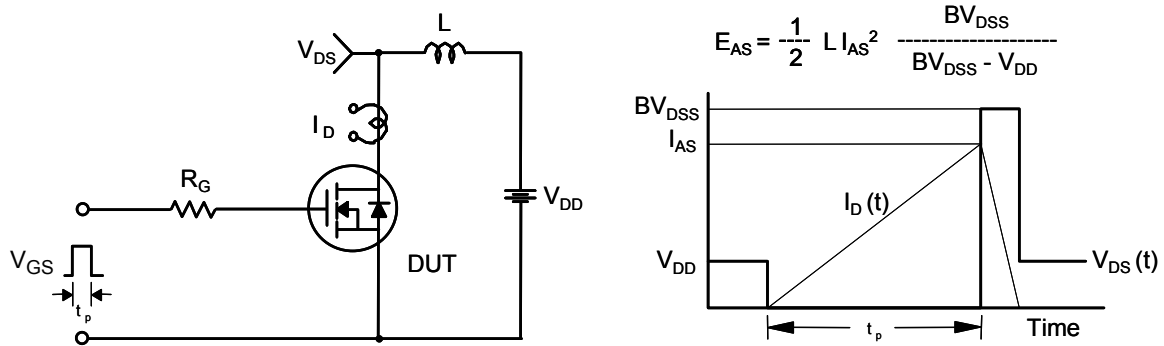
Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

Ø4.09
3.50

⊕ | 0.36 Ⓜ | B | AⓂ

A 10.67
9.65

3.43
2.54

16.51
14.22

△9.40
8.38

1 2 3

6.35 MAX

14.73
12.70

(1.91)

1.78
1.14

1.02
0.38

2.54

5.08

⊕ | 0.36 Ⓜ | B | AⓂ

B

4.83
3.56

"A1"

7°
3°

6.86
5.84

5°
3°

5°
3°

0.61
△0.33

8.89
6.86

△13.40
12.19

3 2 1

2.92
2.03

5°
3°   5°
3°

NOTES: UNLESS OTHERWISE SPECIFIED
A) REFERENCE JEDEC, TO-220, ISSUE K,
VARIATION AB, DATED APRIL, 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER
ANSI Y14,5 - 1973
D) LOCATION OF THE PIN HOLE MAY VARY
(LOWER LEFT CORNER, LOWER CENTER
AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE,
F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE   = 1,14 - 1,40
G) DRAWING FILE NAME: TO220B03REV6

Figure 16. TO-220, Molded, 3-Lead, Jedec Variation AB

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I66

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