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FDC855N

Single N-Channel, Logic Level, PowerTrench® MOSFET 30V, 6.1A, 27mΩ

Features

- Max $r_{DS(on)}$ = 27mΩ at $V_{GS} = 10V$, $I_D = 6.1A$
- Max $r_{DS(on)}$ = 36mΩ at $V_{GS} = 4.5V$, $I_D = 5.3A$
- SuperSOT™ -6 package: small footprint (72% smaller than standard SO-8; low profile (1mm thick).
- RoHS Compliant

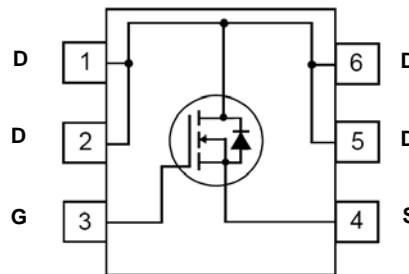
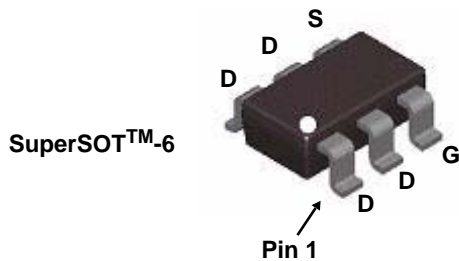


General Description

This N-Channel Logic Level MOSFET is an efficient solution for low voltage and battery powered applications. Utilizing Fairchild Semiconductor's advanced PowerTrench® process, this device possesses minimized on-state resistance to optimize the power consumption. They are ideal for applications where in-line power loss is critical.

Application

- Power Management in Notebook, Hard Disk Drive



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	6.1	A
	-Pulsed	20	
P_D	Power Dissipation (Steady State) (Note 1a)	1.6	W
	Power Dissipation (Steady State) (Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	30	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.855	FDC855N	SuperSOT-6	7"	8 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		24		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{V}, V_{DS} = 24\text{V}$, $T_C = 125^\circ\text{C}$			1 250	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 6.1\text{A}$		20.7	27.0	m Ω
		$V_{GS} = 4.5\text{V}, I_D = 5.3\text{A}$		28.2	36.0	
		$V_{GS} = 10\text{V}, I_D = 6.1\text{A}, T_J = 125^\circ\text{C}$		30.1	39.3	
g_{FS}	Forward Transconductance	$V_{DD} = 10\text{V}, I_D = 6.1\text{A}$		20		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}$, $f = 1\text{MHz}$		493	655	pF
C_{oss}	Output Capacitance			108	145	pF
C_{rss}	Reverse Transfer Capacitance			62	95	pF
R_g	Gate Resistance	$f = 1\text{MHz}$		1.0		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{V}, I_D = 6.1\text{A}$, $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		6	12	ns
t_r	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			14	23	ns
t_f	Fall Time			2	10	ns
Q_g	Total Gate Charge at 10V		$V_{GS} = 0\text{V to } 10\text{V}$	$V_{DD} = 15\text{V}$, $I_D = 6.1\text{A}$	9.2	13
Q_g	Total Gate Charge at 5V	$V_{GS} = 0\text{V to } 5\text{V}$	4.9		7.0	nC
Q_{gs}	Gate to Source Charge		1.7			nC
Q_{gd}	Gate to Drain "Miller" Charge		3.1			nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 1.3\text{A}$ (Note 2)		0.80	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 6.1\text{A}, di/dt = 100\text{A}/\mu\text{s}$		17	31	ns
Q_{rr}	Reverse Recovery Charge			6	12	nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $78^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $156^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2: Pulse Test: Pulse Width < $300\mu\text{s}$, Duty Cycle < 2.0%.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

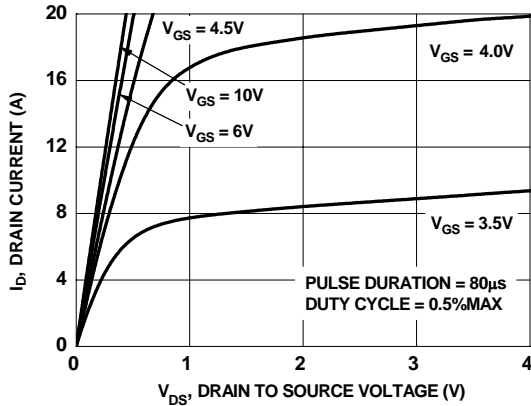


Figure 1. On-Region Characteristics

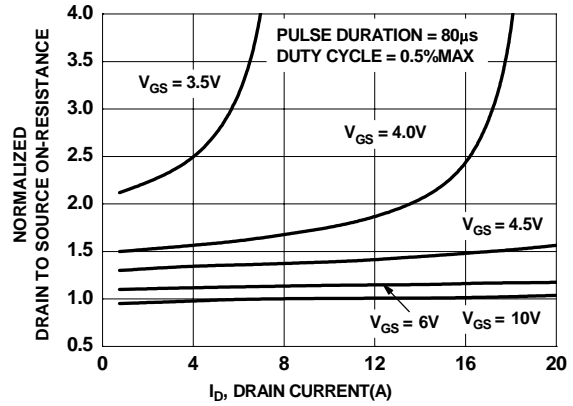


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

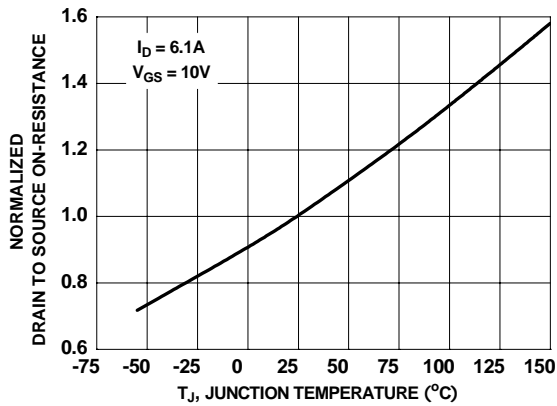


Figure 3. Normalized On-Resistance vs Junction Temperature

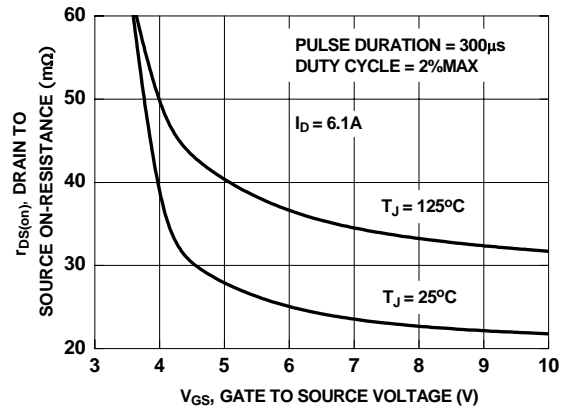


Figure 4. On-Resistance vs Gate to Source Voltage

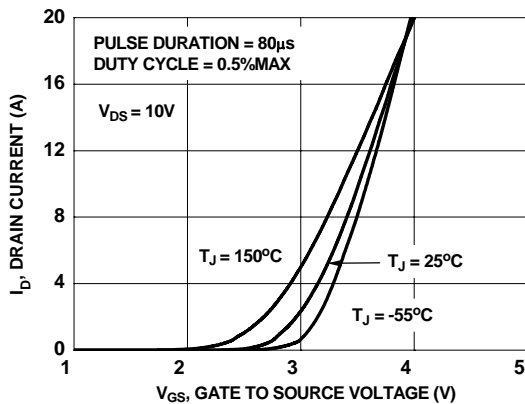


Figure 5. Transfer Characteristics

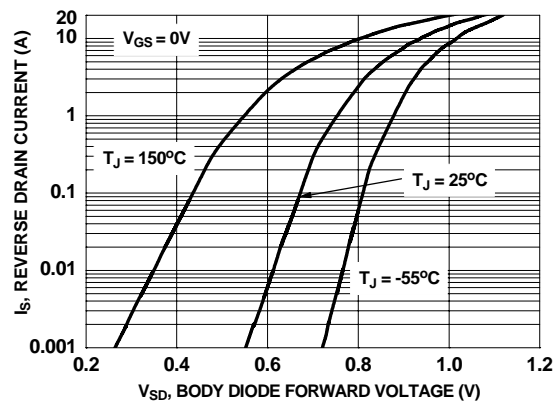


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

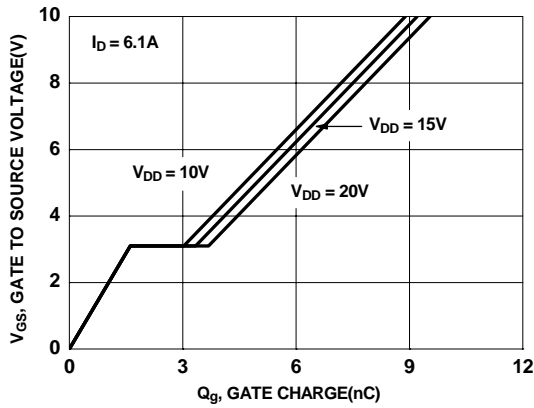


Figure 7. Gate Charge Characteristics

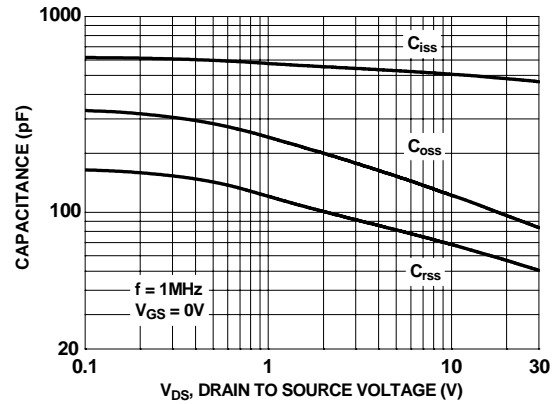


Figure 8. Capacitance vs Drain to Source Voltage

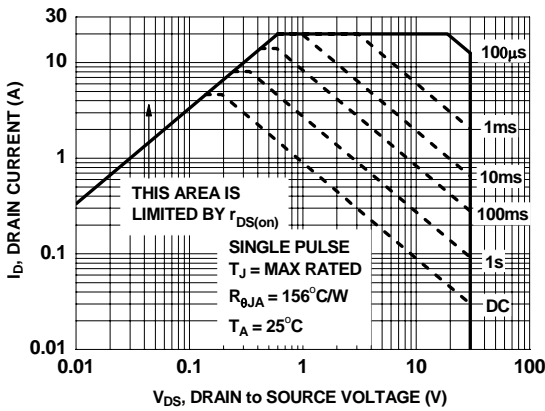


Figure 9. Forward Bias Safe Operating Area

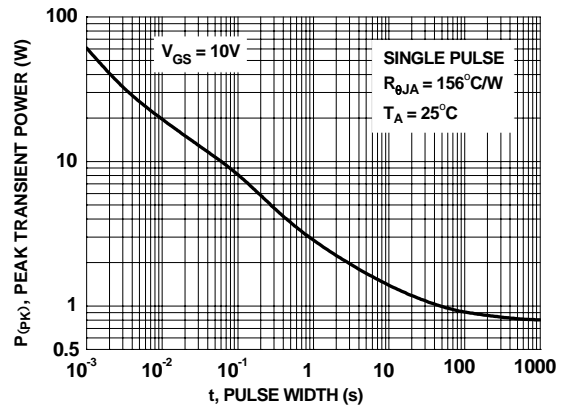


Figure 10. Single Pulse Maximum Power Dissipation

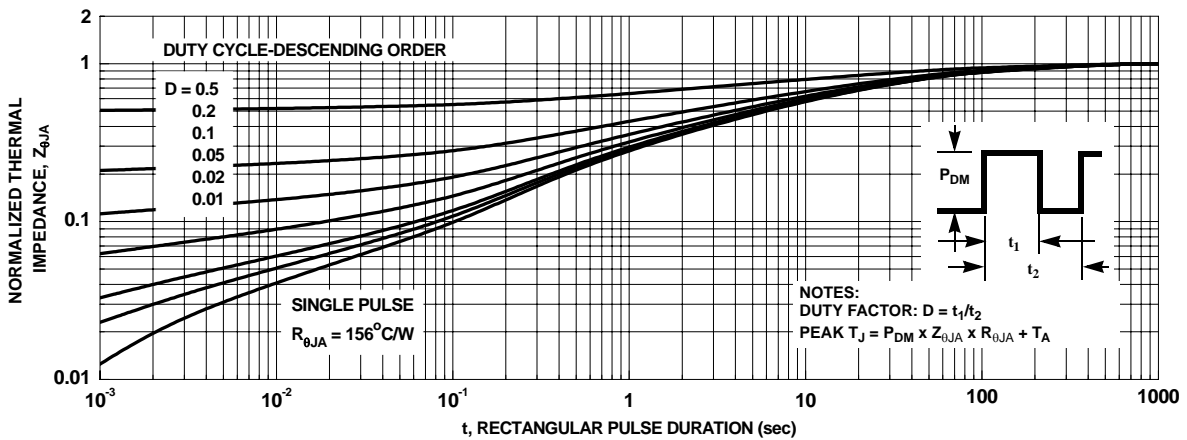
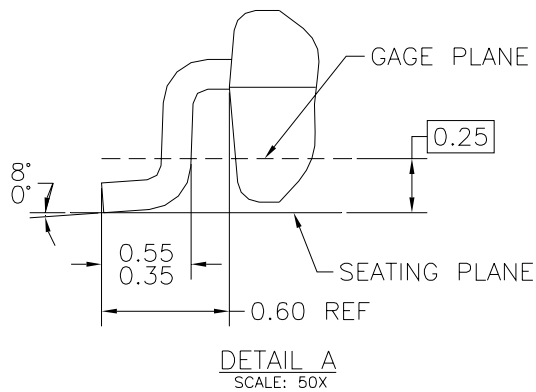
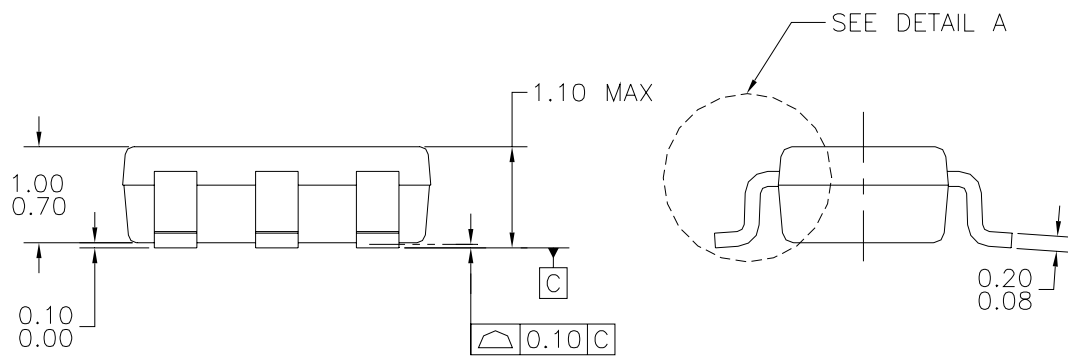
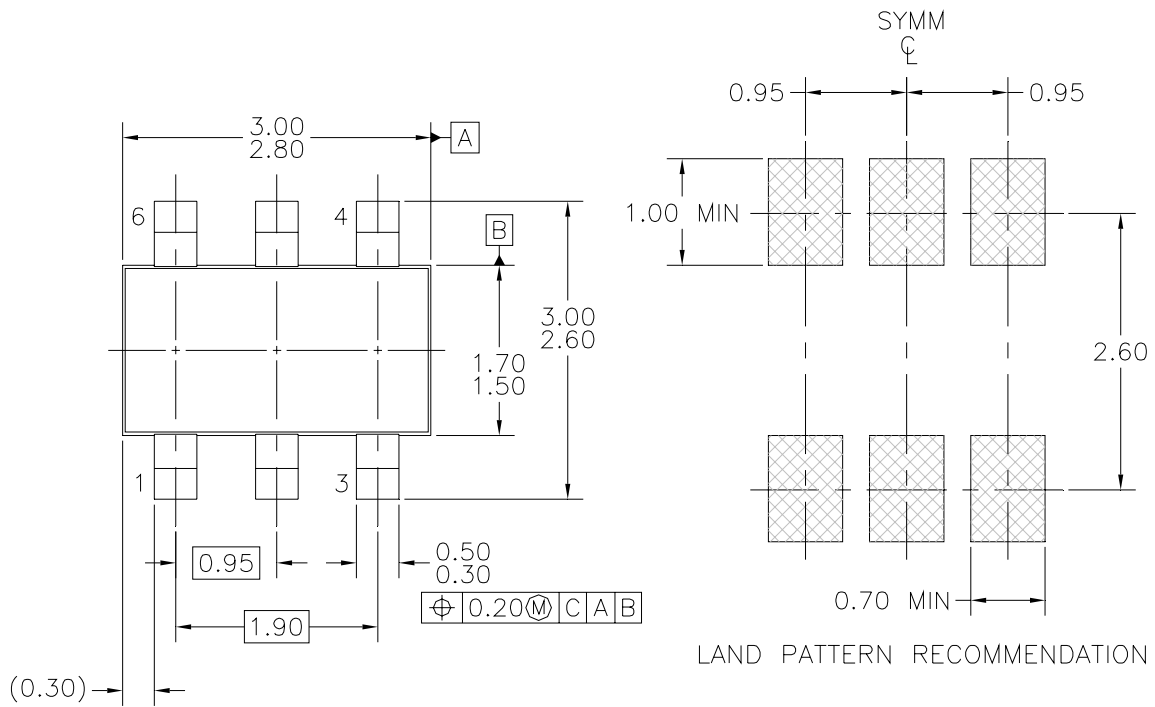


Figure 11. Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED



- A) THIS PACKAGE CONFORMS TO JEDEC MO-193. VAR. AA, ISSUE C, DATED JANUARY 2000.
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