

# Octal D-Type Flip-Flops with Clear

## MM74HC273

### General Description

The MM74HC273 edge triggered flip-flops utilize advanced silicon-gate CMOS technology to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 8 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the LOW-to-HIGH transition of the CLOCK input. The CLEAR input when LOW, sets all outputs to a low state.

Each output can drive 10 low power Schottky TTL equivalent loads. The MM74HC273 is functionally as well as pin compatible to the 74LS273. All inputs are protected from damage due to static discharge by diodes to  $V_{CC}$  and ground.

### Features

- Typical Propagation Delay: 18 ns
- Wide Operating Voltage Range
- Low Input Current: 1  $\mu$ A Maximum
- Low Quiescent Current: 160  $\mu$ A (74 Series)
- Output Drive: 10 LS-TTL Loads
- This is a Pb-Free Device

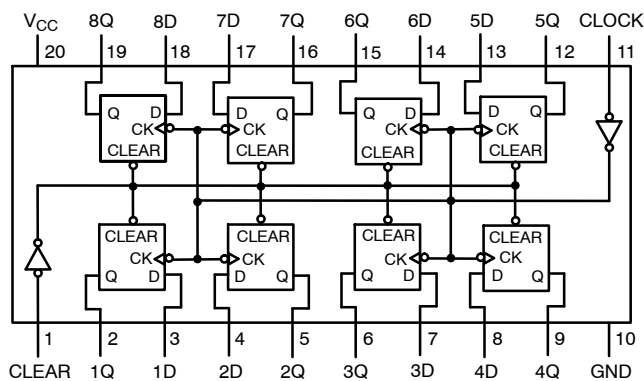
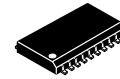


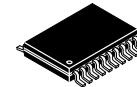
Figure 1. Connection Diagram



SOIC-20 WB  
CASE 751D-05

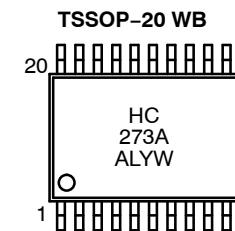
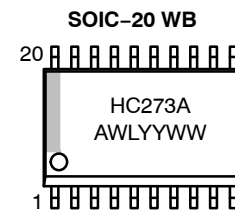


SOIC-20, 300 mils  
CASE 751BJ-01



TSSOP-20 WB  
CASE 948E

### MARKING DIAGRAMS



HC273A = Specific Device Code  
A = Assembly Location  
WL, L = Wafer Lot Number  
Y = Year  
WW, YW = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

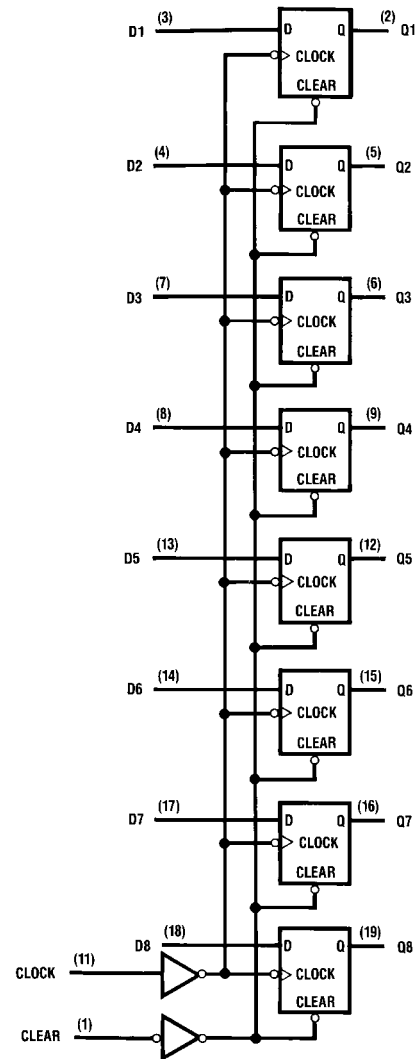
# MM74HC273

**TRUTH TABLE** (Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q <sub>0</sub>

**NOTES:**

- H = HIGH Level (Steady State)
- L = LOW Level (Steady State)
- X = Don't Care
- ↑ = Transition from LOW-to-HIGH level
- Q<sub>0</sub> = The level of Q before the indicated steady state input conditions were established.



**Figure 2. Logic Diagram**

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Symbol	Rating	Value	Unit	
V <sub>CC</sub>	Supply Voltage	-0.5 to +7.0 V	V	
V <sub>IN</sub>	DC Input Voltage	-0.5 to V <sub>CC</sub> +0.5 V	V	
V <sub>OUT</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> +0.5 V	V	
I <sub>IK</sub> , I <sub>OK</sub>	Clamp Diode Current	±20	mA	
I <sub>OUT</sub>	DC Output Current, per pin	±25	mA	
I <sub>CC</sub>	DC V <sub>CC</sub> or GND Current, per pin	±50	mA	
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C	
P <sub>D</sub>	Power Dissipation	Note 2	600	mW
		S. O. Package only	500	mW
T <sub>L</sub>	Lead Temperature (Soldering 10 seconds)	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating – plastic "N" package: 12 mW/°C from 65°C to 85°C.

# MM74HC273

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	Supply Voltage	2	6	V	
$V_{IN}, V_{OUT}$	DC Input or Output Voltage	0	$V_{CC}$	V	
$T_A$	Operating Temperature Range	-55	125	°C	
$t_r, t_f$	Input Rise or Fall Times	$V_{CC} = 2.0\text{ V}$	-	1000	ns
		$V_{CC} = 4.5\text{ V}$	-	500	ns
		$V_{CC} = 6.0\text{ V}$	-	400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Note 3)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ\text{C}$		$T_A = -40$ to $85^\circ\text{C}$	$T_A = -55$ to $125^\circ\text{C}$	Unit
				Typ	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0 V		1.5	1.5	1.5	V
			4.5 V		3.15	3.15	3.15	V
			6.0 V		4.2	4.2	4.2	V
$V_{IL}$	Maximum LOW Level Input Voltage		2.0 V		0.5	0.5	0.5	V
			4.5 V		1.35	1.35	1.35	V
			6.0 V		1.8	1.8	1.8	V
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20\ \mu\text{A}$	2.0 V	2.0	1.9	1.9	1.9	V
			4.5 V	4.5	4.4	4.4	4.4	V
			6.0 V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0\text{ mA}$ $ I_{OUT}  \leq 5.2\text{ mA}$	4.5 V	4.2	3.98	3.84	3.7	V
			6.0 V	5.7	5.48	5.34	5.2	V
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20\ \mu\text{A}$	2.0 V	0	0.1	0.1	0.1	V
			4.5 V	0	0.1	0.1	0.1	V
			6.0 V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0\text{ mA}$ $ I_{OUT}  \leq 5.2\text{ mA}$	4.5 V	0.2	0.26	0.33	0.4	V
			6.0 V	0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0 V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\ \mu\text{A}$	6.0 V		8	80	160	$\mu\text{A}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. For a power supply of  $5\text{ V} \pm 10\%$  the worst case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5\text{ V}$  and  $4.5\text{ V}$  respectively. (The  $V_{IH}$  value at 5.5 V is 3.85 V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

# MM74HC273

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 15\text{ pF}$ ,  $t_r = t_f = 6\text{ ns}$ )

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
$f_{MAX}$	Maximum Operating Frequency		50	30	MHz
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, Clock to Output		18	27	ns
$t_{PHL}$	Maximum Propagation Delay, Clear to Output		18	27	ns
$t_{REM}$	Minimum Removal Time, Clear to Clock		10	20	ns
$t_s$	Minimum Setup Time, Data to Clock		10	20	ns
$t_H$	Minimum Hold Time, Clock to Data		-2	0	ns
$t_W$	Minimum Pulse Width, Clock to Clear		10	16	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS

( $C_L = 50\text{ pF}$ ,  $t_r = t_f = 6\text{ ns}$ , unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ\text{C}$		$T_A = -40\text{ to }85^\circ\text{C}$	$T_A = -55\text{ to }125^\circ\text{C}$	Unit
				Typ	Guaranteed Limits			
$f_{MAX}$	Maximum Operating Frequency		2.0 V	16	5	4	3	MHz
			4.5 V	74	27	21	18	MHz
			6.0 V	78	31	24	20	MHz
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, Clock to Output		2.0 V	38	135	170	205	ns
			4.5 V	14	27	34	41	ns
			6.0 V	12	23	29	35	ns
$t_{PHL}$	Maximum Propagation Delay, Clear to Output		2.0 V	42	135	170	205	ns
			4.5 V	19	27	34	41	ns
			6.0 V	18	23	29	35	ns
$t_{REM}$	Minimum Removal Time, Clear to Clock		2.0 V	0	25	32	37	ns
			4.5 V	0	5	6	7	ns
			6.0 V	0	4	5	6	ns
$t_s$	Minimum Setup Time, Data to Clock		2.0 V	26	100	125	150	ns
			4.5 V	7	20	25	30	ns
			6.0 V	5	17	21	25	ns
$t_H$	Minimum Hold Time, Clock to Clock		2.0 V	-15	0	0	0	ns
			4.5 V	-6	0	0	0	ns
			6.0 V	-4	0	0	0	ns
$t_W$	Minimum Pulse Width, Clock or Clear		2.0 V	34	80	100	120	ns
			4.5 V	11	16	20	24	ns
			6.0 V	10	14	18	20	ns
$t_r$ , $t_f$	Maximum Input Rise and Fall Time, Clock		2.0 V	-	1000	1000	1000	ns
			4.5 V	-	500	500	500	ns
			6.0 V	-	400	400	400	ns
$t_{THL}$ , $t_{TLH}$	Maximum Output Rise and Fall Time		2.0 V	28	75	95	110	ns
			4.5 V	11	15	19	22	ns
			6.0 V	9	13	16	19	ns

# MM74HC273

## AC ELECTRICAL CHARACTERISTICS (continued)

( $C_L = 50$  pF,  $t_r = t_f = 6$  ns, unless otherwise specified)

Symbol	Parameter	Conditions	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40 to 85°C	T <sub>A</sub> = -55 to 125°C	Unit
				Typ	Guaranteed Limits			
C <sub>PD</sub>	Power Dissipation Capacitance (Note 4)	(per flip-flop)		45				pF
C <sub>IN</sub>	Maximum Input Capacitance			7	10	10	10	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. C<sub>PD</sub> determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

## ORDERING INFORMATION

Device	Package	Shipping†
MM74HC273WM	SOIC-20 WB (Pb-Free and Halide Free)	38 Units / Tube
MM74HC273WMX	SOIC-20, 300 mils (Pb-Free and Halide Free)	1000 / Tape & Reel
MM74HC273MTC	TSSOP-20 WB (Pb-Free)	75 Units / Tube
MM74HC273MTCX		2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MECHANICAL CASE OUTLINE

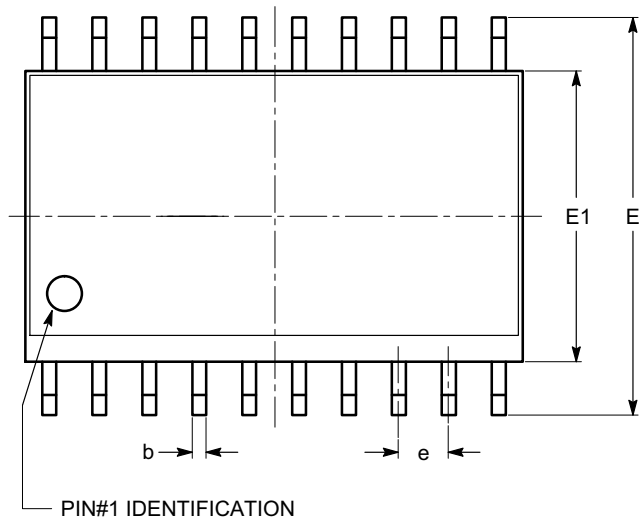
## PACKAGE DIMENSIONS

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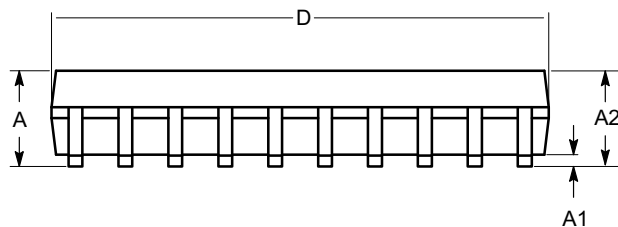
SOIC-20, 300 mils  
CASE 751BJ-01  
ISSUE O

DATE 19 DEC 2008

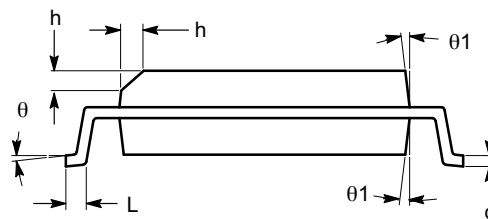


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
A2	2.05		2.55
b	0.31	0.41	0.51
c	0.20	0.27	0.33
D	12.60	12.80	13.00
E	10.01	10.30	10.64
E1	7.40	7.50	7.60
e	1.27 BSC		
h	0.25		0.75
L	0.40	0.81	1.27
$\theta$	0°		8°
$\theta 1$	5°		15°



SIDE VIEW



END VIEW

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-013.

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

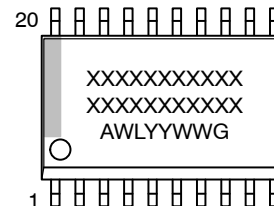
RECOMMENDED  
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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TSSOP-20 WB  
CASE 948E  
ISSUE D

DATE 17 FEB 2016

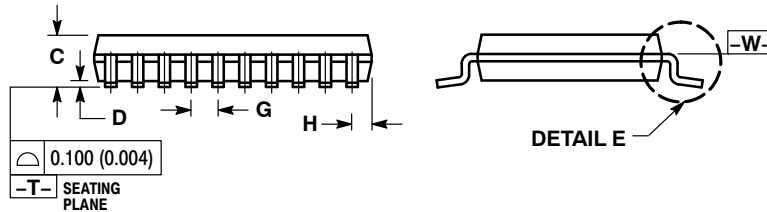
SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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