

MOSFET - Power, Single P-Channel, SOT-23 -50 V, 10 Ω

BSS84L, BVSS84L, SBSS84L

- SOT-23 Surface Mount Package Saves Board Space
- BV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	-50	Vdc
Gate-to-Source Voltage - Continuous	V_{GS}	± 20	Vdc
Drain Current Continuous @ $T_A = 25^\circ\text{C}$ Pulsed Drain Current ($t_p \leq 10 \mu\text{s}$)	I_D I_{DM}	-130 -520	mA
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	225	mW
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Thermal Resistance - Junction-to-Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Thermal Resistance - Junction-to-Ambient (Note 1)	$R_{\theta JA}$	377.2	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes, for 10 seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

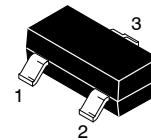
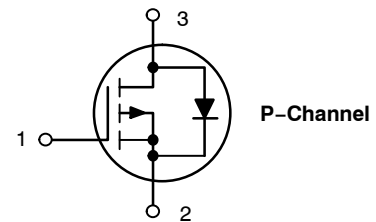
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. And the $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting the part on JEDEC Standard 51-3/51-7.



ON Semiconductor®

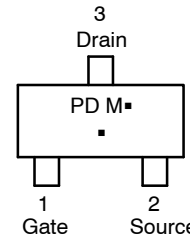
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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$
-50 V	10 Ω @ -10 V



SOT-23
CASE 318
STYLE 21

MARKING DIAGRAM & PIN ASSIGNMENT



PD = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
BSS84LT1G, BVSS84LT1G, SBSS84LT1G	SOT-23 (Pb-Free)	3,000 / Tape & Reel
BSS84LT7G	SOT-23 (Pb-Free)	3,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = -250\ \mu\text{Adc}$)	$V_{(BR)DSS}$	-50	-	-	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = -25\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) ($V_{DS} = -50\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) ($V_{DS} = -50\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	I_{DSS}	-	-	-0.1 -15 -60	μAdc
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	-	-	± 10	nAdc

ON CHARACTERISTICS (Note 2)

Gate-Source Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$)	$V_{GS(th)}$	-0.9	-	-2.0	Vdc
Static Drain-to-Source On-Resistance ($V_{GS} = -5.0\text{ Vdc}$, $I_D = -100\ \text{mAdc}$)	$R_{DS(on)}$	-	4.7	10	Ω
Transfer Admittance ($V_{DS} = -25\text{ Vdc}$, $I_D = -100\ \text{mAdc}$, $f = 1.0\text{ kHz}$)	$ Y_{fs} $	50	-	-	mS

DYNAMIC CHARACTERISTICS

Input Capacitance	$V_{DS} = 5.0\text{ Vdc}$	C_{iss}	-	36	-	pF
Output Capacitance	$V_{DS} = 5.0\text{ Vdc}$	C_{oss}	-	17	-	
Transfer Capacitance	$V_{DG} = 5.0\text{ Vdc}$	C_{rss}	-	6.5	-	

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$V_{DD} = -15\text{ Vdc}$, $I_D = -2.5\text{ Adc}$, $R_L = 50\ \Omega$	$t_{d(on)}$	-	3.6	-	ns
Rise Time		t_r	-	9.7	-	
Turn-Off Delay Time		$t_{d(off)}$	-	12	-	
Fall Time		t_f	-	1.7	-	
Gate Charge	$V_{DD} = -40\text{ Vdc}$, $I_D = -0.5\text{ A}$, $V_{GS} = -10\text{ V}$	Q_T	-	2.2	-	nC

SOURCE-DRAIN DIODE CHARACTERISTICS

Continuous Current		I_S	-	-	-0.130	A
Pulsed Current		I_{SM}	-	-	-0.520	
Forward Voltage (Note 3)	$V_{GS} = 0\text{ V}$, $I_S = -130\text{ mA}$	V_{SD}	-	-	-2.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
3. Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS



Figure 1. Transfer Characteristics

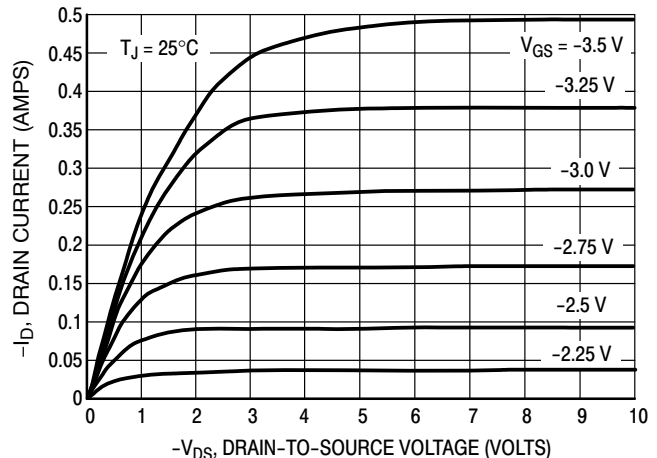


Figure 2. On-Region Characteristics

BSS84L, BVSS84L, SBSS84L

TYPICAL ELECTRICAL CHARACTERISTICS



Figure 3. On-Resistance versus Drain Current

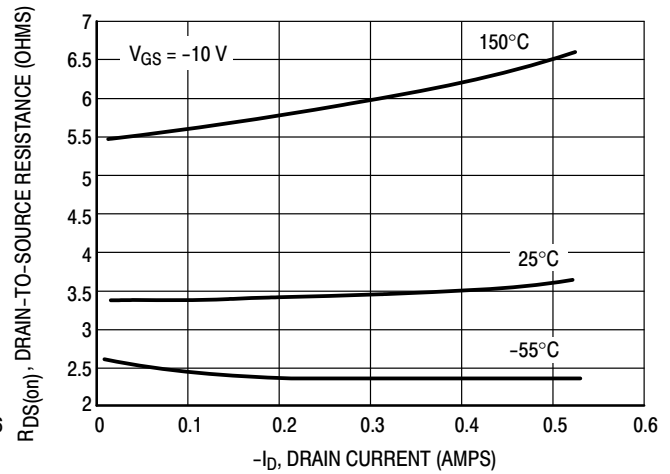


Figure 4. On-Resistance versus Drain Current

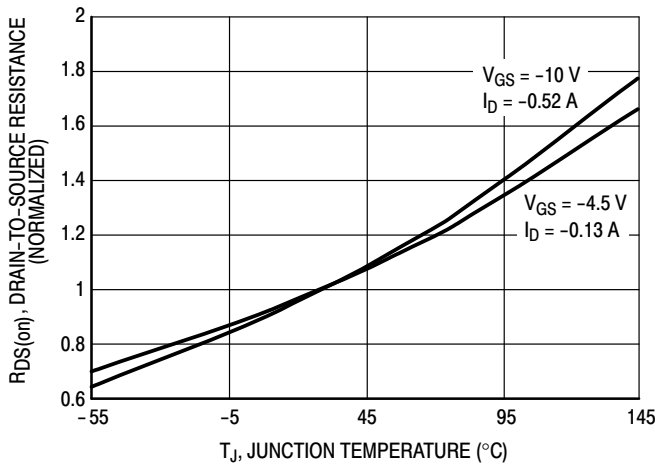


Figure 5. On-Resistance Variation with Temperature



Figure 6. Gate Charge

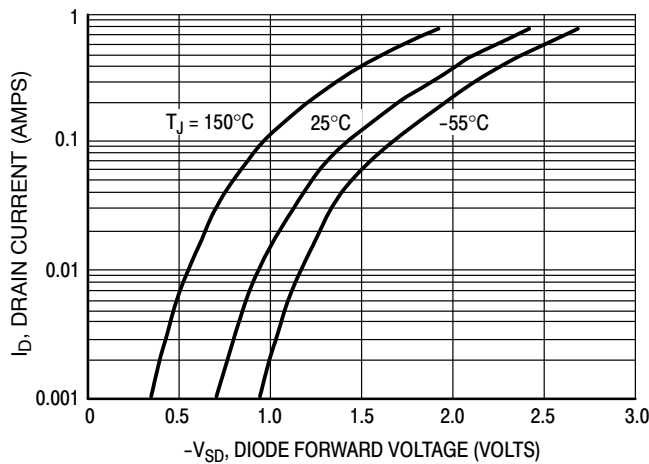


Figure 7. Body Diode Forward Voltage

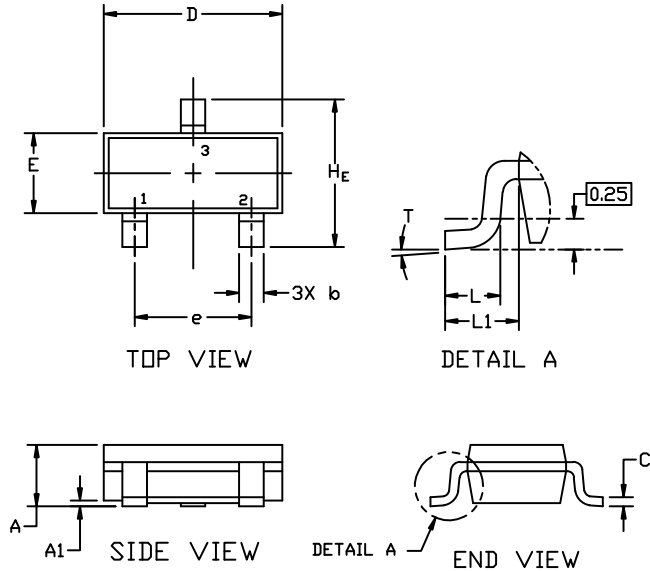
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SOT-23 (TO-236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1

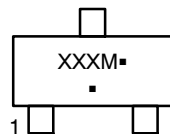


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

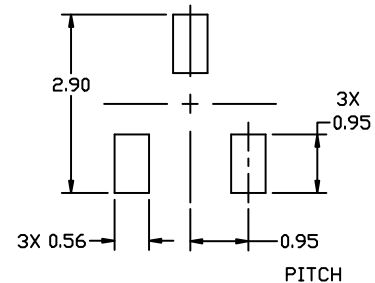
DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H _E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



SOT-23 (TO-236) CASE 318 ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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