

NTF5P03, NVF5P03

MOSFET – Power, P-Channel, SOT-223

-5.2 A, -30 V

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature SOT-223 Surface Mount Package
- Avalanche Energy Specified
- AEC-Q101 Qualified and PPAP Capable – NVF5P03T3G
- These Devices are Pb-Free and are RoHS Compliant

Applications

- DC-DC Converters
- Power Management
- Motor Controls
- Inductive Loads
- Replaces MMFT5P03HD

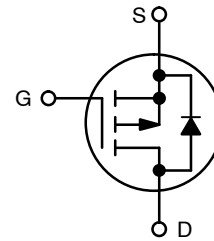


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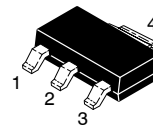
<http://onsemi.com>

-5.2 AMPERES, -30 VOLTS

$R_{DS(on)} = 100 \text{ m}\Omega$

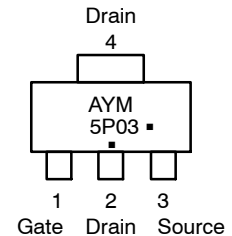


P-Channel MOSFET



**SOT-223
CASE 318E
STYLE 3**

MARKING DIAGRAM & PIN ASSIGNMENT



- A = Assembly Location
- Y = Year
- M = Date Code
- 5P03 = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTF5P03T3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NVF5P03T3G	SOT-223 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTF5P03, NVF5P03

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Negative sign for P-Channel devices omitted for clarity

Rating		Symbol	Max	Unit
Drain-to-Source Voltage		V_{DSS}	-30	V
Drain-to-Gate Voltage ($R_{GS} = 1.0\text{ M}\Omega$)		V_{DGR}	-30	V
Gate-to-Source Voltage - Continuous		V_{GS}	± 20	V
1 sq in FR-4 or G-10 PCB 10 seconds	Thermal Resistance - Junction to Ambient	R_{THJA}	40	$^\circ\text{C}/\text{W}$
	Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	3.13	Watts
	Linear Derating Factor		25	$\text{mW}/^\circ\text{C}$
	Drain Current - Continuous @ $T_A = 25^\circ\text{C}$	I_D	-5.2	A
Minimum FR-4 or G-10 PCB 10 seconds	Drain Current - Continuous @ $T_A = 70^\circ\text{C}$	I_D	-4.1	A
	Pulsed Drain Current (Note 1)	I_{DM}	-26	A
	Thermal Resistance - Junction to Ambient	R_{THJA}	80	$^\circ\text{C}/\text{W}$
	Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.56	Watts
	Linear Derating Factor		12.5	$\text{mW}/^\circ\text{C}$
	Drain Current - Continuous @ $T_A = 25^\circ\text{C}$	I_D	-3.7	A
	Continuous @ $T_A = 70^\circ\text{C}$	I_D	-2.9	A
	Pulsed Drain Current (Note 1)	I_{DM}	-19	A
Operating and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = -30\text{ Vdc}$, $V_{GS} = -10\text{ Vdc}$, Peak $I_L = -12\text{ Apk}$, $L = 3.5\text{ mH}$, $R_G = 25\ \Omega$)		E_{AS}	250	mJ

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Repetitive rating; pulse width limited by maximum junction temperature.

NTF5P03, NVF5P03

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Cpk ≥ 2.0) (Notes 2 and 4) (V _{GS} = 0 Vdc, I _D = -250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	-30 -	- -28	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = -24 Vdc, V _{GS} = 0 Vdc) (V _{DS} = -24 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	- -	- -	-1.0 -25	μAdc
Gate-Body Leakage Current (V _{GS} = ± 20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	± 100	nAdc

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage (Cpk ≥ 2.0) (Notes 2 and 4) (V _{DS} = V _{GS} , I _D = -250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	-1.0 -	-1.75 3.5	-3.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Cpk ≥ 2.0) (Notes 2 and 4) (V _{GS} = -10 Vdc, I _D = -5.2 Adc) (V _{GS} = -4.5 Vdc, I _D = -2.6 Adc)	R _{DS(on)}	-	76 107	100 150	mΩ
Forward Transconductance (Note 2) (V _{DS} = -15 Vdc, I _D = -2.0 Adc)	g _{fs}	2.0	3.9	-	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = -25 Vdc, V _{GS} = 0 V, f = 1.0 MHz)	C _{iss}	-	500	950	pF
Output Capacitance		C _{oss}	-	153	440	
Transfer Capacitance		C _{rss}	-	58	140	

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	(V _{DD} = -15 Vdc, I _D = -4.0 Adc, V _{GS} = -10 Vdc, R _G = 6.0 Ω) (Note 2)	t _{d(on)}	-	10	24	ns
Rise Time		t _r	-	33	48	
Turn-Off Delay Time		t _{d(off)}	-	38	94	
Fall Time		t _f	-	20	92	
Turn-On Delay Time	(V _{DD} = -15 Vdc, I _D = -2.0 Adc, V _{GS} = -10 Vdc, R _G = 6.0 Ω) (Note 2)	t _{d(on)}	-	16	38	ns
Rise Time		t _r	-	45	110	
Turn-Off Delay Time		t _{d(off)}	-	23	60	
Fall Time		t _f	-	24	80	
Gate Charge	(V _{DS} = -24 Vdc, I _D = -4.0 Adc, V _{GS} = -10 Vdc) (Note 2)	Q _T	-	15	38	nC
		Q ₁	-	1.6	-	
		Q ₂	-	3.5	-	
		Q ₃	-	2.6	-	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = -4.0 Adc, V _{GS} = 0 Vdc) (I _S = -4.0 Adc, V _{GS} = 0 Vdc, T _J = 125°C) (Note 2)	V _{SD}	- -	-1.1 -0.89	-1.5 -	Vdc
Reverse Recovery Time	(I _S = -4.0 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs) (Note 2)	t _{rr}	-	34	-	ns
		t _a	-	20	-	
		t _b	-	14	-	
Reverse Recovery Stored Charge		Q _{RR}	-	0.036	-	μC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. Switching characteristics are independent of operating junction temperatures.
4. Reflects typical values.

$$C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$$

TYPICAL ELECTRICAL CHARACTERISTICS

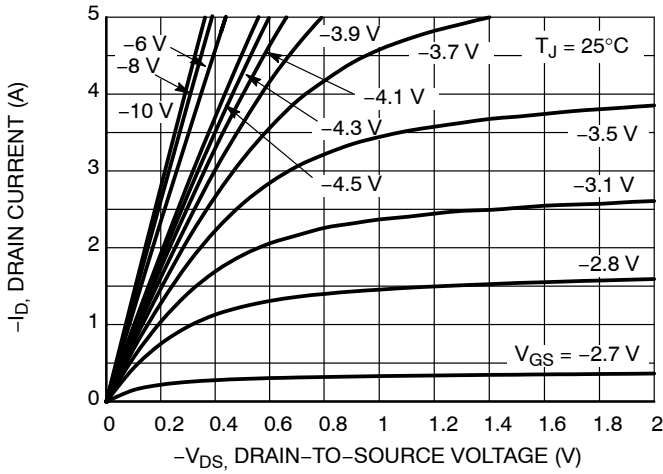


Figure 1. On-Region Characteristics

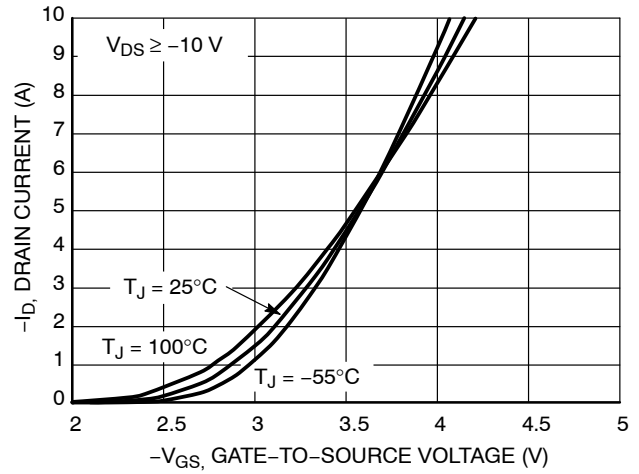


Figure 2. Transfer Characteristics

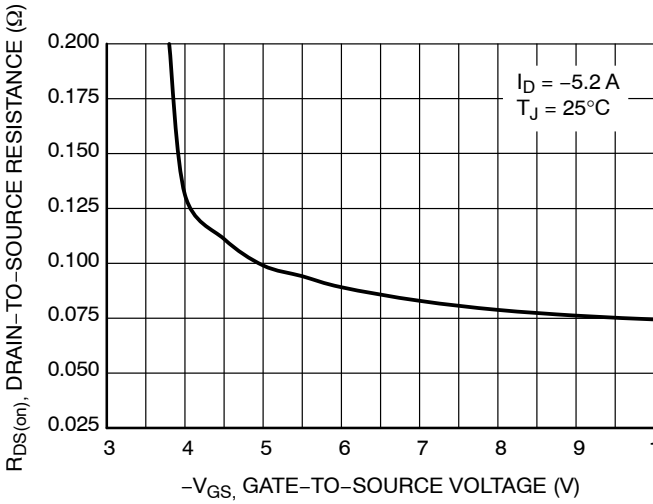


Figure 3. On-Resistance versus Gate-to-Source Voltage

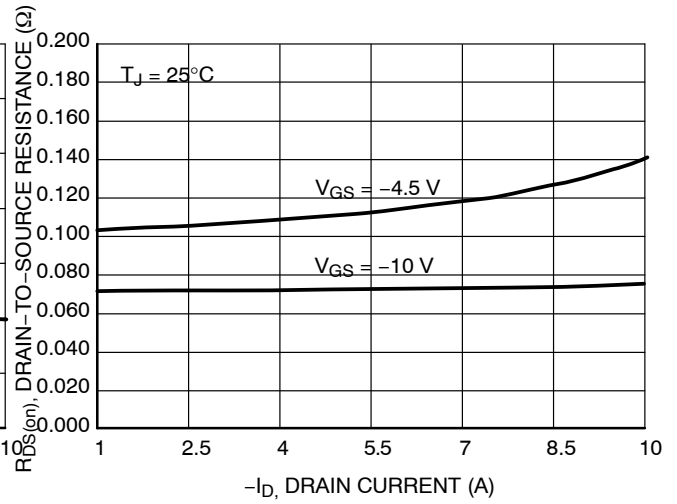


Figure 4. On-Resistance versus Drain Current and Gate Voltage

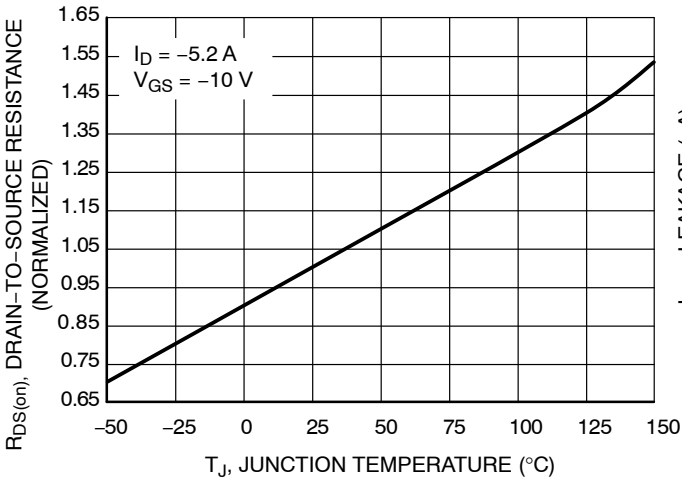


Figure 5. On-Resistance Variation with Temperature

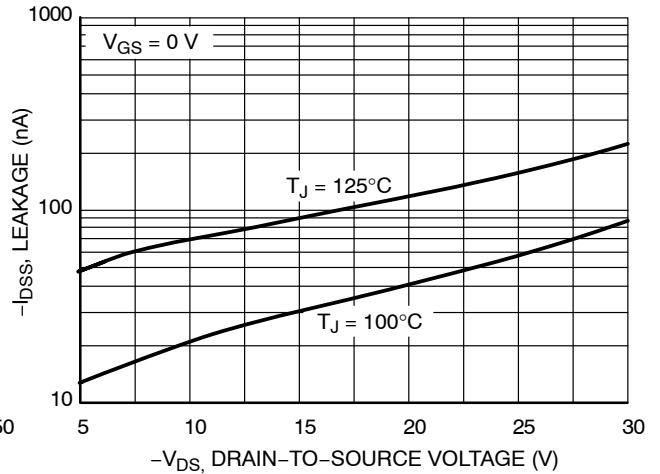


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

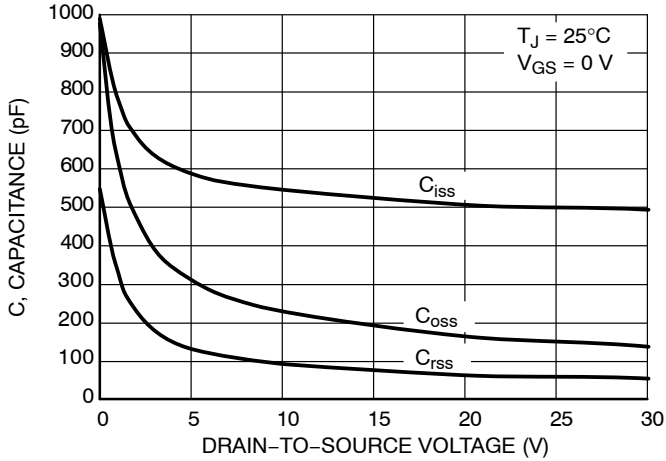


Figure 7. Capacitance Variation

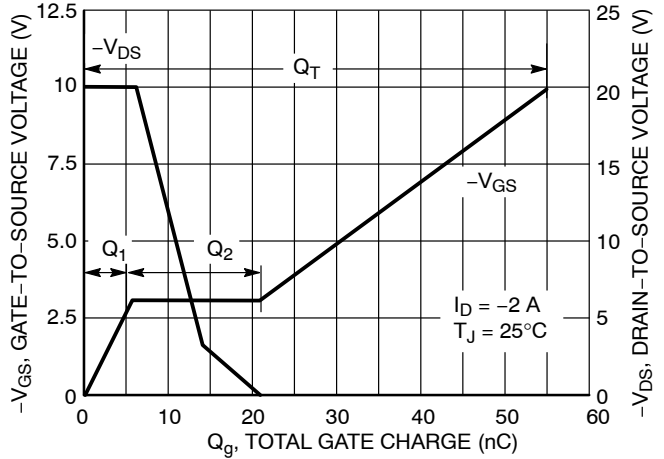


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

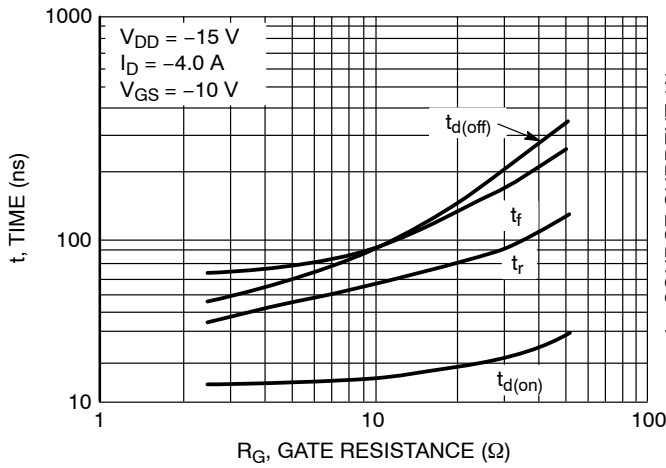


Figure 9. Resistive Switching Time Variation versus Gate Resistance

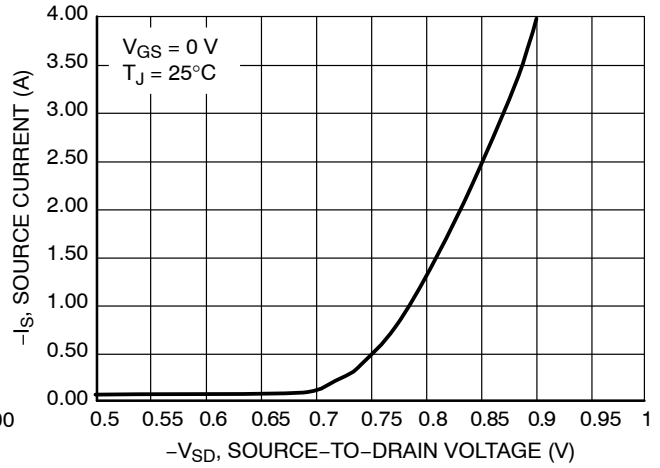
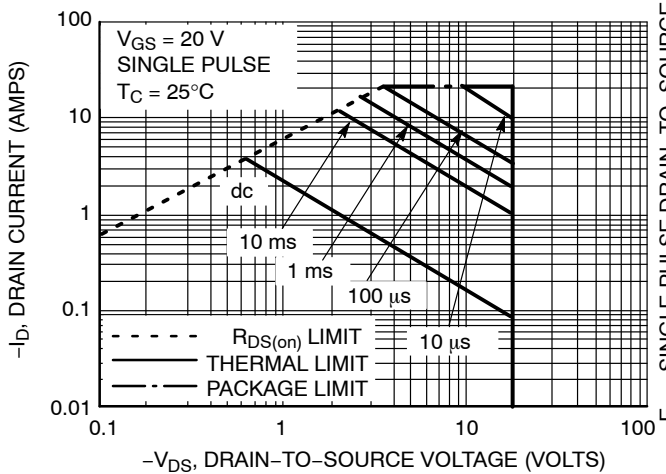


Figure 10. Diode Forward Voltage versus Current



Mounted on 2"sq. FR4 board (1"sq. 2 oz. Cu 0.06" thick single sided) with on die operating, 10 s max.

Figure 11. Maximum Rated Forward Biased Safe Operating Area

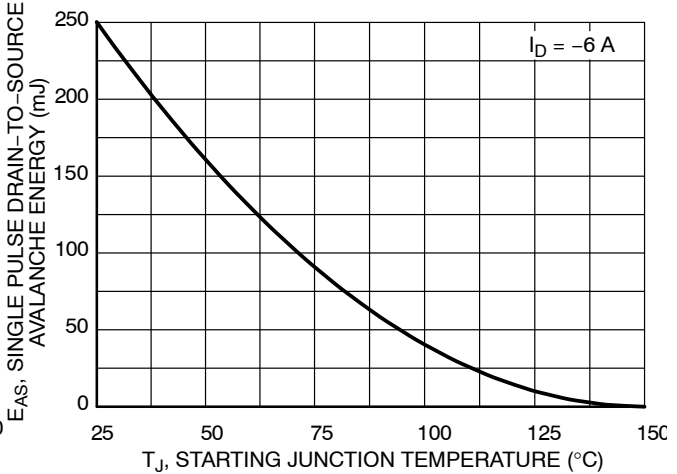


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

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TYPICAL ELECTRICAL CHARACTERISTICS

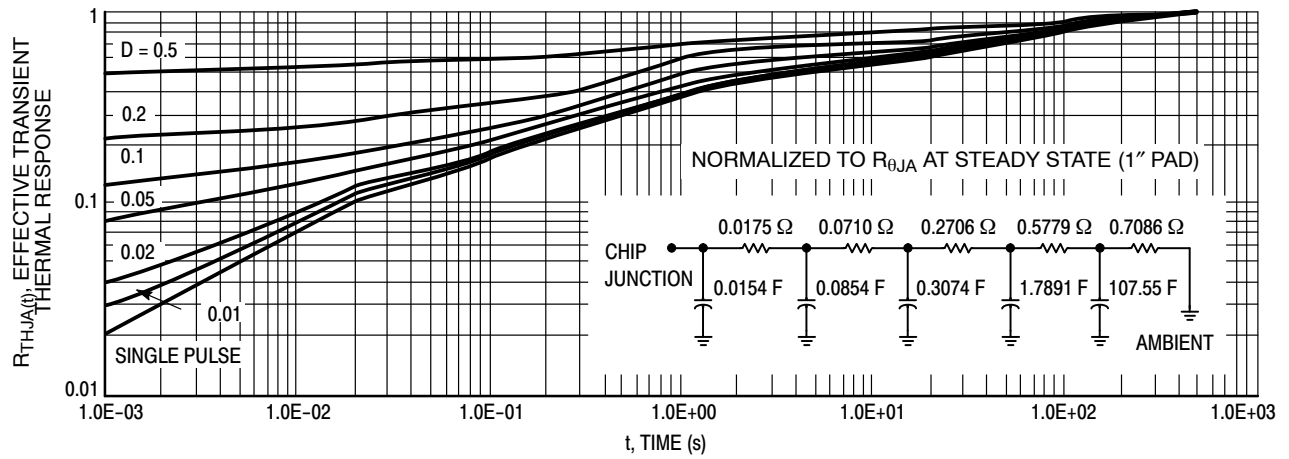


Figure 13. FET Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

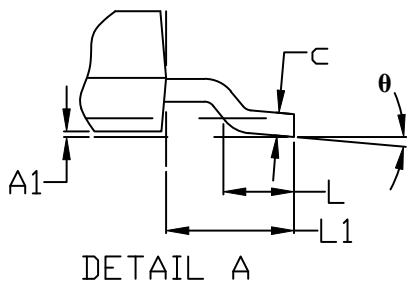
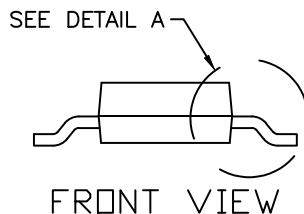
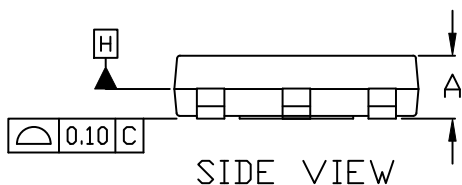
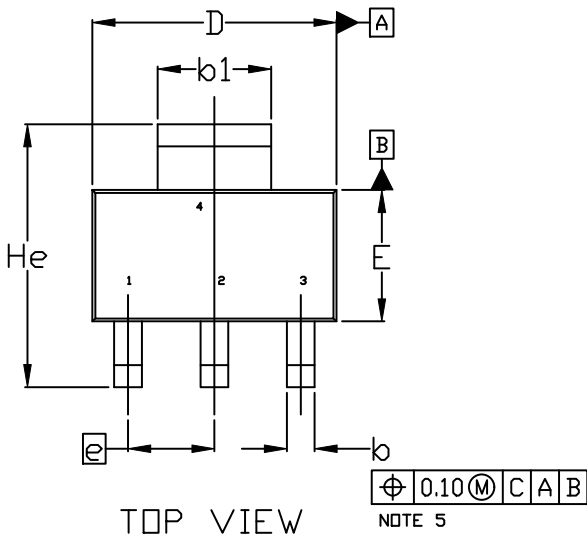
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SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

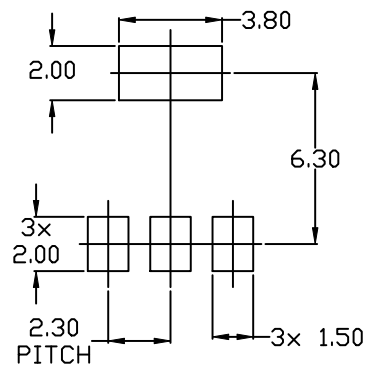
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

- | | | | | |
|--|---|---|---|---|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE | STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN | STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE |
| STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT | STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE | STYLE 8:
CANCELLED | STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE |
| STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2 | STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT | STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | | |

**GENERIC
 MARKING DIAGRAM***




- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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