MOSFET – Dual, N-Channel, POWERTRENCH®

30 V, 0.75 A, 0.4 Ω

FDG8850NZ

General Description

This dual N−Channel logic level enhancement mode field effect transistors are produced using **onsemi**'s proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on−state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.

Features

- Max $R_{DS(on)}$ = 0.4 Ω at V_{GS} = 4.5 V, I_D = 0.75 A
- Max $R_{DS(on)}$ = 0.5 Ω at V_{GS} = 2.7 V, I_D = 0.67 A
- Very Low Level Gate Drive Requirements Allowing Operation in 3 V Circuits ($V_{GS(th)}$ < 1.5 V)
- Very Small Package Outline SC−70 6 Lead
- This Device is Pb−Free, Halide Free and is RoHS Compliant

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

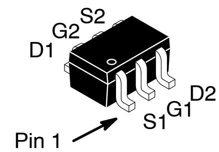
Symbol	Parameter		Ratings	Unit
V_{DS}	Drain to Source Voltage		30	V
V_{GS}	Gate to Source Voltage		±12	V
I_D	Drain Current	Continuous	0.75	A
		Pulsed	2.2	
P_D	Power Dissipation	(Note 1a)	0.36	W
		(Note 1b)	0.30	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

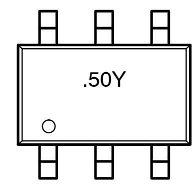
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Single Operation (Note 1a)	350	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Single Operation (Note 1b)	415	

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
30 V	0.4 Ω @ 4.5 V	0.75 A
	0.5 Ω @ 2.7 V	



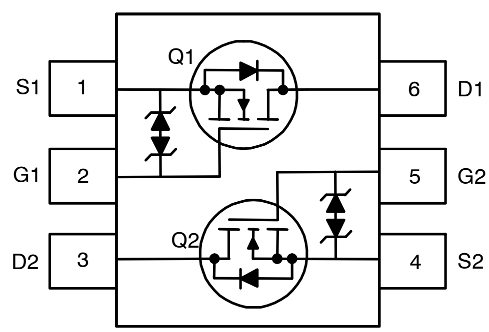
SC−88 (SC−70 6 Lead), 1.25 x 2
CASE 419AD−01

MARKING DIAGRAM



.50 = Specific Device Code
Y = 1−Digit Weekly Date Code

PIN ASSIGNMENT



NOTE: The pinouts are symmetrical; pin 1 and 4 are interchangeable. Units inside the carrier can be of either orientation and will not affect the functionality of the device.

ORDERING INFORMATION

Device	Package	Shipping†
FDG8850NZ	SC−88 (SC−70 6 Lead), 1.25 x 2	3000 / Tape & Reel

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

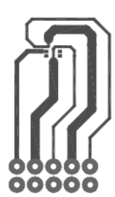
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	25	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±12 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	0.65	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	–3.0	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 4.5 V, I_D = 0.75 A	–	0.25	0.4	Ω
		V_{GS} = 2.7 V, I_D = 0.67 A	–	0.29	0.5	
		V_{GS} = 4.5 V, I_D = 0.75 A, T_J = 125°C	–	0.36	0.6	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 0.75 A	–	3	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	–	90	120	pF
C_{oss}	Output Capacitance		–	20	30	pF
C_{rss}	Reverse Transfer Capacitance		–	15	25	pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 5 V, I_D = 0.5 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω	–	4	10	ns
t_r	Rise Time		–	1	10	ns
$t_{d(off)}$	Turn–Off Delay Time		–	9	18	ns
t_f	Fall Time		–	1	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 4.5 V, V_{DD} = 5 V, I_D = 0.75 A	–	1.03	1.44	nC
Qgs	Gate to Source Charge		–	0.29	–	nC
Qgd	Gate to Drain "Miller" Charge		–	0.17	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain–Source Diode Forward Current		–	–	0.3	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.3 A (Note 2)	–	0.76	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a. 350°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 415°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

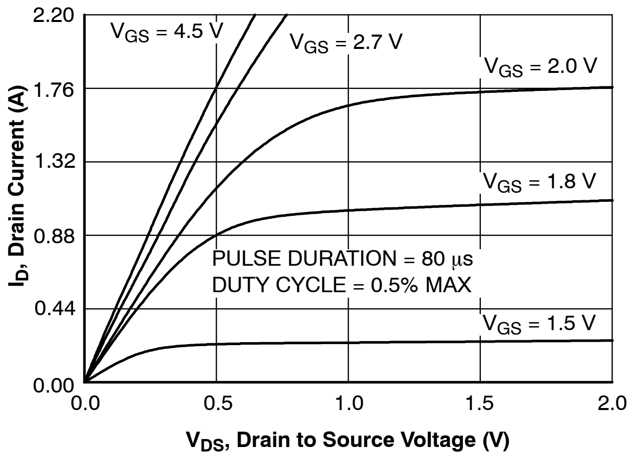


Figure 1. On−Region Characteristics

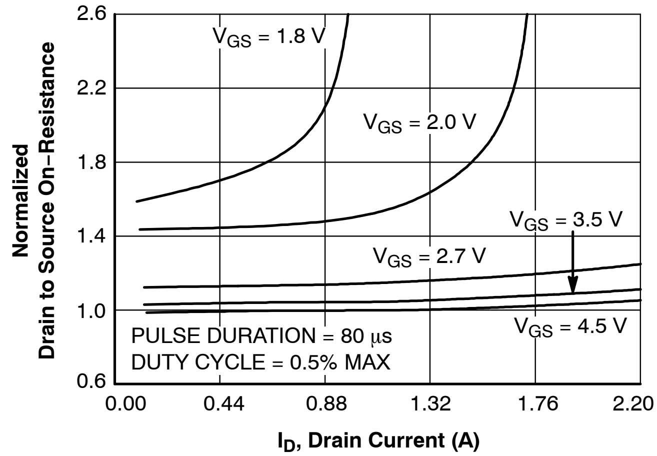


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

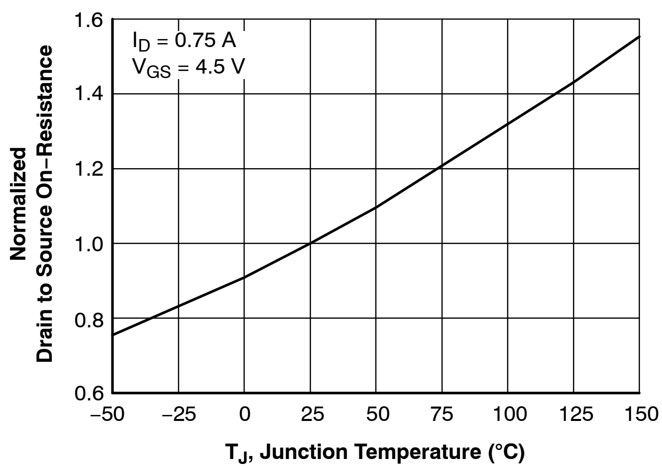


Figure 3. Normalized On−Resistance vs. Junction Temperature

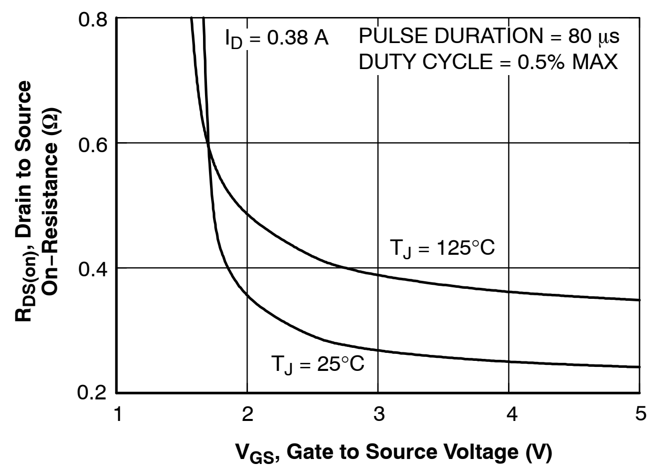


Figure 4. On−Resistance vs. Gate to Source Voltage

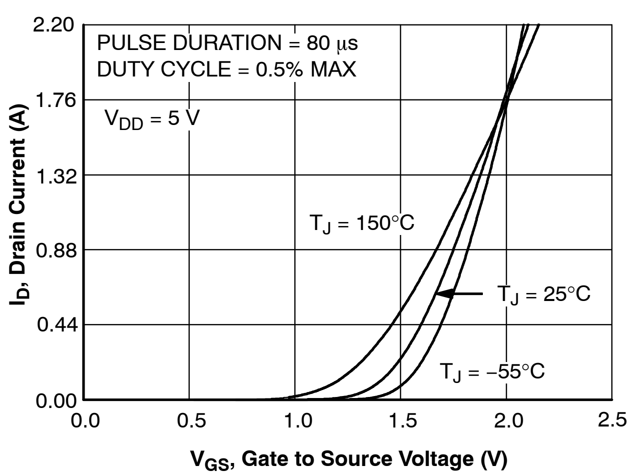


Figure 5. Transfer Characteristics

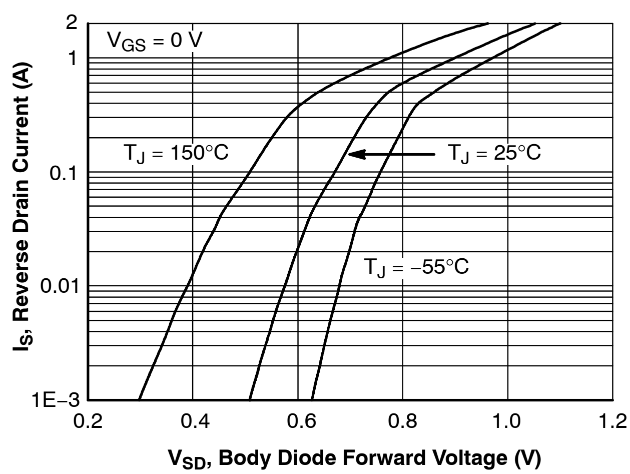


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

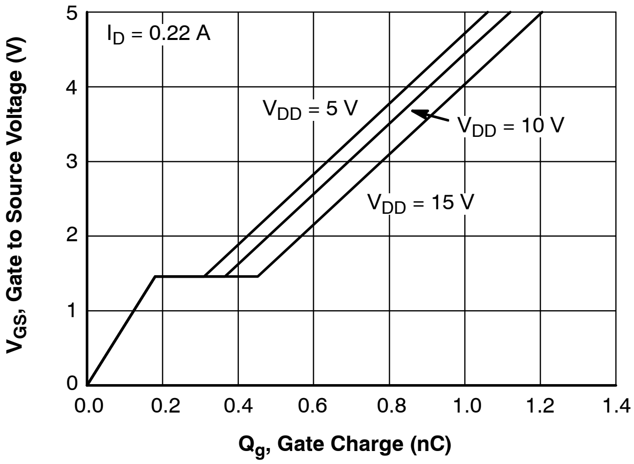


Figure 7. Gate Charge Characteristics

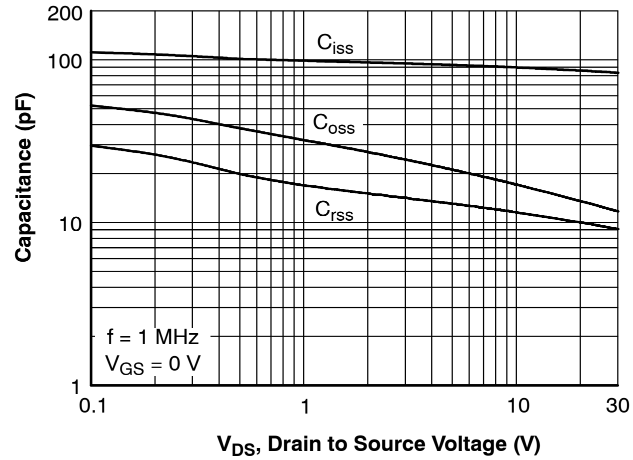


Figure 8. Capacitance vs. Drain to Source Voltage

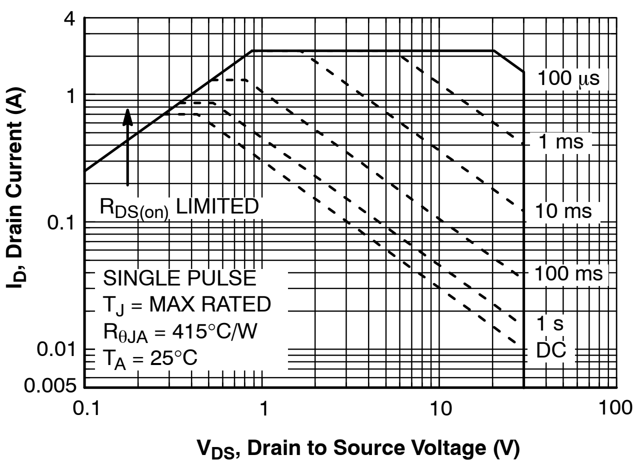


Figure 9. Forward Bias Safe Operating Area

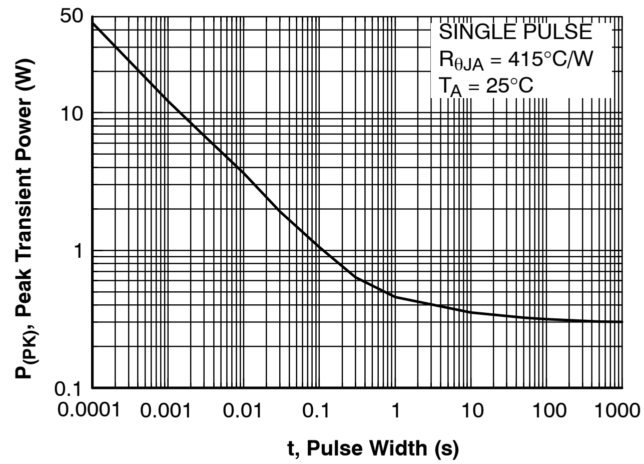


Figure 10. Single Pulse Maximum Power Dissipation

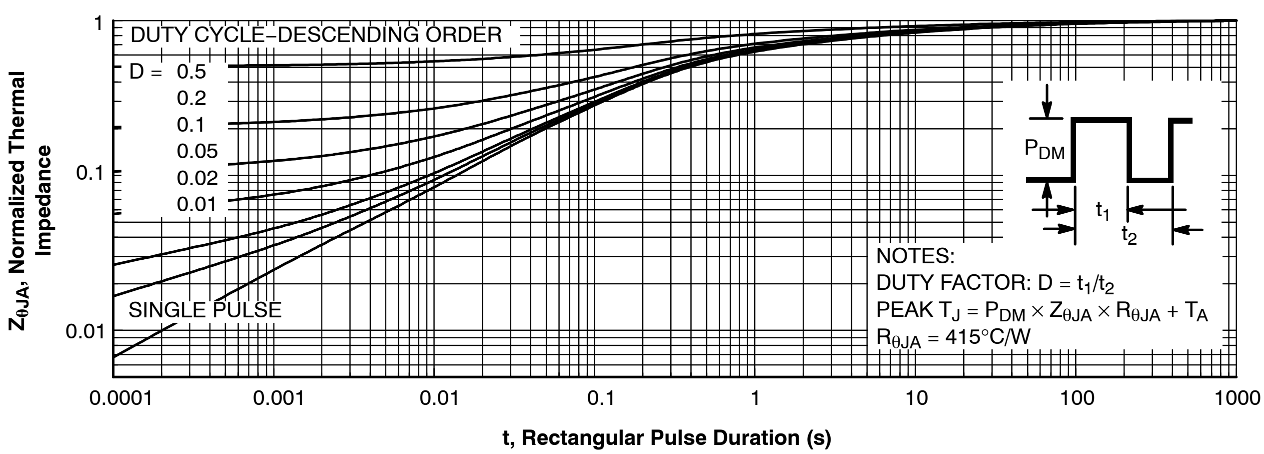
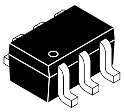
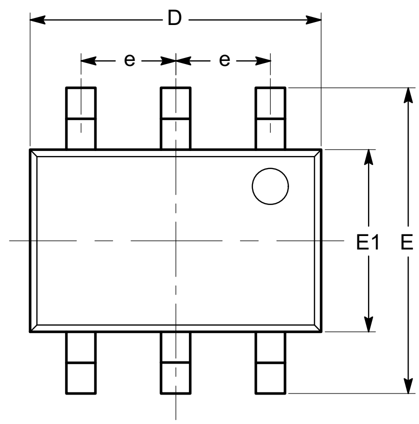


Figure 11. Transient Thermal Response Curve



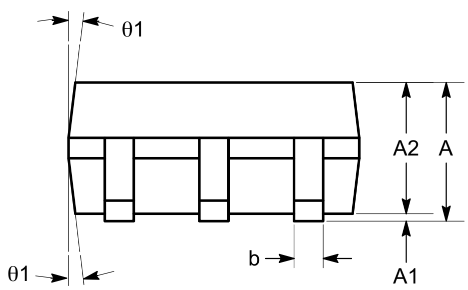
SC−88 (SC−70 6 Lead), 1.25x2
CASE 419AD
ISSUE A

DATE 07 JUL 2010

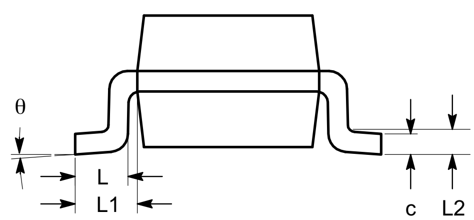


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
L2	0.15 BSC		
θ	0º		8º
θ1	4º		10º



SIDE VIEW



END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

DOCUMENT NUMBER:	98AON34266E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SC−88 (SC−70 6 LEAD), 1.25X2	PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

◊