

# MOSFET – Dual, N-Channel, POWERTRENCH®

**30 V, 0.75 A, 0.4 Ω**

## FDG8850NZ

### General Description

This dual N-Channel logic level enhancement mode field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.

### Features

- Max  $R_{DS(on)}$  = 0.4 Ω at  $V_{GS} = 4.5$  V,  $I_D = 0.75$  A
- Max  $R_{DS(on)}$  = 0.5 Ω at  $V_{GS} = 2.7$  V,  $I_D = 0.67$  A
- Very Low Level Gate Drive Requirements Allowing Operation in 3 V Circuits ( $V_{GS(th)} < 1.5$  V)
- Very Small Package Outline SC-70 6 Lead
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

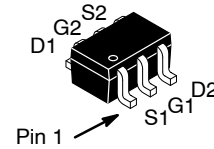
Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 12$	V
$I_D$	Drain Current	Continuous	0.75
		Pulsed	2.2
$P_D$	Power Dissipation	(Note 1a)	0.36
		(Note 1b)	0.30
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

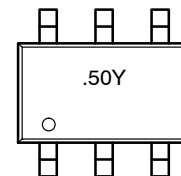
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Single Operation (Note 1a)	350	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Single Operation (Note 1b)	415	

$V_{DS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
30 V	0.4 Ω @ 4.5 V	0.75 A
	0.5 Ω @ 2.7 V	



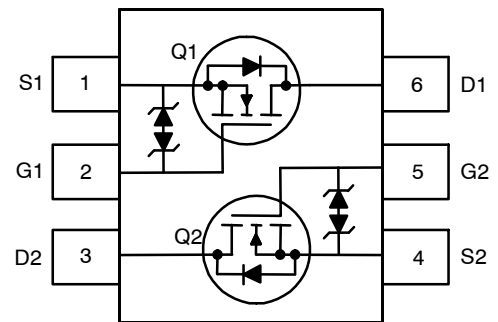
SC-88 (SC-70 6 Lead), 1.25 x 2  
CASE 419AD-01

### MARKING DIAGRAM



.50 = Specific Device Code  
Y = 1-Digit Weekly Date Code

### PIN ASSIGNMENT



NOTE: The pinouts are symmetrical; pin 1 and 4 are interchangeable. Units inside the carrier can be of either orientation and will not affect the functionality of the device.

### ORDERING INFORMATION

Device	Package	Shipping†
FDG8850NZ	SC-88 (SC-70 6 Lead), 1.25 x 2	3000 / Tape & Reel

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# FDG8850NZ

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### OFF CHARACTERISTICS

B <sub>V</sub> DSS	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	30	–	–	V
$\frac{\Delta B_{V_{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	25	–	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V	–	–	1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±12 V, V <sub>DS</sub> = 0 V	–	–	±10	μA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	0.65	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	–3.0	–	mV/°C
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.75 A	–	0.25	0.4	Ω
		V <sub>GS</sub> = 2.7 V, I <sub>D</sub> = 0.67 A	–	0.29	0.5	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.75 A, T <sub>J</sub> = 125°C	–	0.36	0.6	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 0.75 A	–	3	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	90	120	pF
C <sub>oss</sub>	Output Capacitance		–	20	30	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	15	25	pF

### SWITCHING CHARACTERISTICS (Note 2)

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 5 V, I <sub>D</sub> = 0.5 A, V <sub>GS</sub> = 4.5 V, R <sub>GEN</sub> = 6 Ω	–	4	10	ns
t <sub>r</sub>	Rise Time		–	1	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	9	18	ns
t <sub>f</sub>	Fall Time		–	1	10	ns
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 4.5 V, V <sub>DD</sub> = 5 V, I <sub>D</sub> = 0.75 A	–	1.03	1.44	nC
Q <sub>gs</sub>	Gate to Source Charge		–	0.29	–	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		–	0.17	–	nC

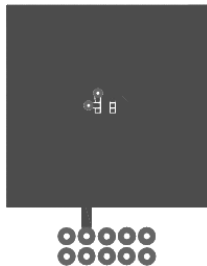
### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	–	–	0.3	A	
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 0.3 A (Note 2)	–	0.76	1.2	V

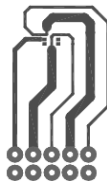
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### NOTES:

- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a. 350°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 415°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

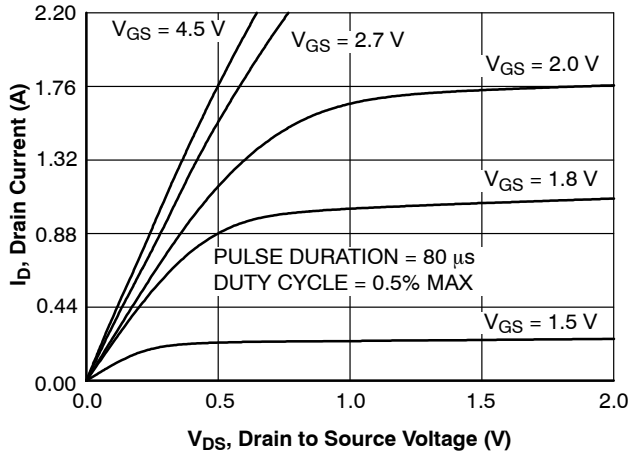


Figure 1. On-Region Characteristics

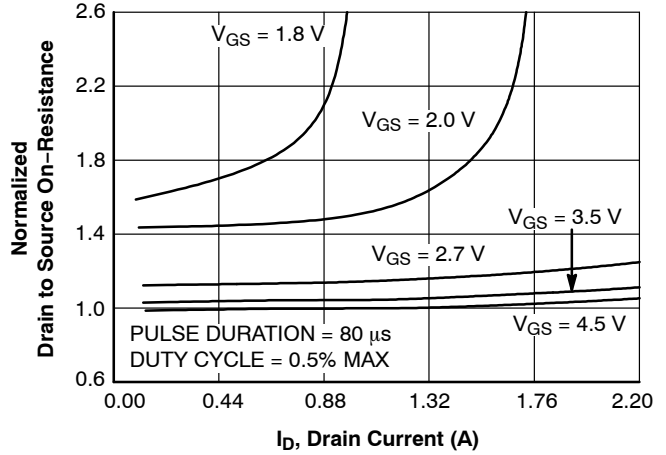


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

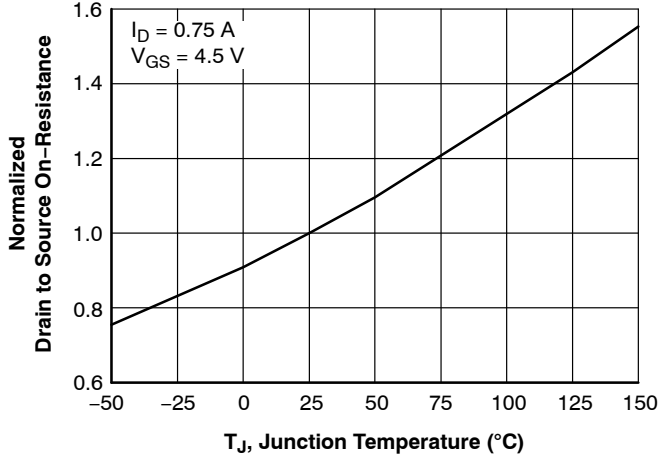


Figure 3. Normalized On-Resistance vs. Junction Temperature

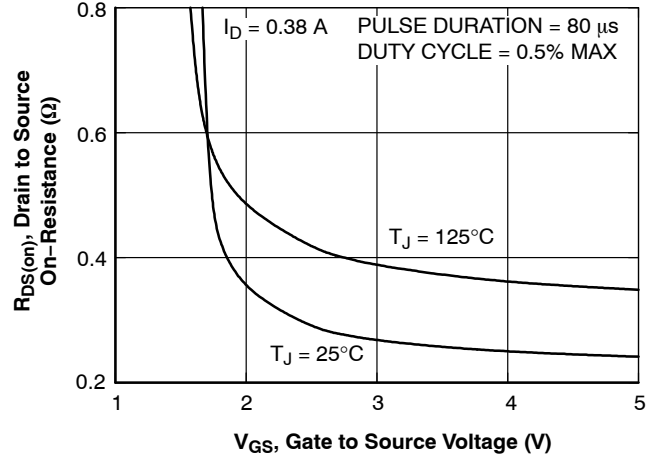


Figure 4. On-Resistance vs. Gate to Source Voltage

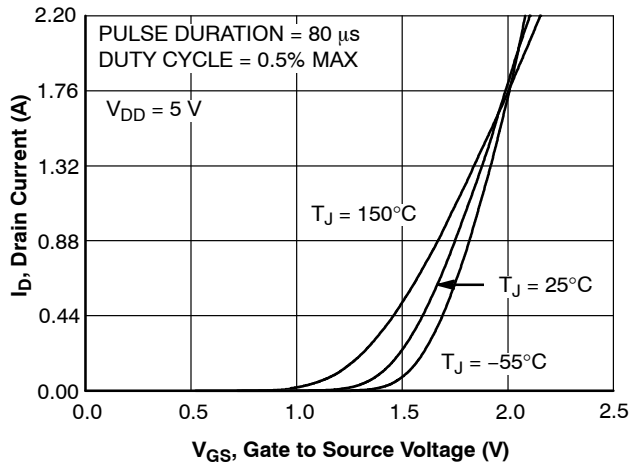


Figure 5. Transfer Characteristics

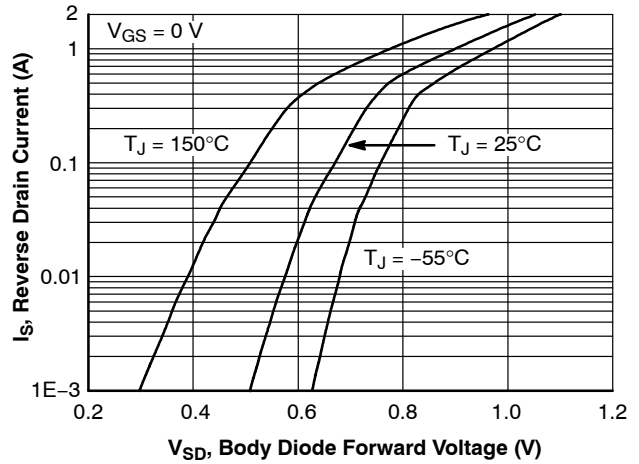


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# FDG8850NZ

## TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

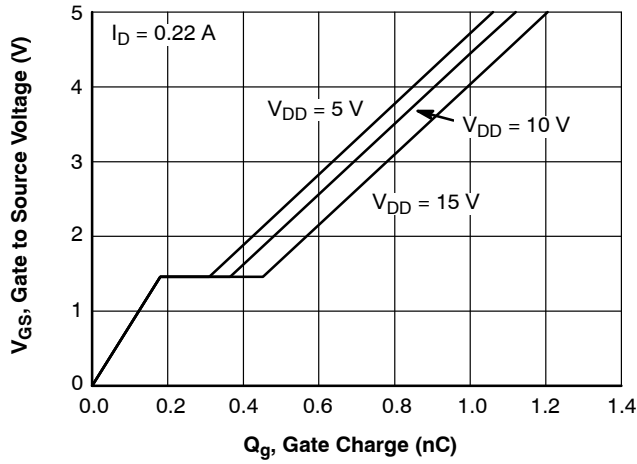


Figure 7. Gate Charge Characteristics

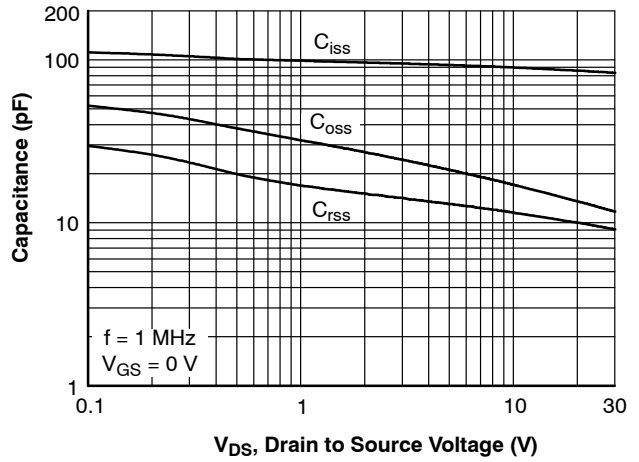


Figure 8. Capacitance vs. Drain to Source Voltage

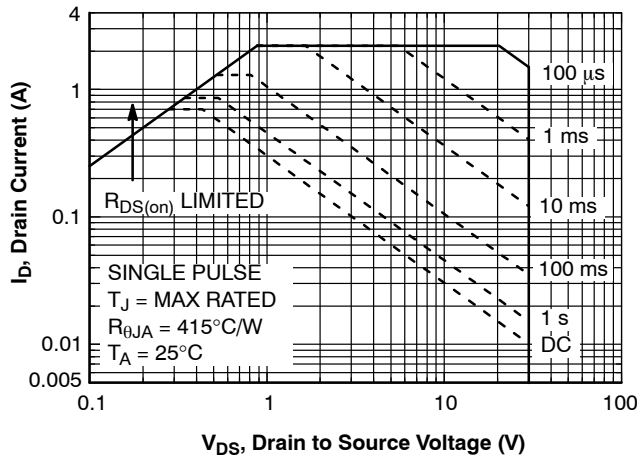


Figure 9. Forward Bias Safe Operating Area

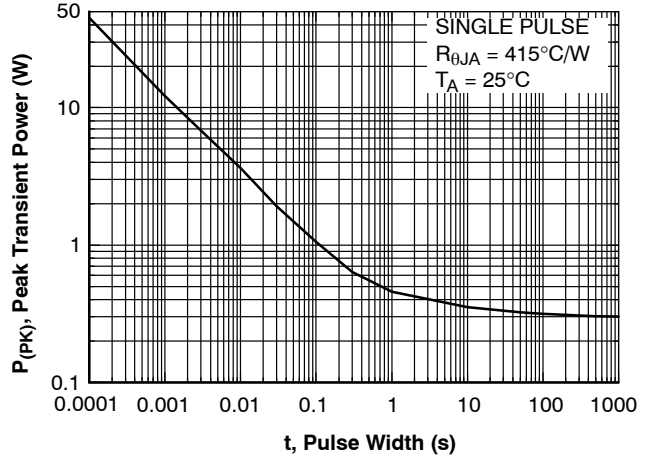


Figure 10. Single Pulse Maximum Power Dissipation

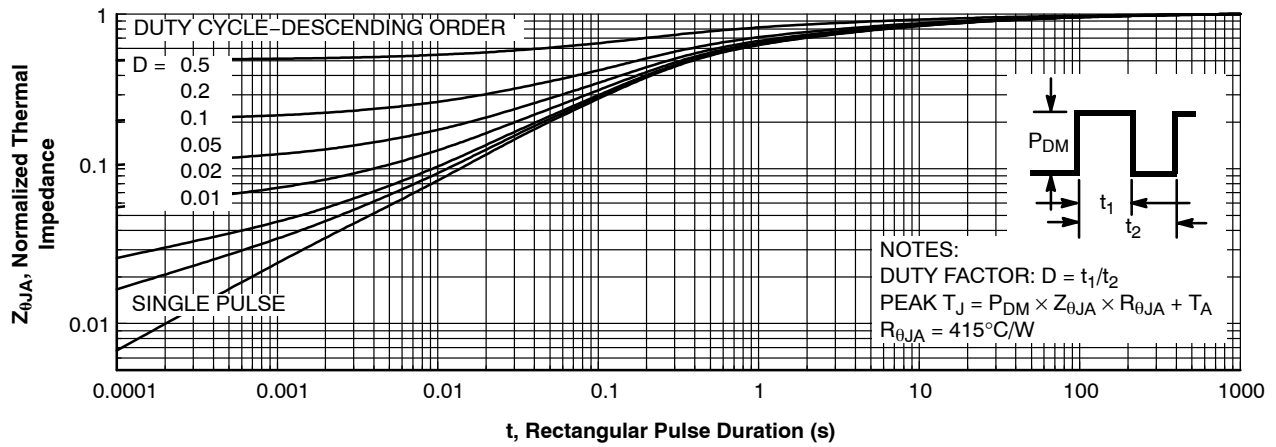
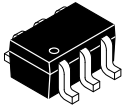


Figure 11. Transient Thermal Response Curve

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# MECHANICAL CASE OUTLINE

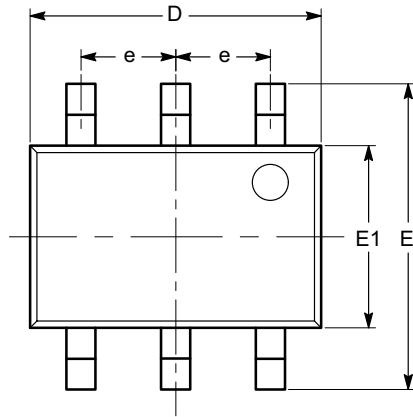
## PACKAGE DIMENSIONS



1

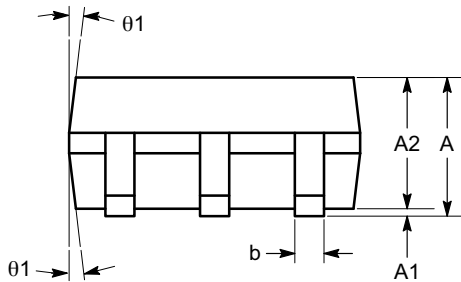
SC-88 (SC-70 6 Lead), 1.25x2  
CASE 419AD  
ISSUE A

DATE 07 JUL 2010

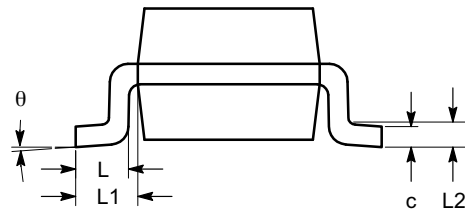


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
L2	0.15 BSC		
$\theta$	0°		8°
$\theta_1$	4°		10°



SIDE VIEW



END VIEW

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

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