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April 2009

FDS4435BZ

P-Channel PowerTrench[®] MOSFET -30V, -8.8A, 20m Ω

Features

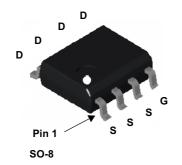
- Max $r_{DS(on)}$ = 20m Ω at V_{GS} = -10V, I_D = -8.8A
- Max $r_{DS(on)}$ = 35m Ω at V_{GS} = -4.5V, I_D = -6.7A
- Extended V_{GSS} range (-25V) for battery applications
- HBM ESD protection level of ±3.8KV typical (note 3)
- High performance trench technology for extremely low r_{DS(on)}
- High power and current handling capability
- Termination is Lead-free and RoHS compliant

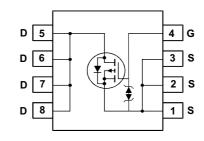


General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Param		Ratings	Units	
V _{DS}	Drain to Source Voltage			-30	V
V_{GS}	Gate to Source Voltage			±25	V
ı	Drain Current -Continuous	T _A = 25°C	(Note 1a)	-8.8	А
'D	-Pulsed			-50	_ ^
В	Power Dissipation	T _A = 25°C	(Note 1a)	2.5	W
P_{D}	Power Dissipation	T _A = 25°C	(Note 1b)	1.0	VV
E _{AS}	Single Pulse Avalanche Energy		(Note 4)	24	mJ
T _J , T _{STG}	Operating and Storage Junction Tempera	ature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS4435BZ	FDS4435BZ	SO-8	13"	12mm	2500units

©2009 Fairchild Semiconductor Corporation FDS4435BZ Rev.C1

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I _D = -250μA, referenced to 25°C		-21		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24V, V_{GS} = 0V$			1	μΑ
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25V$, $V_{DS} = 0V$			±10	μА

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-1	-2.1	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25°C		6		mV/°C
		$V_{GS} = -10V, I_D = -8.8A$		16	20	
r _{DS(on)}	r _{DS(on)} Static Drain to Source On Resistance	$V_{GS} = -4.5V, I_D = -6.7A$		26	35	mΩ
, ,	$V_{GS} = -10V$, $I_D = -8.8A$, $T_J = 125$ °C		22	28		
9 _{FS}	Forward Transconductance	$V_{DS} = -5V, I_{D} = -8.8A$		24		S

Dynamic Characteristics

C _{iss}	Input Capacitance	15)/)/ 0)/		1385	1845	pF
C _{oss}	Output Capacitance	─V _{DS} = -15V, V _{GS} = 0V, —f = 1MHz		275	365	pF
C _{rss}	Reverse Transfer Capacitance	1 - 11VII 12		230	345	pF
R_g	Gate Resistance	f = 1MHz		4.5		Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		10	20	ns
t _r	Rise Time	V_{DD} = -15V, I_{D} = -8.8A, V_{GS} = -10V, R_{GEN} = 6Ω	6	12	ns
t _{d(off)}	Turn-Off Delay Time	V _{GS} = -10V, K _{GEN} = 012	30	48	ns
t _f	Fall Time		12	22	ns
Q_g	Total Gate Charge	V _{GS} = 0V to -10V	28	40	nC
Q_g	Total Gate Charge	$V_{GS} = 0V \text{ to } -5V$ $V_{DD} = -15V,$ $I_{D} = -8.8A$	16	23	nC
Q _{gs}	Gate to Source Charge	I _D 8.8A	5.2		nC
Q_{gd}	Gate to Drain "Miller" Charge		7.4		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0V, I _S = -8.8A (Note 2)		-0.9	-1.2	V
t _{rr}	Reverse Recovery Time	I _E = -8.8A. di/dt = 100A/us		29	44	ns
Q _{rr}	Reverse Recovery Charge	1 _F = -8.8A, α//αι = 100Α/μ\$		23	35	nC

NOTES:

^{1.} R_{0,1A} is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0,1C} is guaranteed by design while R_{0,1C} is determined by the user's board design.



a. 50°C/W when mounted on a 1 in² pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.
- 3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
- 4. Starting T_J = 25°C, L = 1mH, $I_{\mbox{\scriptsize AS}}$ = -7A, $V_{\mbox{\scriptsize DD}}$ = -30V, $V_{\mbox{\scriptsize GS}}$ = -10V

Typical Characteristics T_J = 25°C unless otherwise noted

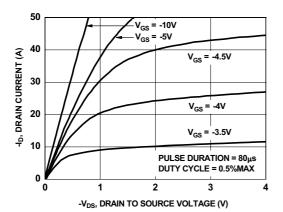


Figure 1. On-Region Characteristics

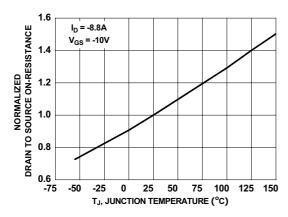


Figure 3. Normalized On-Resistance vs Junction Temperature

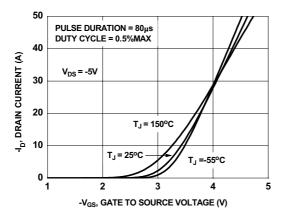


Figure 5. Transfer Characteristics

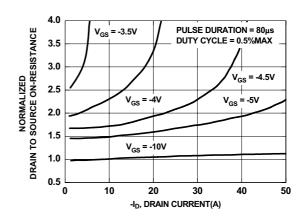


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

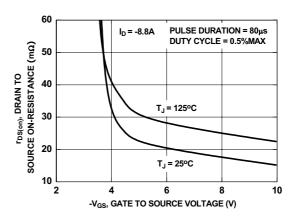


Figure 4. On-Resistance vs Gate to Source Voltage

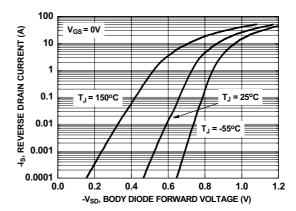


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

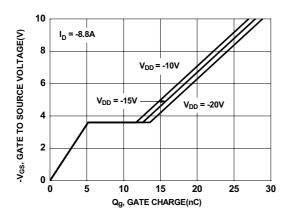


Figure 7. Gate Charge Characteristics

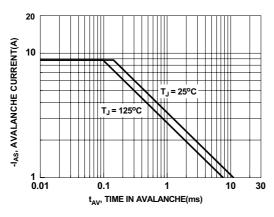


Figure 9. Unclamped Inductive Switching Capability

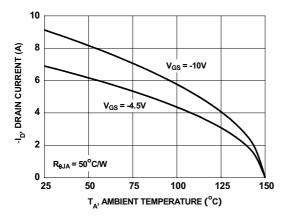


Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

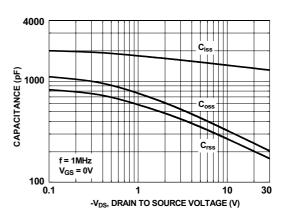


Figure 8. Capacitance vs Drain to Source Voltage

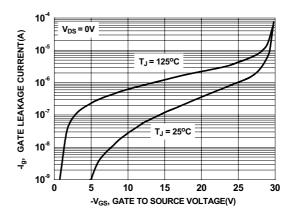


Figure 10. Gate Leakage Current vs Gate to Source Voltage

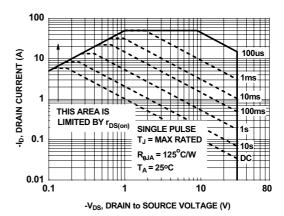


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

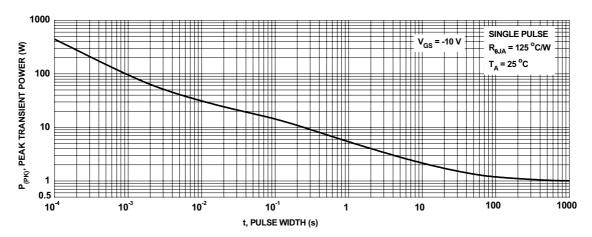


Figure 13. Single Pulse Maximum Power Dissipation

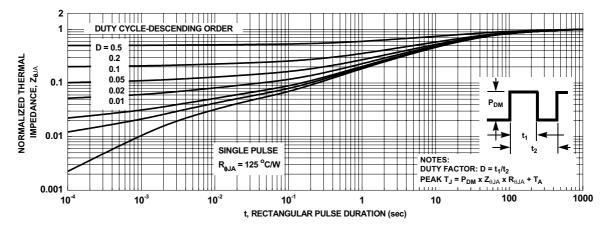


Figure 14. Transient Thermal Response Curve





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