NTTFS4840N

Power MOSFET
30 V, 26 A, Single N−Channel, μ8FL

Features
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications
- DC−DC Converters
- Point of Load
- Power Load Switch
- Notebook Battery Management
- Motor Control

ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	24 mΩ @ 10 V	26 A
	36 mΩ @ 4.5 V	

N−Channel MOSFET

D (5−8)
G (4)
S (1,2,3)

WDFN8 (μ8FL) CASE 511AB

MARKING DIAGRAM

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1
S ┃   ┃ D
S ┃4840┃ D
S ┃AYWW■┃ D
G ┃   ┃ D
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4840 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb−Free Package

(Note: Microdot may be in either location)

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{θJA}$ (Note 1)	Steady State	T_A = 25°C	I_D	7.3	A
		T_A = 85°C		5.3	
Power Dissipation $R_{θJA}$ (Note 1)		T_A = 25°C	P_D	2.2	W
Continuous Drain Current $R_{θJA}$ ≤ 10 s (Note 1)		T_A = 25°C	I_D	10.3	A
		T_A = 85°C		7.5	
Power Dissipation $R_{θJA}$ ≤ 10 s (Note 1)		T_A = 25°C	P_D	4.4	W
Continuous Drain Current $R_{θJA}$ (Note 2)		T_A = 25°C	I_D	4.6	A
		T_A = 85°C		3.3	
Power Dissipation $R_{θJA}$ (Note 2)		T_A = 25°C	P_D	0.84	W
Continuous Drain Current $R_{θJC}$ (Note 1)		T_C = 25°C	I_D	26	A
		T_C = 85°C		19	
Power Dissipation $R_{θJC}$ (Note 1)		T_C = 25°C	P_D	27.8	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	77	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to +150	°C
Source Current (Body Diode)			I_S	23	A
Drain to Source dV/dt			dV/dt	6.0	V/ns
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, V_{DD} = 50 V, V_{GS} = 10 V, I_L = 18.3 A_{pk}, L = 0.1 mH, R_G = 25 Ω)			E_{AS}	16.7	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
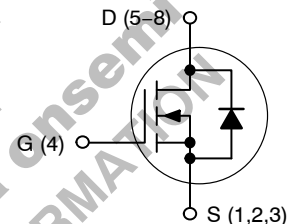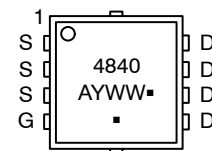2. Surface−mounted on FR4 board using the minimum recommended pad size.

ORDERING INFORMATION

Device	Package	Shipping†
NTTFS4840NTAG	WDFN8 (Pb−Free)	1500/Tape & Reel
NTTFS4840NTWG	WDFN8 (Pb−Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	4.5	°C/W
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	57.5	
Junction−to−Ambient − Steady State (Note 4)	$R_{\theta JA}$	149.2	
Junction−to−Ambient − (t ≤ 10 s) (Note 3)	$R_{\theta JA}$	28.7	

3. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
4. Surface−mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				17		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5		3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.6		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V to 11.5 V	I_D = 20 A		15	24	mΩ
			I_D = 10 A		15		
		V_{GS} = 4.5 V	I_D = 20 A		28	36	
			I_D = 10 A		25		
Forward Transconductance	g_{FS}	V_{DS} = 1.5 V, I_D = 20 A			22		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 15 V			580		pF
Output Capacitance	C_{oss}				140		
Reverse Transfer Capacitance	C_{rss}				80		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 20 A			5.5		nC
Threshold Gate Charge	$Q_{G(TH)}$				0.75		
Gate−to−Source Charge	Q_{GS}				2.2		
Gate−to−Drain Charge	Q_{GD}				2.8		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 20 A			10.8		nC
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			10.5		ns
Rise Time	t_r				38.2		
Turn−Off Delay Time	$t_{d(off)}$				11.5		
Fall Time	t_f				2.6		

5. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			6.3		ns
Rise Time	t_r				19.4		
Turn−Off Delay Time	$t_{d(off)}$				15.8		
Fall Time	t_f				1.7		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 20 A	T_J = 25°C		0.96	1.2	V
			T_J = 125°C		0.87		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 20 A			12.5		ns
Charge Time	t_a				7.7		
Discharge Time	t_b				4.8		
Reverse Recovery Charge	Q_{RR}				4.4		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	T_A = 25°C			0.66		nH
Drain Inductance	L_D				0.20		
Gate Inductance	L_G				1.5		
Gate Resistance	R_G				2.0	3.0	Ω

5. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS
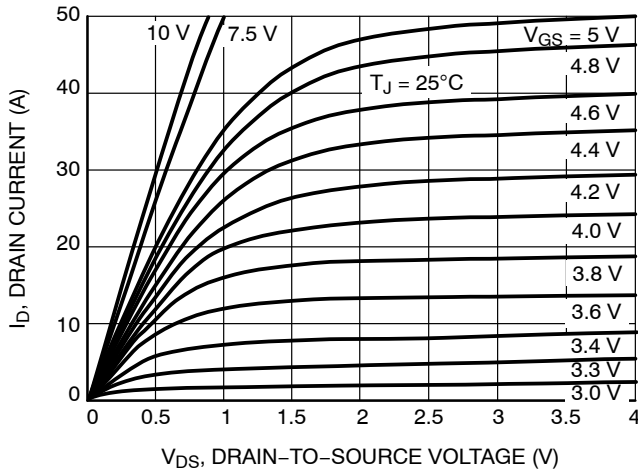
Figure 1. On−Region Characteristics
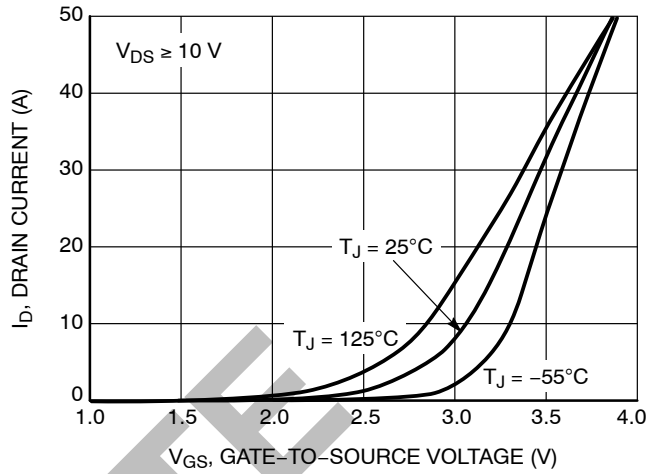
Figure 2. Transfer Characteristics
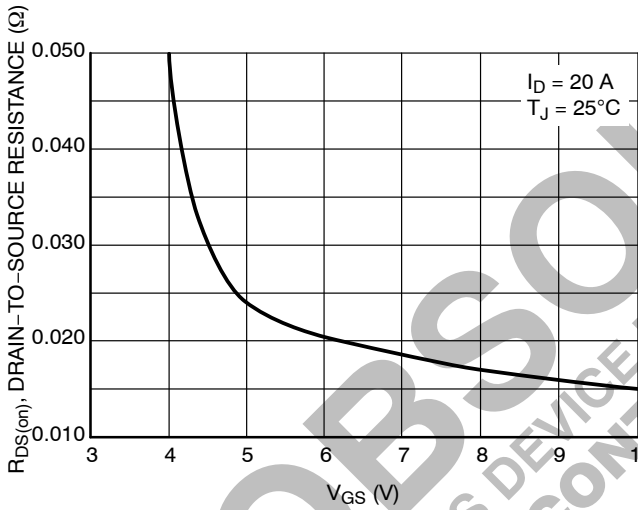
Figure 3. On−Resistance vs. V$_{GS}$
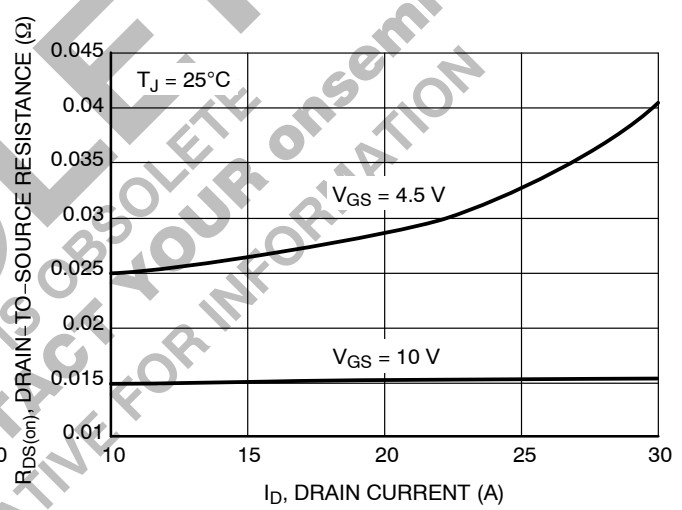
Figure 4. On−Resistance vs. Drain Current and Gate Voltage
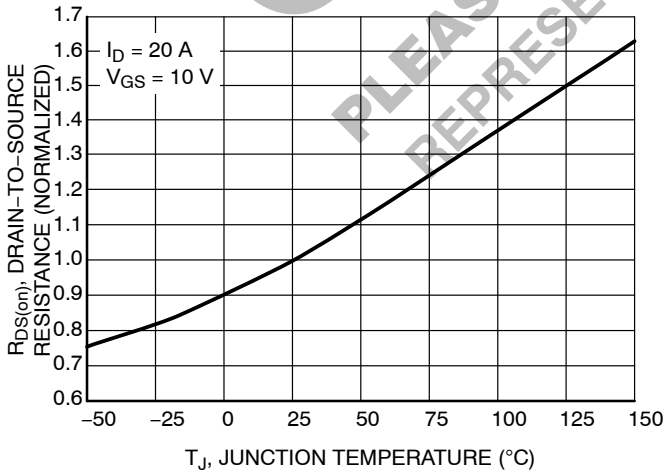
Figure 5. On−Resistance Variation with Temperature
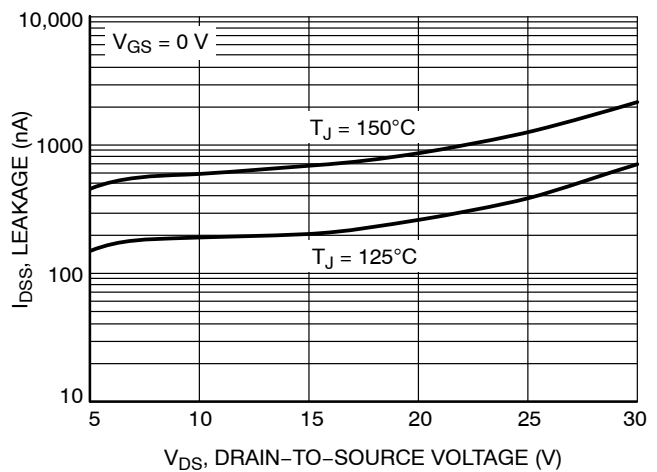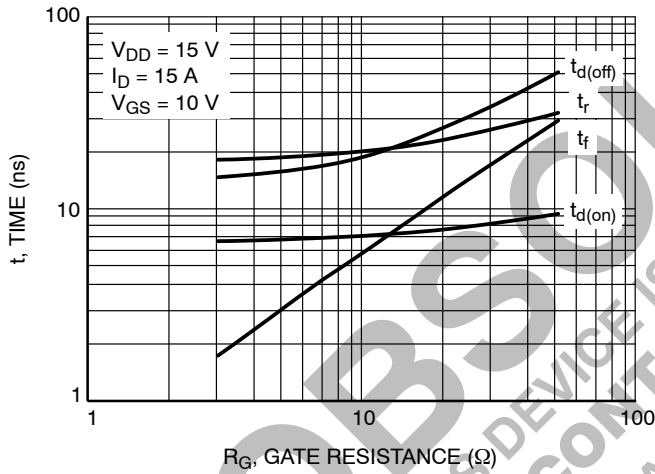

Figure 6. Drain−to−Source Leakage Current vs. Voltage

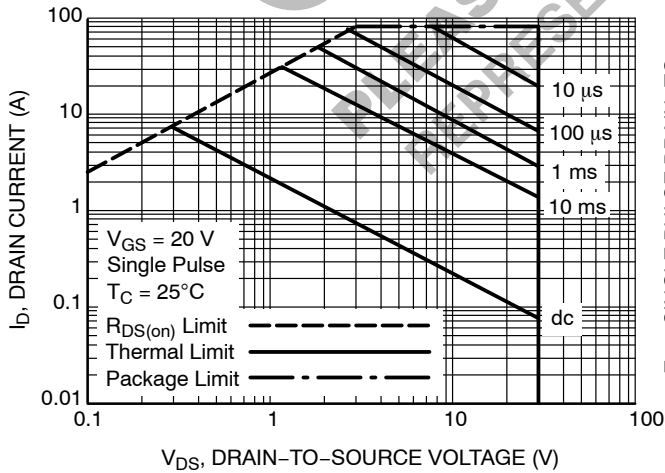## TYPICAL CHARACTERISTICS
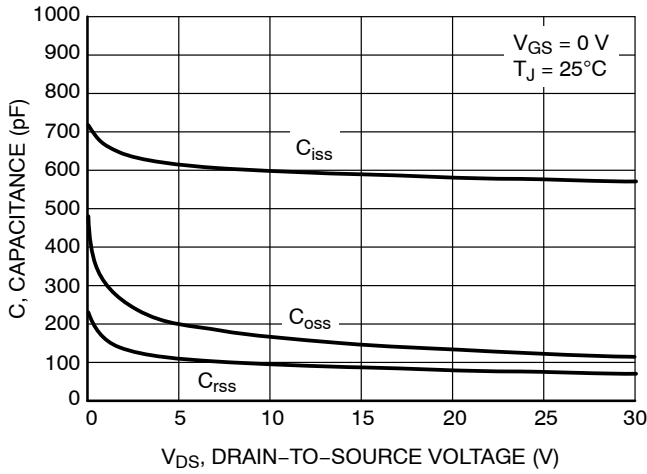
Figure 7. Capacitance Variation
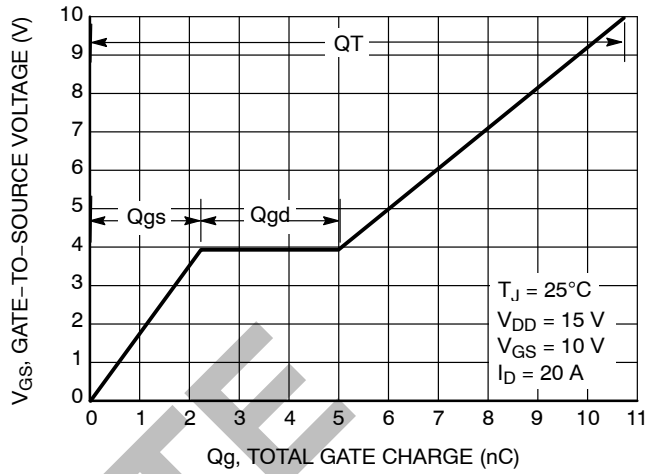
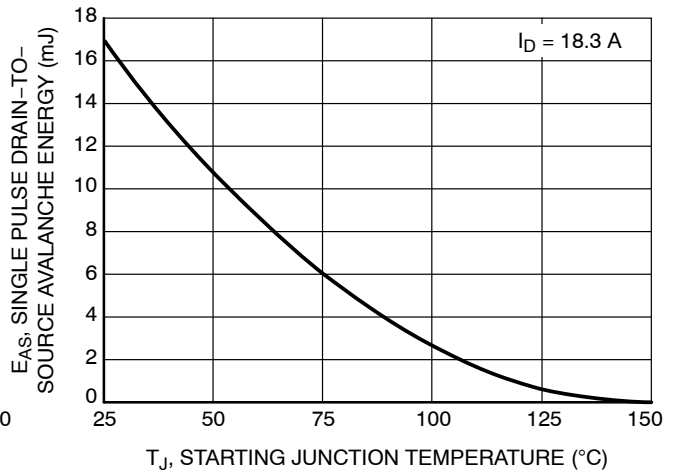**Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

Figure 9. Resistive Switching Time Variation vs. Gate Resistance
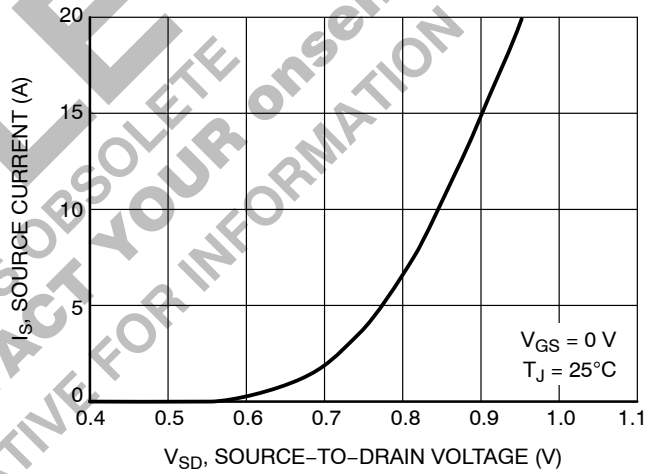
Figure 10. Diode Forward Voltage vs. Current

Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS

Figure 13. Thermal Response

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PACKAGE DIMENSIONS

WDFN8 3.3x3.3, 0.65P
CASE 511AB−01
ISSUE B

TOP VIEW

SIDE VIEW — **DETAIL A**

DETAIL A

BOTTOM VIEW
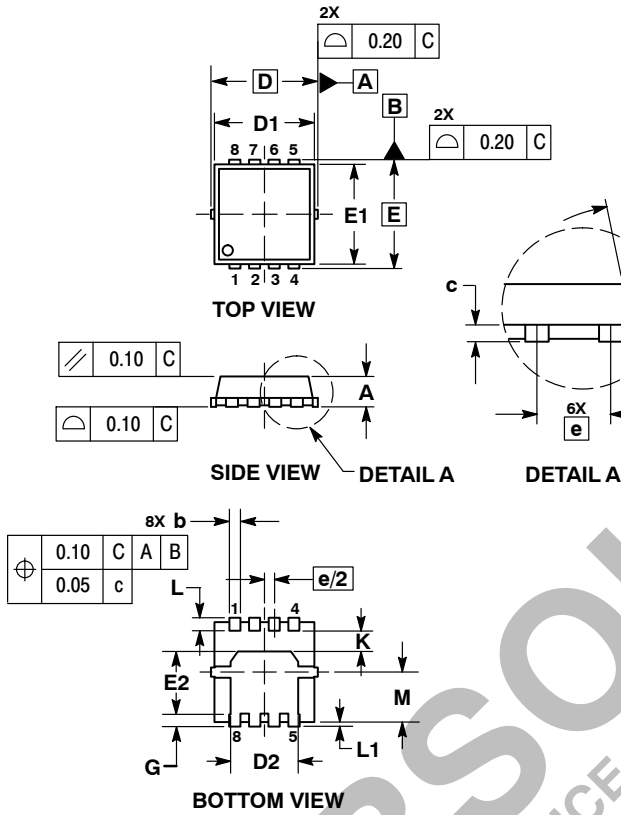
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.64	---	---	0.025	---	---
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °

SOLDERING FOOTPRINT*

PACKAGE OUTLINE
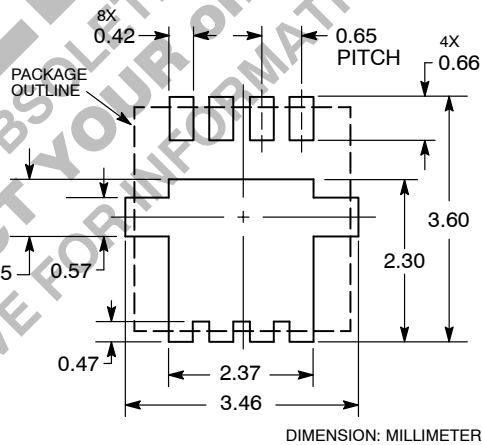
DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTTFS4840N/D

单击下面可查看定价，库存，交付和生命周期等信息

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