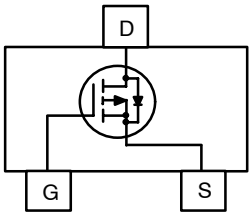
# MOSFET – P-Channel, Logic Level, POWERTRENCH®

## 60 V

# FDN5618P

SOT−23−3
CASE 527AG




### General Description

This 60 V P−Channel MOSFET uses **onsemi**'s high voltage POWERTRENCH process. It has been optimized for power management applications.

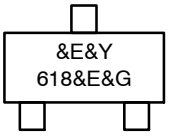
### Features

- −1.25 A, −60 V
  - $R_{DS(on)}$ = 0.170 Ω @ $V_{GS}$ = −10 V
  - $R_{DS(on)}$ = 0.230 Ω @ $V_{GS}$ = −4.5 V
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- This Device is Pb−Free and Halogen Free

### Applications

- DC−DC Converters
- Load Switch
- Power Management

### MARKING DIAGRAM




&E = Designates Space
&Y = Binary Calendar Year Coding Scheme
618 = Specific Device Code
&G = Date Code

### ABSOLUTE MAXIMUM RATINGS $T_A$ = 25°C unless otherwise noted.

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{DSS}$ | Drain−Source Voltage | −60 | V |
| $V_{GSS}$ | Gate−Source Voltage | ±20 | V |
| $I_D$ | Drain Current − Continuous (Note 1a) | −1.25 | A |
| | Drain Current − Pulsed | −10 | |
| $P_D$ | Maximum Power Dissipation (Note 1a) | 0.5 | W |
| | Maximum Power Dissipation (Note 1b) | 0.46 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient (Note 1a) | 250 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction−to−Case (Note 1) | 75 | °C/W |

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDN5618P | SOT−23−3 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** $T_A$ = 25°C unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = −250 μA | −60 | – | – | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = −250 μA, Referenced to 25°C | – | −58 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = −48 V, $V_{GS}$ = 0 V | – | – | −1 | μA |
| $I_{GSSF}$ | Gate–Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | – | – | 100 | nA |
| $I_{GSSR}$ | Gate–Body Leakage, Reverse | $V_{GS}$ = −20 V, $V_{DS}$ = 0 V | – | – | −100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = −250 μA | −1 | −1.6 | −3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = −250 μA, Referenced to 25°C | – | 4 | – | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = −10 V, $I_D$ = −1.25 A | – | 0.148 | 0.170 | Ω |
| | | $V_{GS}$ = −4.5 V, $I_D$ = −1.0 A | – | 0.185 | 0.230 | |
| | | $V_{GS}$ = −10 V, $I_D$ = −3 A, $T_J$ = 125°C | – | 0.245 | 0.315 | |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = −10 V, $V_{DS}$ = −5 V | −5 | – | – | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = −5 V, $I_D$ = −1.25 A | – | 4.3 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = −30 V, $V_{GS}$ = 0 V, f = 1.0 MHz | – | 430 | – | pF |
| $C_{oss}$ | Output Capacitance | | – | 52 | – | |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 19 | – | |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = −30 V, $I_D$ = −1 A, $V_{GS}$ = −10 V, $R_{GEN}$ = 6 Ω | – | 6.5 | 13 | ns |
| $t_r$ | Turn–On Rise Time | | – | 8 | 16 | |
| $t_{d(off)}$ | Turn–Off Delay Time | | – | 16.5 | 30 | |
| $t_f$ | Turn–Off Fall Time | | – | 4 | 8 | |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = −30 V, $I_D$ = −1.25 A, $V_{GS}$ = −10 V | – | 8.6 | 13.8 | nC |
| $Q_{gs}$ | Gate–Source Charge | | – | 1.5 | – | |
| $Q_{gd}$ | Gate–Drain Charge | | – | 1.3 | – | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | – | – | −0.42 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = −0.42 A (Note 2) | – | −0.7 | −1.2 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

a) 250°C/W when mounted on a 0.02 $in^2$ pad of 2 oz. copper.

b) 270°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

## TYPICAL CHARACTERISTICS

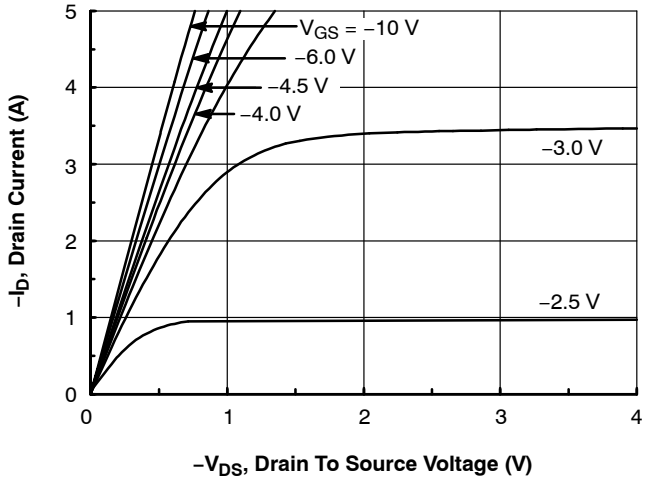



Figure 1. On−Region Characteristics

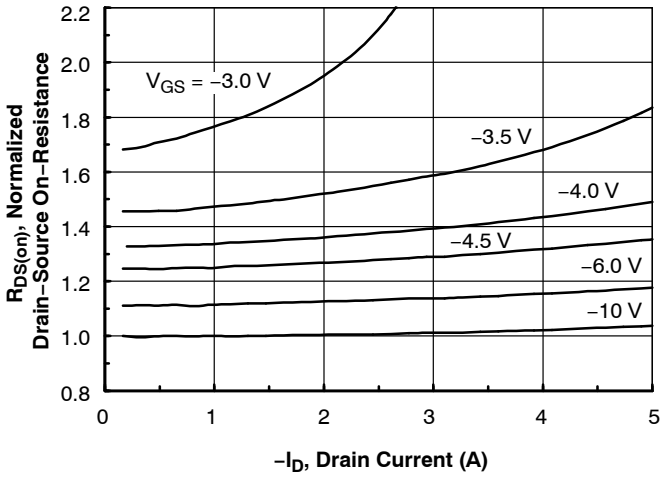



Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

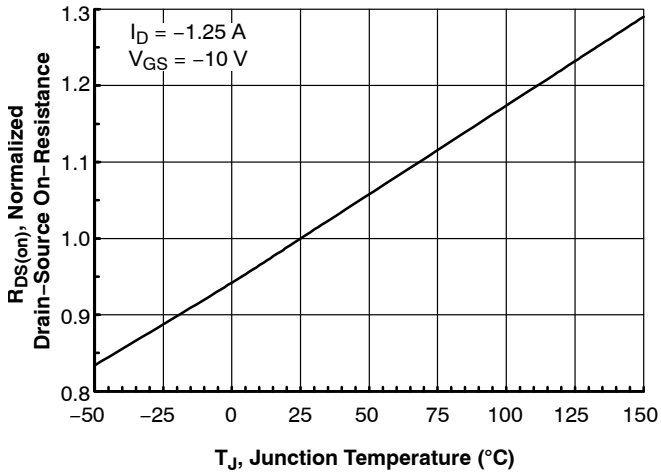



Figure 3. On−Resistance Variation with Temperature

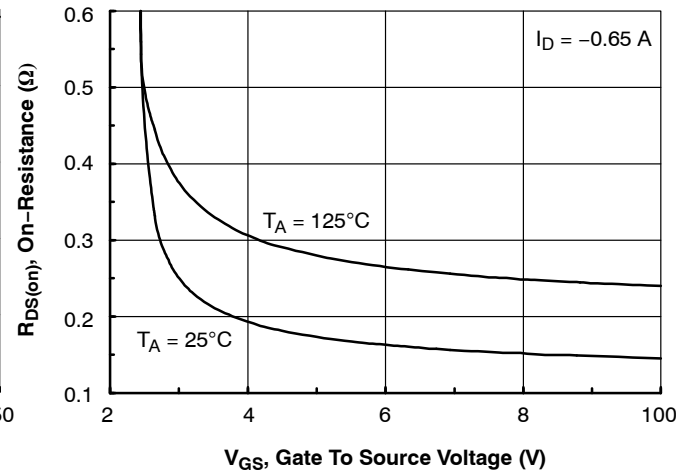



Figure 4. On−Resistance Variation with Gate−to−Source Voltage

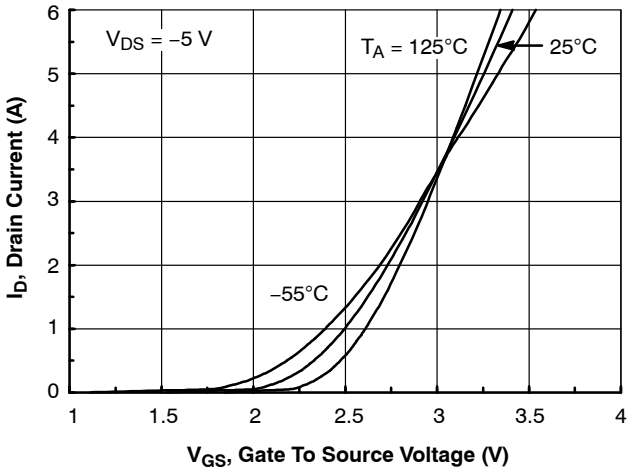



Figure 5. Transfer Characteristics

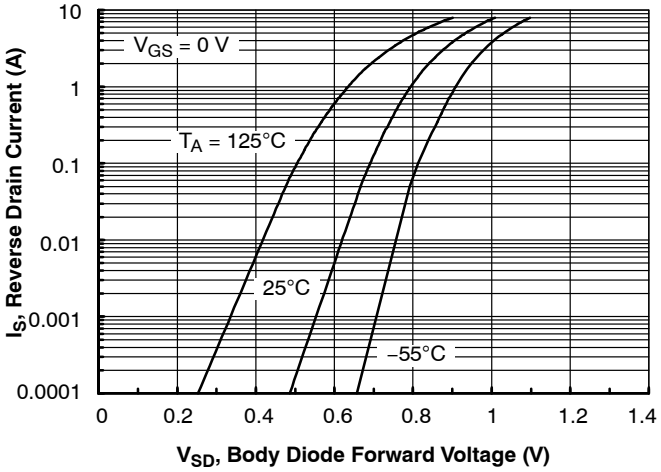



Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

## TYPICAL CHARACTERISTICS (CONTINUED)

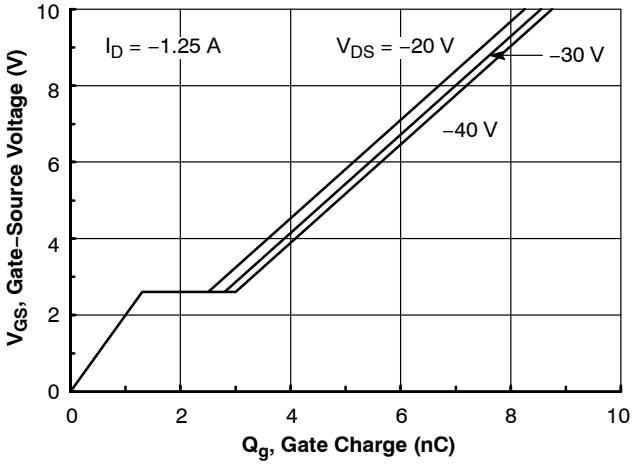



**Figure 7. Gate Charge Characteristics**

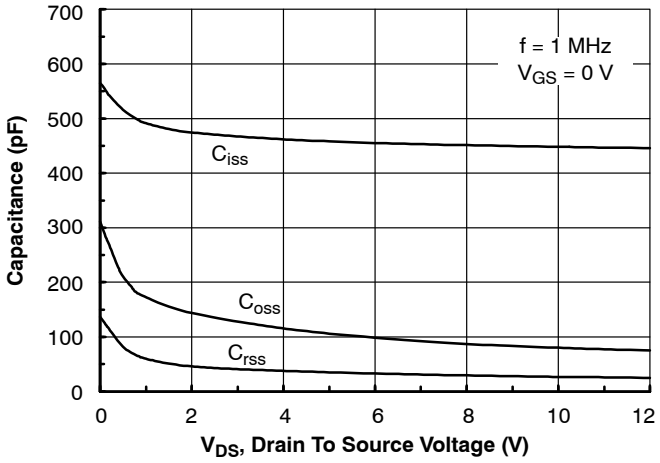



**Figure 8. Capacitance Characteristics**

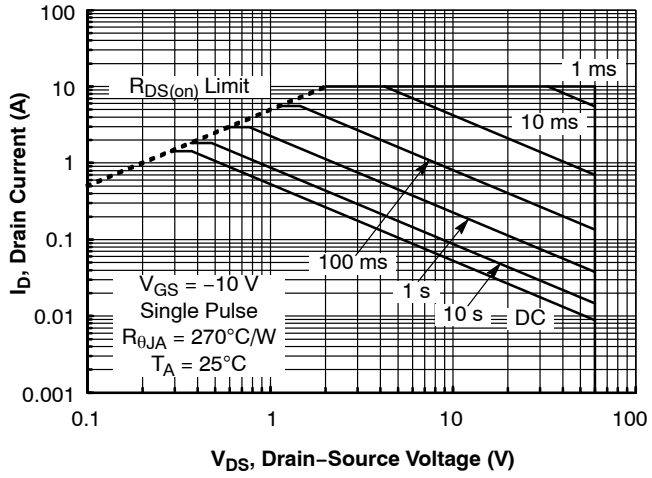



**Figure 9. Maximum Safe Operating Area**

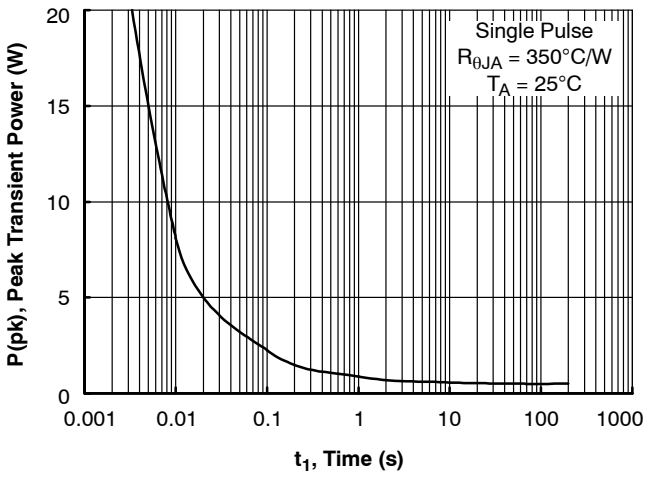



**Figure 10. Single Pulse Maximum Power Dissipation**

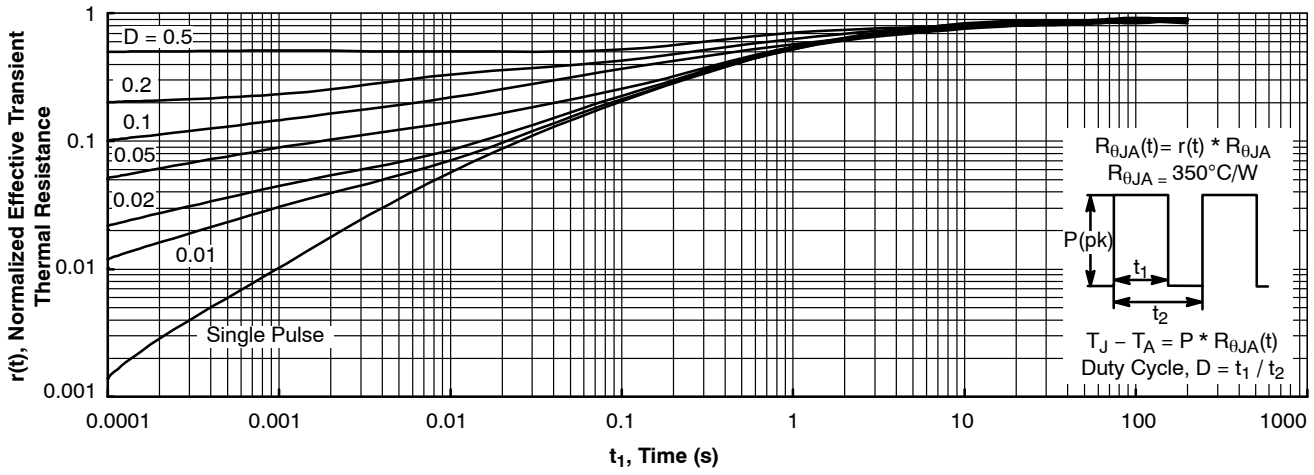
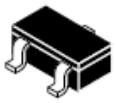



**Figure 11. Transient Thermal Response Curve**

Thermal characterization performed using the conditions described in Note 1a.
Transient thermal response will change depending on the circuit board design.

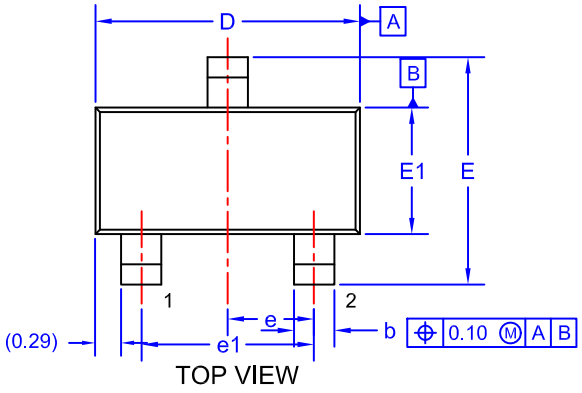
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®



**SOT−23/SUPERSOT™ −23, 3 LEAD, 1.4x2.9**
CASE 527AG
ISSUE A

DATE 09 DEC 2019

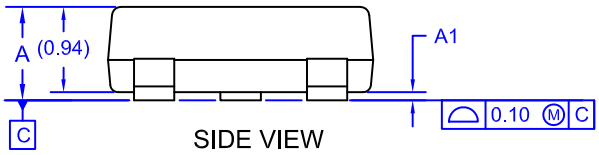


TOP VIEW

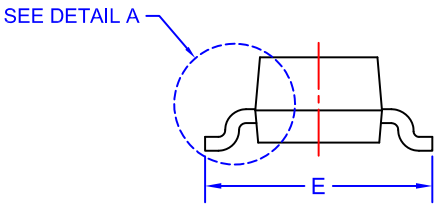
NOTES: UNLESS OTHERWISE SPECIFIED

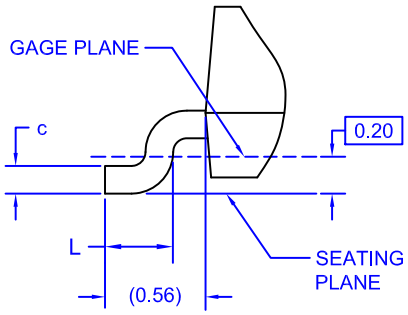
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

| DIM | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 0.85 | 0.95 | 1.12 |
| A1 | 0.00 | 0.05 | 0.10 |
| b | 0.370 | 0.435 | 0.508 |
| c | 0.085 | 0.150 | 0.180 |
| D | 2.80 | 2.92 | 3.04 |
| E | 2.31 | 2.51 | 2.71 |
| E1 | 1.20 | 1.40 | 1.52 |
| e | | 0.95 BSC | |
| e1 | | 1.90 BSC | |
| L | 0.33 | 0.38 | 0.43 |

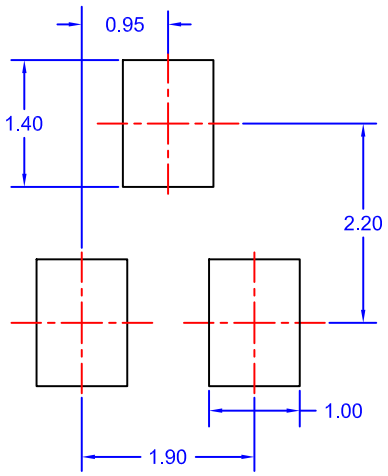


SIDE VIEW



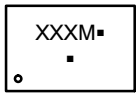
DETAIL A



LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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