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TinyLogic ULP-A Universal Configurable Logic Gates

NC7SP57, NC7SP58

The NC7SP57 and NC7SP58 are universal configurable logic gates in tiny footprint packages. The devices are designed to operate for V_{CC} = 0.9 V to 3.6 V.

Features

- Designed for 0.9 V to 3.6 V V_{CC} Operation
- 3.4 ns t_{PD} at 3.3 V (Typ)
- Inputs/Outputs Over−Voltage Tolerant up to 3.6 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 2.6 mA at 3.3 V
- Available in SC−88 and MicroPak™ Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

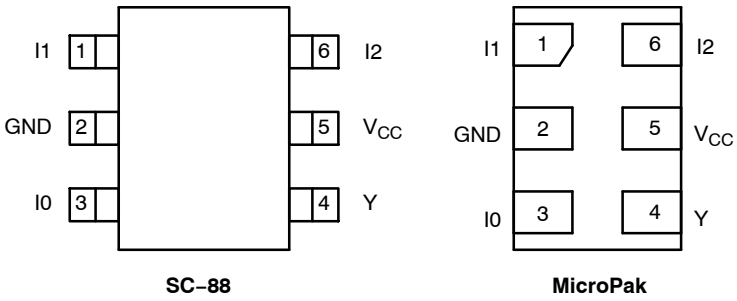

Figure 1. Pinout Diagrams (Top Views)

PIN ASSIGNMENT

Pin	SC−88	MicroPak
1	I1	I1
2	GND	GND
3	I0	I0
4	Y	Y
5	V_{CC}	V_{CC}
6	I2	I2

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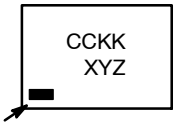
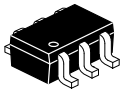
MARKING DIAGRAM

SIP6 1.45X1.0 MicroPak CASE 127EB

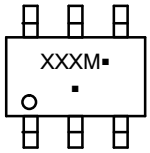


CC = Specific Device Code
KK = 2−Digit Lot Run Traceability Code
XY = 2−Digit Date Code
Z = Assembly Plant Code

MARKING DIAGRAM



SC−88 DF SUFFIX CASE 419B−02



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 9 of this data sheet.

FUNCTION TABLE

Inputs			NC7SP57	NC7SP58
I2	I1	I0	$Y = (\overline{I0}) \bullet (\overline{I2}) + (I1) \bullet (I2)$	$Y = (I0) \bullet (\overline{I2}) + (\overline{I1}) \bullet (I2)$
L	L	L	H	L
L	L	H	L	H
L	H	L	H	L
L	H	H	L	H
H	L	L	L	H
H	L	H	L	H
H	H	L	H	L
H	H	H	H	L

FUNCTION SELECTION TABLE

2−Input Logic Function	Device Selection	Connection Configuration
2−Input AND	NC7SP57	Figure 2
2−Input AND with inverted input	NC7SP58	Figure 8, 9
2−Input AND with both inputs inverted	NC7SP57	Figure 5
2−Input NAND	NC7SP58	Figure 7
2−Input NAND with inverted input	NC7SP57	Figure 3, 4
2−Input NAND with both inputs inverted	NC7SP58	Figure 10
2−Input OR	NC7SP58	Figure 10
2−Input OR with inverted input	NC7SP57	Figure 3, 4
2−Input OR with both inputs inverted	NC7SP58	Figure 7
2−Input NOR	NC7SP57	Figure 5
2−Input NOR with inverted input	NC7SP58	Figure 8, 9
2−Input NOR with both inputs inverted	NC7SP57	Figure 2
2−Input XOR	NC7SP58	Figure 11
2−Input XNOR	NC7SP57	Figure 6

Logic Configurations NC7SP57

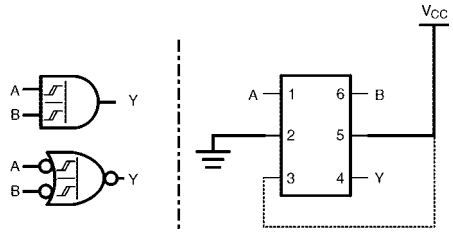


Figure 2. 2−Input AND Gate

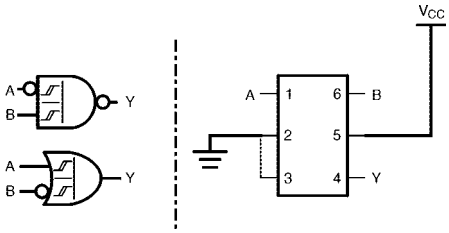


Figure 3. 2−Input NAND with Inverted A Input

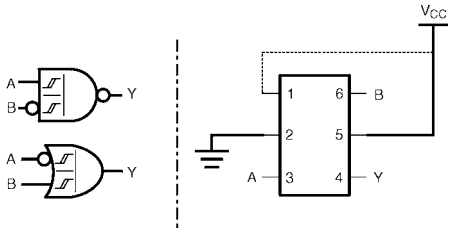


Figure 4. 2−Input NAND with Inverted B Input

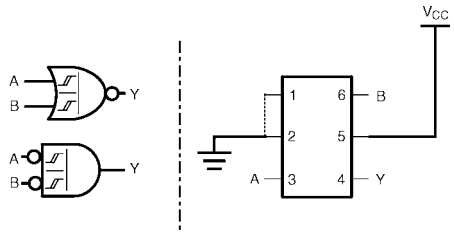


Figure 5. 2−Input NOR Gate

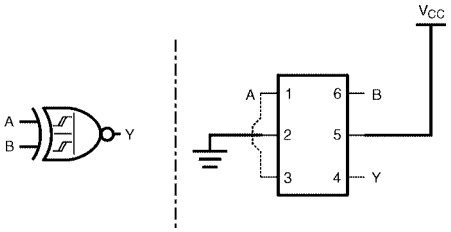


Figure 6. 2−Input XNOR Gate

NOTE: Figure 2 through Figure 6 show the logical functions that can be implemented using the NC7SP57. The diagrams show the DeMorgan's equivalent logic duals for a given 2−input function. Next to the logical implementation is the board level physical implementation of how the pins of the function should be connected.

Logic Configurations NC7SP58

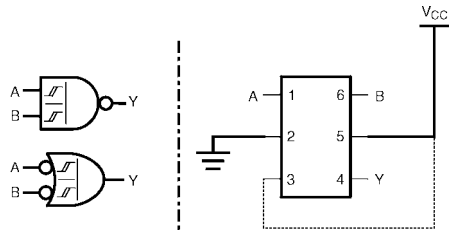


Figure 7. 2−Input NAND Gate

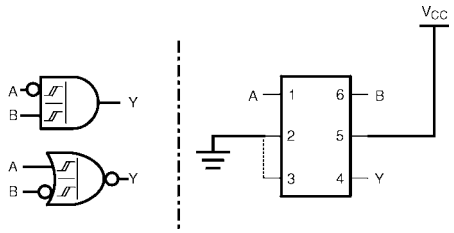


Figure 8. 2−Input AND with Inverted A Input

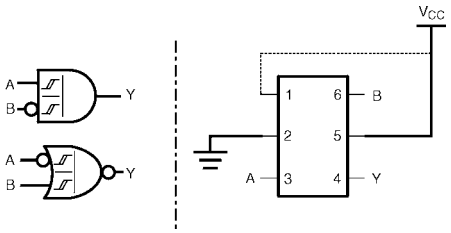


Figure 9. 2−Input AND with Inverted B Input

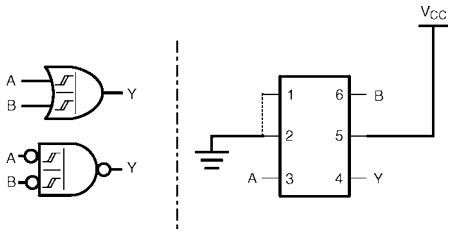


Figure 10. 2−Input OR Gate

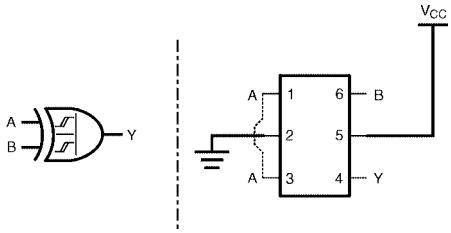


Figure 11. 2−Input XOR Gate

NOTE: Figure 7 through Figure 11 show the logical functions that can be implemented using the NC7SP58. The diagrams show the DeMorgan's equivalent logic duals for a given 2−input function. Next to the logical implementation is the board level physical implementation of how the pins of the function should be connected.

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +4.3	V
V_{IN}	DC Input Voltage		−0.5 to +4.3	V
V_{OUT}	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 11) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +4.3 −0.5 to +4.3	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−50	mA
I_{OUT}	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 12)	SC−88 MicroPak	377 154	°C/W
P_D	Power Dissipation in Still Air	SC−88 MicroPak	332 812	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		0.9	3.6	V
V_{IN}	DC Input Voltage		0	3.6	V
V_{OUT}	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 11) Power−Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 3.6 3.6	
T_A	Operating Temperature Range		−40	+85	°C
t_r , t_f	Input Transition Rise and Fall Time		0	No Limit	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_P	Positive Threshold Voltage		0.9	_	0.62	–	_	–	V
			1.1	_	–	1.0	_	1.0	
			1.4	_	–	1.2	_	1.2	
			1.65	_	–	1.5	_	1.5	
			3.0	–	–	1.9	–	1.9	
			3.0 to 3.6	–	–	2.6	–	2.6	
V_N	Negative Threshold Voltage		0.9	–	0.34	–	–	–	V
			1.1	0.15	–	_	0.15	_	
			1.4	0.2	–	_	0.2	_	
			1.65	0.25	–	_	0.25	_	
			2.3	0.4	–	–	0.4	–	
			3.0	0.6	–	–	0.6	–	
V_H	Hysteresis Voltage		0.9	–	0.29	–	–	–	V
			1.1	0.08	–	0.6	0.08	0.6	
			1.4	0.09	–	0.8	0.09	0.8	
			1.65	0.1	–	1.0	0.1	1.0	
			2.3	0.25	–	1.1	0.25	1.1	
			3.0	0.6	–	1.8	0.6	1.8	
V_{OH}	High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{OH} = −20 μA	0.9	–	V_{CC} − 0.1	–	–	–	
			1.1 to 1.3	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
			1.4 to 1.6	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
			1.65 to 1.95	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
			2.3 to 2.7	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
			3.0 to 3.6	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
		I_{OH} = −0.5 mA	1.1 to 1.3	0.75 x V_{CC}	–	–	0.70 x V_{CC}	–	
		I_{OH} = −1 mA	1.4 to 1.6	1.07	–	–	0.99	–	
		I_{OH} = −1.5 mA	1.65 to 1.95	1.24	–	–	1.22	–	
		I_{OH} = −2.1 mA	2.3 to 2.7	1.95	–	–	1.87	–	
		I_{OH} = −2.6 mA	3.0 to 3.6	2.61	–	–	2.55	–	
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{OL} = 20 μA	0.9	–	0.1	–	–	–	
			1.1 to 1.3	–	–	0.1	–	0.1	
			1.4 to 1.6	–	–	0.1	–	0.1	
			1.65 to 1.95	–	–	0.1	–	0.1	
			2.3 to 2.7	–	–	0.1	–	0.1	
			3.0 to 3.6	–	–	0.1	–	0.1	
		I_{OL} = 0.5 mA	1.1 to 1.3	–	–	0.3 x V_{CC}	–	0.3 x V_{CC}	
		I_{OL} = 1 mA	1.4 to 1.6	–	–	0.31	–	0.37	
		I_{OL} = 1.5 mA	1.65 to 1.95	–	–	0.31	–	0.35	
		I_{OL} = 2.1 mA	2.3 to 2.7	–	–	0.31	–	0.33	
		I_{OL} = 2.6 mA	3.0 to 3.6	–	–	0.31	–	0.33	

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
I_{IN}	Input Leakage Current	V_{IN} = 0 V to 3.6 V	0.9 to 3.6	–	–	±0.1	–	±0.5	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 0 V to 3.6 V or V_{OUT} = 0 V to 3.6 V	0	–	–	0.5	–	0.5	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	0.9 to 3.6	–	–	0.9	–	0.9	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

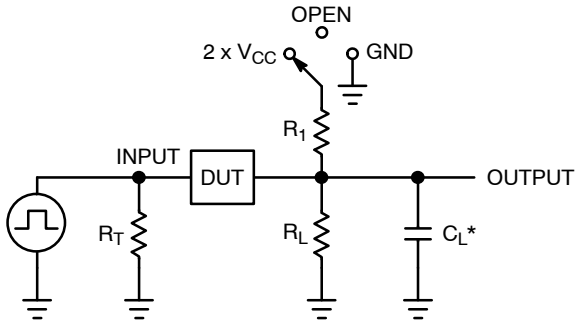
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, (I0 or I1 or I2) to Y (Figures 12 and 13)	R_L = 1 MΩ, C_L = 10 pF	0.9	–	54.3	–	–	–	ns
			1.10 to 1.30	–	15.1	30.8	–	51.0	
			1.40 to 1.60	–	8.2	17.0	–	21.0	
			1.65 to 1.95	–	5.9	14.0	–	17.0	
			2.3 to 2.7	–	4.0	10.0	–	13.0	
			3.0 to 3.6	–	3.4	8.0	–	12.0	
t_{PLH}, t_{PHL}	Propagation Delay, (I0 or I1 or I2) to Y (Figures 12 and 13)	R_L = 1 MΩ, C_L = 15 pF	0.9	–	55.8	–	–	–	ns
			1.10 to 1.30	–	15.6	32.1	–	52.0	
			1.40 to 1.60	–	8.6	18.0	–	22.0	
			1.65 to 1.95	–	6.3	15.0	–	18.0	
			2.3 to 2.7	–	4.2	11.0	–	14.0	
			3.0 to 3.6	–	3.6	9.0	–	12.0	
t_{PLH}, t_{PHL}	Propagation Delay, (I0 or I1 or I2) to Y (Figures 12 and 13)	R_L = 1 MΩ, C_L = 30 pF	0.9	–	60.2	–	–	–	ns
			1.10 to 1.30	–	17.2	33.6	–	55.0	
			1.40 to 1.60	–	9.9	20.0	–	24.0	
			1.65 to 1.95	–	7.4	17.0	–	20.0	
			2.3 to 2.7	–	5.0	12.0	–	15.0	
			3.0 to 3.6	–	4.1	11.0	–	14.0	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Typical (T_A = 25°C)	Unit
C_{IN}	Input Capacitance	V_{CC} = 0 V	2.0	pF
C_{OUT}	Output Capacitance	V_{CC} = 0 V	4.0	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	f = 10 MHz, V_{CC} = 0.9 to 3.6 V, V_{IN} = 0 V or V_{CC}	8.0	pF

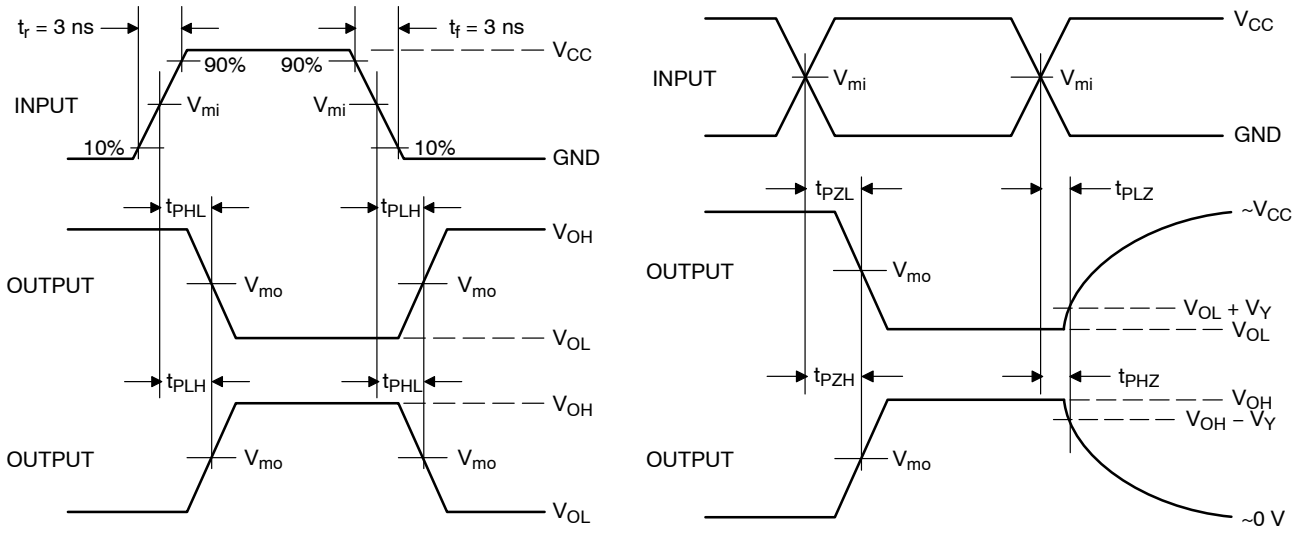
5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.



C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	2 x V_{CC}
t_{PHZ} / t_{PZH}	GND

Figure 12. Test Circuit



V_{CC}, V	V_{mi}, V	V_{mo}, V	V_Y, V
0.9	V_{CC} / 2	V_{CC} / 2	0.1
1.1 to 1.3	V_{CC} / 2	V_{CC} / 2	0.1
1.4 to 1.6	V_{CC} / 2	V_{CC} / 2	0.1
1.65 to 1.95	V_{CC} / 2	V_{CC} / 2	0.15
2.3 to 2.7	V_{CC} / 2	V_{CC} / 2	0.15
3.0 to 3.6	1.5	1.5	0.3

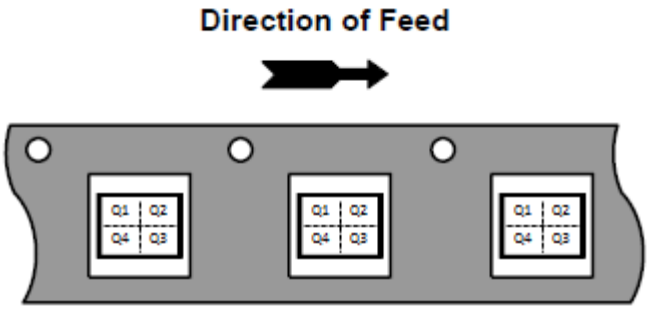
Figure 13. Switching Waveforms

ORDERING INFORMATION

Device	Package	Marking	Pin 1 Orientation (See below)	Shipping†
NC7SP57P6X	SC−88	P57	Q4	3000 / Tape & Reel
NC7SP57L6X	MicroPak	K9	Q4	5000 / Tape & Reel
NC7SP58P6X	SC−88	P58	Q4	3000 / Tape & Reel
NC7SP58L6X	MicroPak	L3	Q4	5000 / Tape & Reel

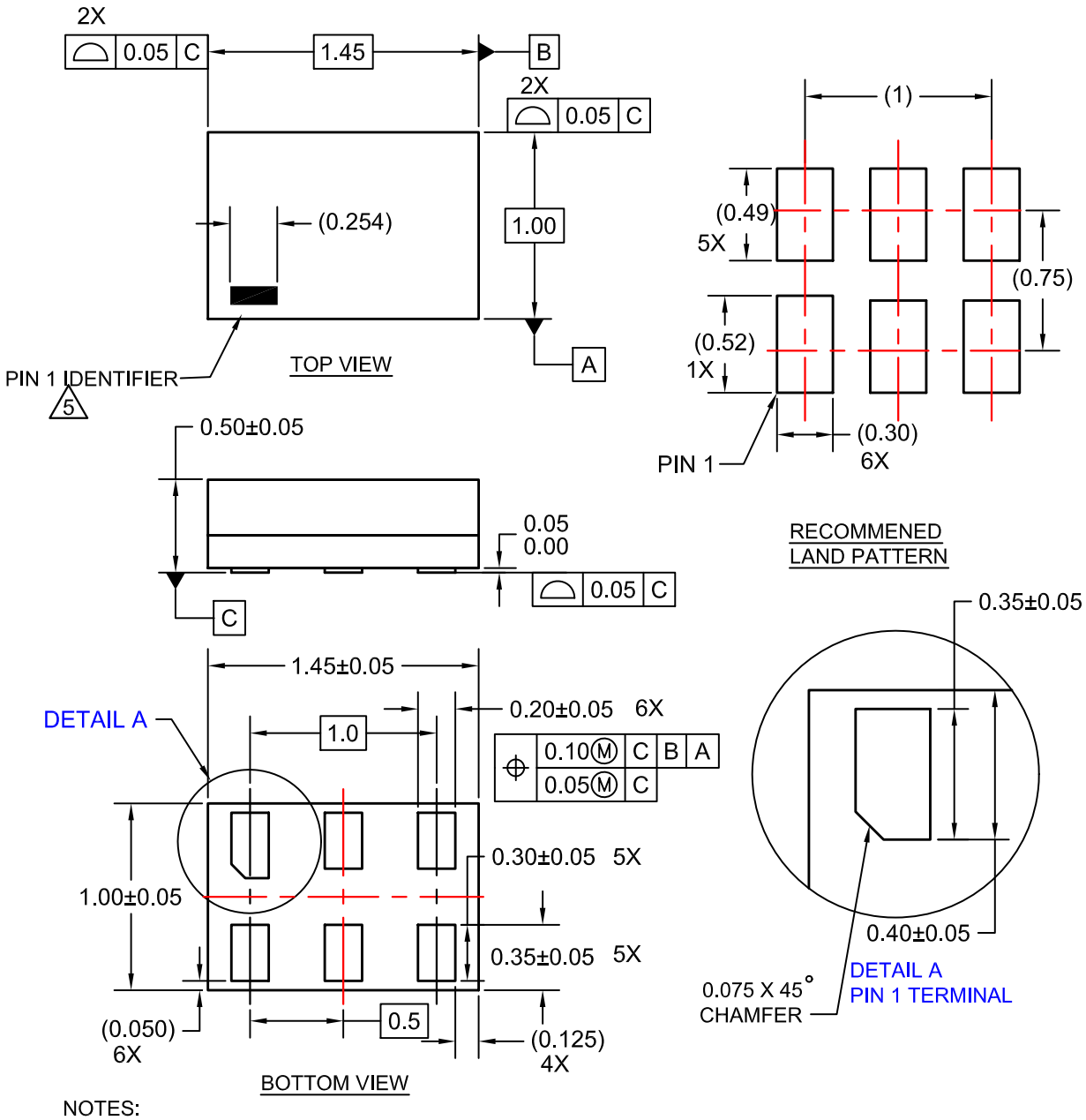
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Pin 1 Orientation in Tape and Reel



PACKAGE DIMENSIONS

SIP6 1.45X1.0
CASE 127EB
ISSUE O

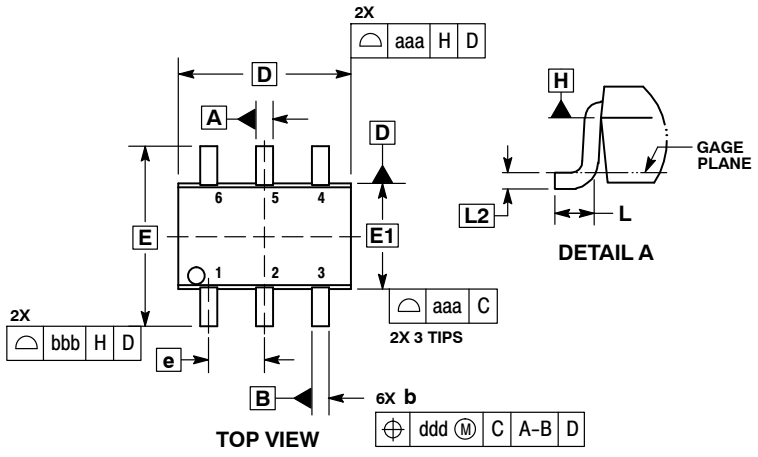


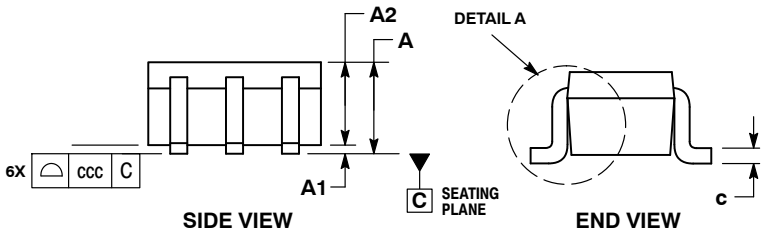
NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

PACKAGE DIMENSIONS

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

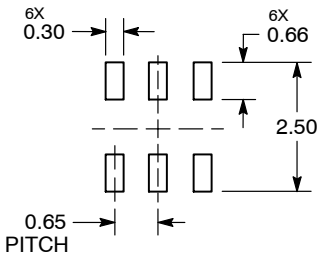




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

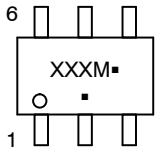
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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