MC74HCT244A

Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver with LSTTL-Compatible Inputs

High−Performance Silicon−Gate CMOS

The MC74HCT244A is identical in pinout to the LS244. This device may be used as a level converter for interfacing TTL or NMOS outputs to High−Speed CMOS inputs. The HCT244A is an octal noninverting buffer line driver line receiver designed to be used with 3−state memory address drivers, clock drivers, and other bus−oriented systems. The device has non−inverted outputs and two active−low output enables.

The HCT244A is the non−inverting version of the HCT240. See also HCT241.

Features

- Output Drive Capability: 15 LSTTL Loads
- TTL NMOS−Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 112 FETs or 28 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
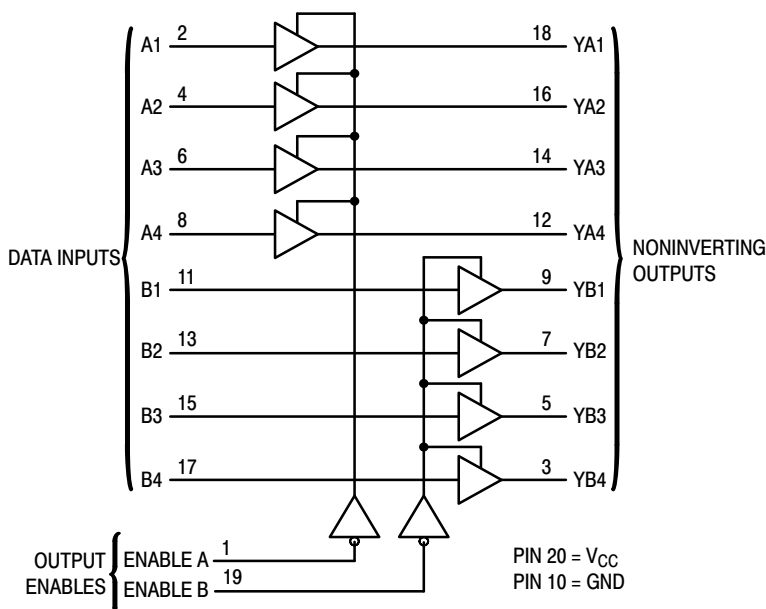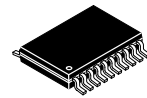- These Devices are Pb−Free and are RoHS Compliant

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SOIC−20W
DW SUFFIX
CASE 751D

TSSOP−20
DT SUFFIX
CASE 948E

PIN ASSIGNMENT

ENABLE A	1	20	V_{CC}
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

MARKING DIAGRAMS

HCT244A
AWLYYWWG

SOIC−20W

HCT
244A
ALYW■
■

TSSOP−20
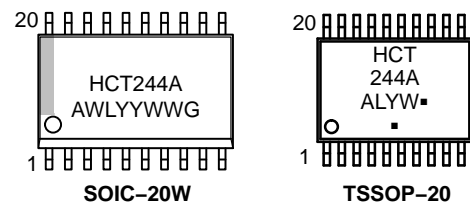
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ■	= Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = high impedance, X = don't care

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

Figure 1. Logic Diagram

DATA INPUTS: A1 (2) → YA1 (18), A2 (4) → YA2 (16), A3 (6) → YA3 (14), A4 (8) → YA4 (12), B1 (11) → YB1 (9), B2 (13) → YB2 (7), B3 (15) → YB3 (5), B4 (17) → YB4 (3)

NONINVERTING OUTPUTS

OUTPUT ENABLES: ENABLE A (1), ENABLE B (19)

PIN 20 = V_{CC}
PIN 10 = GND

MC74HCT244A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq$ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
†Derating: SOIC Package: –7 mW/°C from 65° to 125°C
            TSSOP Package: –6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 2)	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit –55 to 25°C	Guaranteed Limit $\leq$ 85°C	Guaranteed Limit $\leq$ 125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $|I_{out}| \leq$ 20 μA	4.5 5.5	2 2	2 2	2 2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $|I_{out}| \leq$ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $|I_{out}| \leq$ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $|I_{out}| \leq$ 6 mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $|I_{out}| \leq$ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $|I_{out}| \leq$ 6 mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State V_{in} = V_{IL} or V_{IH}; V_{out} = V_{CC} or GND	5.5	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4	40	160	μA

Symbol	Parameter	Test Conditions		$\geq$ –55°C	25°C to 125°C	
ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA	5.5	2.9	2.4	mA

1. Total Supply Current = I_{CC} + $\Sigma\Delta I_{CC}$.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±10%, C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		−55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 2 and 4)	20	25	30	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 3 and 5)	26	33	39	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 3 and 5)	22	28	33	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 4)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High−Impedance State)	15	15	15	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	55	pF

* Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

SWITCHING WAVEFORMS
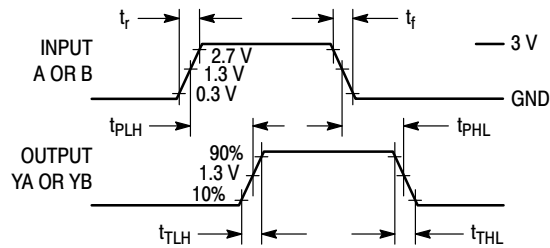
Figure 2.
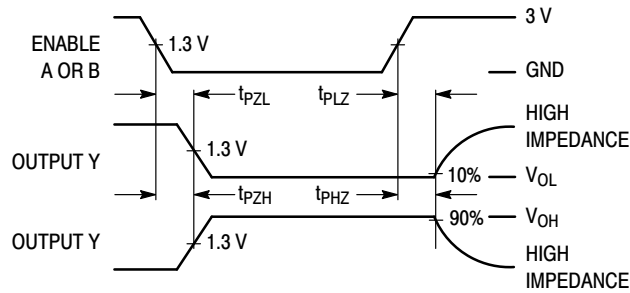
Figure 3.

MC74HCT244A

TEST CIRCUITS
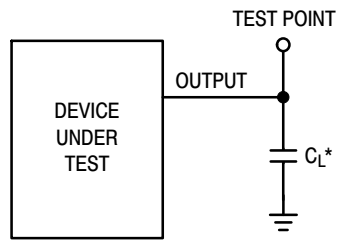
*Includes all probe and jig capacitance

Figure 4.

CONNECT TO V_{CC} WHEN TESTING t_{PLZ} AND t_{PZL}.
CONNECT TO GND WHEN TESTING t_{PHZ} AND t_{PZH}.
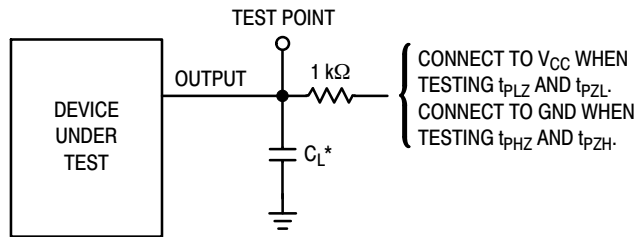
*Includes all probe and jig capacitance

Figure 5.

LOGIC DETAIL
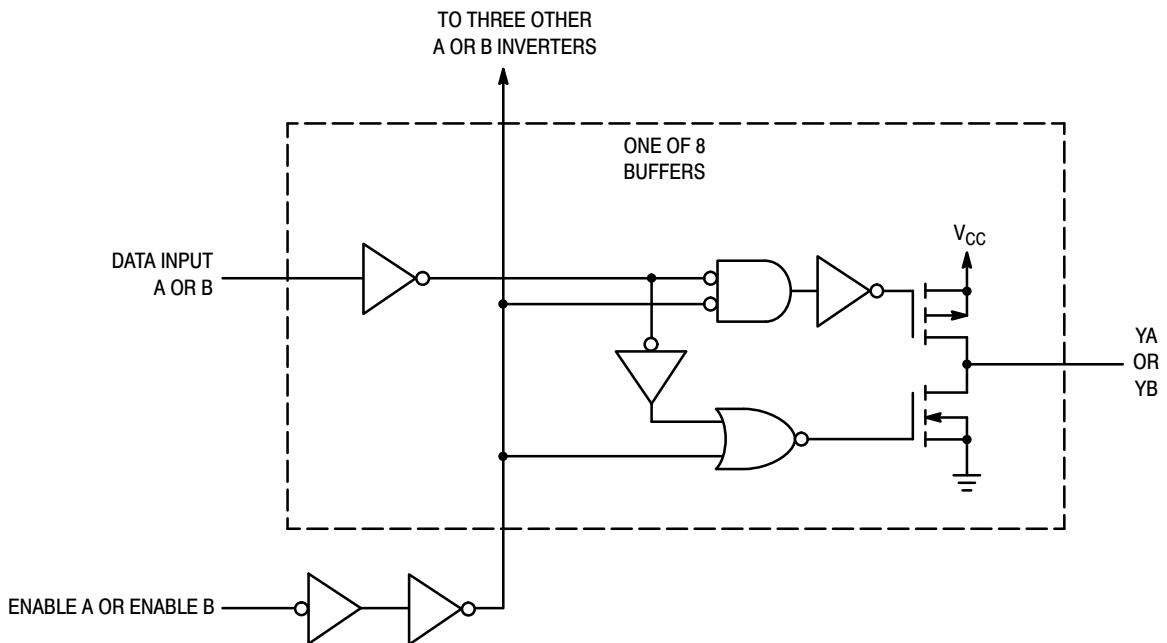
ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT244ADWG	SOIC−20 (Pb−Free)	38 Units / Rail
MC74HCT244ADWR2G	SOIC−20 (Pb−Free)	1000 / Tape & Reel
MC74HCT244ADTR2G	TSSOP−20 (Pb−Free)	2500 / Tape & Reel
NLVHCT244ADTR2G*	TSSOP−20 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

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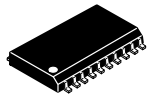
SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015

SCALE 1:1

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
---	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

RECOMMENDED SOLDERING FOOTPRINT*

20X 0.52

20X 1.30

11.00

1.27
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXXXXXXX
XXXXXXXXXX
AWLYYWWG
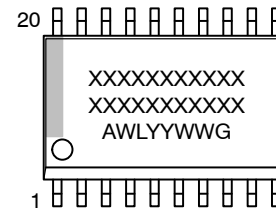
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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| DESCRIPTION: | SOIC−20 WB | | PAGE 1 OF 1 |

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TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

SCALE 2:1

20X **K** REF

⊕ | 0.15 (0.006) | T | U | Ⓢ

⊕ | 0.10 (0.004) Ⓜ | T | U | Ⓢ | V | Ⓢ

2X **L/2**

L

PIN 1 IDENT

20   11

10

B

−U−

⊕ | 0.15 (0.006) | T | U | Ⓢ

A

−V−

K

K1

J **J1**

SECTION N−N

N

0.25 (0.010)

M

N

F

DETAIL E

C

D **G** **H**

| 0.100 (0.004)

−T− **SEATING PLANE**

−W−

DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT

7.06

1

0.65 PITCH

16X 0.36

16X 1.26

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

XXXX
XXXX
ALYW■

■

○
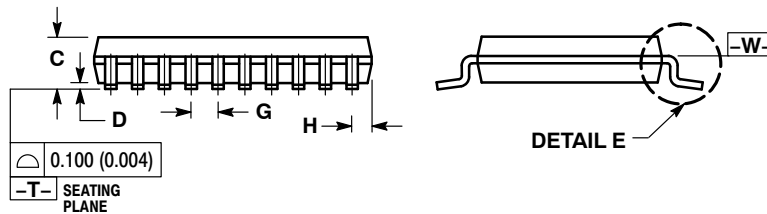
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ■", may or may not be present.

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DESCRIPTION:	TSSOP−20 WB		PAGE 1 OF 1

ADDITIONAL INFORMATION

◊

单击下面可查看定价，库存，交付和生命周期等信息

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