CS8182

Linear Voltage Tracking Regulator - Micropower Low Dropout, Line Driver

200 mA

The CS8182 is a monolithic integrated low dropout tracking regulator designed to provides an adjustable buffered output voltage that closely tracks (±10 mV) the reference input. The output delivers up to 200 mA while being able to be configured higher, lower or equal to the reference voltages.

The device has been designed to operate over a wide range (2.8 V to 45 V) while still maintaining excellent DC characteristics. The CS8182 is protected from reverse battery, short circuit and thermal runaway conditions. The device also can withstand 45 V load dump transients and −50 V reverse polarity input voltage transients. This makes it suitable for use in automotive environments.

The V_{REF}/ENABLE lead serves two purposes. It is used to provide the input voltage as a reference for the output and it also can be pulled low to place the device in sleep mode where it nominally draws 30 μA from the supply.

Features

- 200 mA Source Capability
- Output Tracks within ±10 mV Worst Case
- Low Dropout (0.35 V Typ. @ 200 mA)
- Low Quiescent Current
- Thermal Shutdown
- Short Circuit Protection
- Wide Operating Range
- Internally Fused Leads in SO−8 Package
- For Automotive and Other Applications Requiring Site and Change Control
- These are Pb−Free Devices

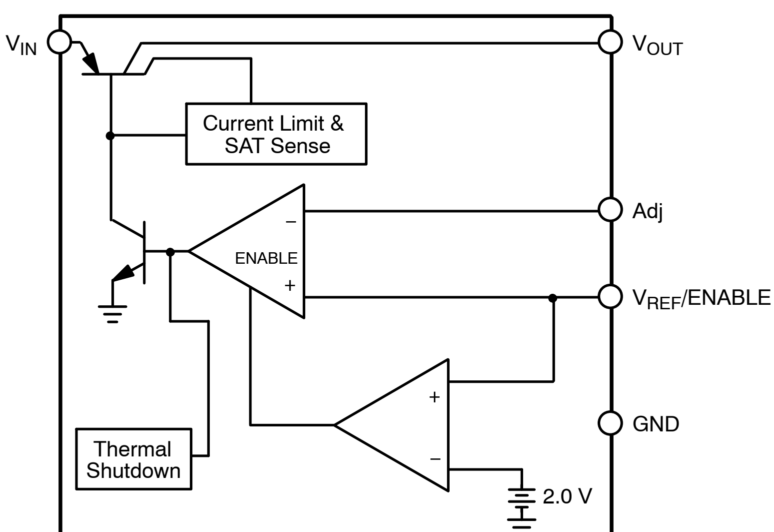

Figure 1. Block Diagram

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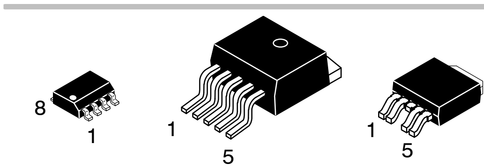
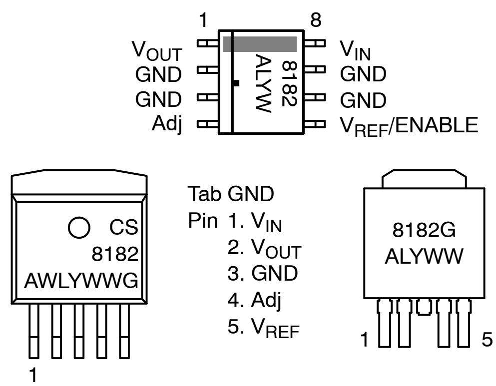


SO−8	D²PAK−5	DPAK−5
DF SUFFIX	DPS SUFFIX	DT SUFFIX
CASE 751	CASE 936AC	CASE 175AA

PIN CONNECTIONS AND MARKING DIAGRAMS



A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Device

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

October, 2019 − Rev. 28

Publication Order Number:
CS8182/D

PACKAGE PIN DESCRIPTION

Package Lead Number			Lead Symbol	Function
SO−8	D^2PAK 5−PIN	DPAK 5−PIN		
8	1	1	V_{IN}	Input Voltage
1	2	2	V_{OUT}	Regulated Output
2, 3, 6, 7	3	3	GND	Ground
4	4	4	Adj	Adjust Lead
5	5	5	V_{REF}/ENABLE	Reference Voltage and ENABLE Input

MAXIMUM RATINGS

Rating	Value	Unit
Storage Temperature Range	−65 to +150	°C
Junction Temperature	+150	°C
Supply Voltage Range (Continuous)	−16 to 45	V
Peak Transient Voltage (V_{IN} = 14 V, Load Dump Transient = 31 V)	45	V
Voltage Range (Adj, V_{OUT}, V_{REF}/ENABLE)	−10 to +V_{IN}	V
Package Thermal Resistance, SO−8: Junction−to−Case, $R_{\theta JC}$ Junction−to−Air, $R_{\theta JA}$	 25 80	 °C/W °C/W
Package Thermal Resistance, D^2PAK Junction−to−Case, $R_{\theta JC}$ Junction−to−Air, $R_{\theta JA}$	 4.0 48	 °C/W °C/W
Package Thermal Resistance, DPAK Junction−to−Case, $R_{\theta JC}$ Junction−to−Air, $R_{\theta JA}$	 8.0 64	 °C/W °C/W
ESD Capability (Human Body Model) (Machine Model)	2.0 200	kV V
Lead Temperature Soldering: (Note 1) (SO−8) (D^2PAK) (DPAK)	240 225 260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. 60 second maximum above 183°C.

RECOMMENDED OPERATING RANGES

Rating	Value	Unit
Junction Temperature, T_J	−40 to+125	°C
Input Voltage, Continuous V_{IN}	3.4 to 45	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{IN} = 14 V; V_{REF}/ENABLE > 2.75 V; −40°C < T_J < +125°C; C_{OUT} ≥ 10 μF; 0.1 Ω < $C_{OUT-ESR}$ < 1.0 Ω @ 10 kHz, unless otherwise specified.)

Parameter	Test Conditions	Min	Typ	Max	Unit
Regular Output					
V_{REF} − V_{OUT} V_{OUT} Tracking Error	4.5 V ≤ V_{IN} ≤ 26 V, 100 μA ≤ I_{OUT} ≤ 200 mA, Note 2 V_{IN} = 12 V, I_{OUT} = 30 mA, V_{REF} = 5.0 V, Note 2	−10 −5.0	– –	10 5	mV mV
Dropout Voltage (V_{IN} − V_{OUT})	I_{OUT} = 100 μA I_{OUT} = 30 mA I_{OUT} = 200 mA	– – –	100 – 350	150 500 600	mV mV mV
Line Regulation	4.5 V ≤ V_{IN} ≤ 26 V, Note 2	–	–	10	mV
Load Regulation	100 μA ≤ I_{OUT} ≤ 200 mA, Note 2	–	–	10	mV
Adj Lead Current	Loop in Regulation	–	0.2	1.0	μA
Current Limit	V_{IN} = 14 V, V_{REF} = 5.0 V, V_{OUT} = 90% of V_{REF}, Note 2	250	–	700	mA
Quiescent Current (I_{IN} − I_{OUT})	V_{IN} = 12 V, I_{OUT} = 200 mA V_{IN} = 12 V, I_{OUT} = 100 μA V_{IN} = 12 V, V_{REF}/ENABLE = 0 V	– – –	15 75 30	25 150 55	mA μA μA
Reverse Current	V_{OUT} = 5.0 V, V_{IN} = 0 V	–	0.2	1.5	mA
Ripple Rejection	f = 120 Hz, I_{OUT} = 200 mA, 4.5 V ≤ V_{IN} ≤ 26 V	60	–	–	dB
Thermal Shutdown	GBD	150	180	210	°C
V_{REF}/ENABLE					
Enable Voltage	–	0.80	2.00	2.75	V
Input Bias Current	V_{REF}/ENABLE	–	0.2	1.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. V_{OUT} connected to Adj lead.

TYPICAL CHARACTERISTICS

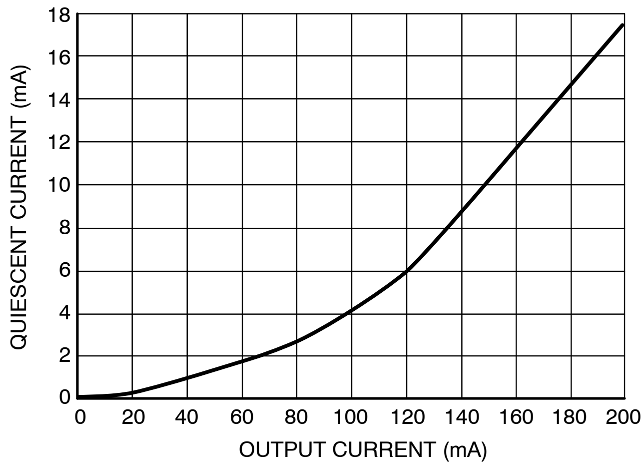


Figure 2. Quiescent Current vs. Output Current

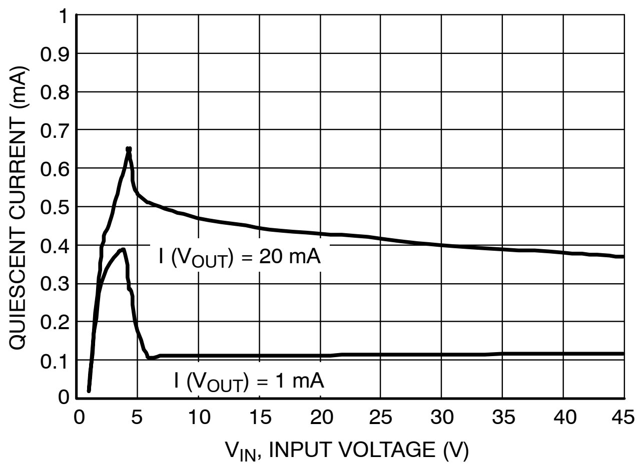


Figure 3. Quiescent Current vs. Input Voltage (Operating Mode)

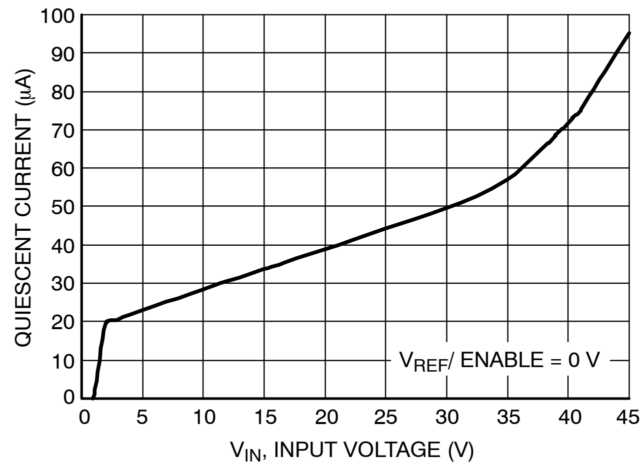


Figure 4. Quiescent Current vs. Input Voltage (Sleep Mode)

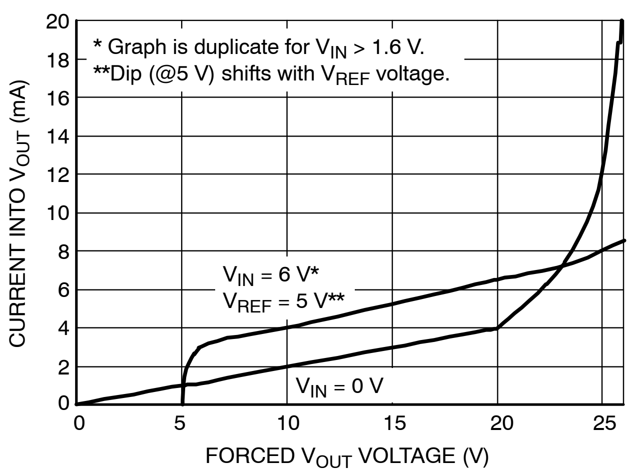


Figure 5. V_{OUT} Reverse Current

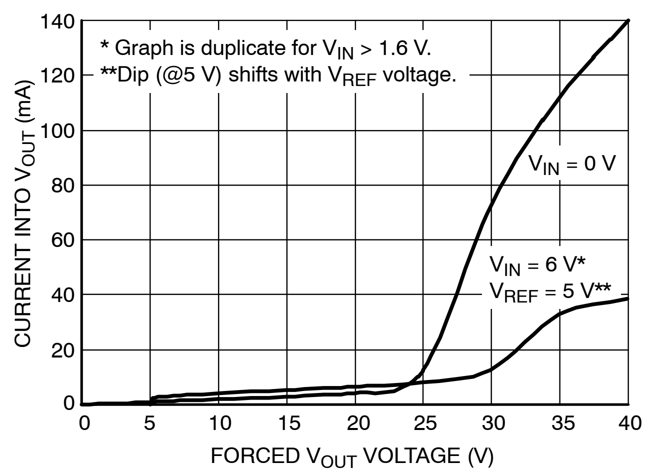


Figure 6. V_{OUT} Reverse Current

CIRCUIT DESCRIPTION

ENABLE Function

By pulling the V_{REF}/ENABLE lead below 2.0 V typically, (see Figure 10 or Figure 11), the IC is disabled and enters a sleep state where the device draws less than 55 μA from supply. When the V_{REF}/ENABLE lead is greater than 2.75 V, V_{OUT} tracks the V_{REF}/ENABLE lead normally.

Output Voltage

The output is capable of supplying 200 mA to the load while configured as a similar (Figure 7), lower (Figure 9), or higher (Figure 8) voltage as the reference lead. The Adj lead acts as the inverting terminal of the op amp and the V_{REF} lead as the non−inverting.

The device can also be configured as a high−side driver as displayed in Figure 12.

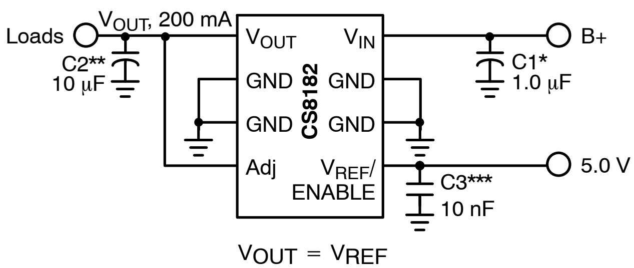


Figure 7. Tracking Regulator at the Same Voltage

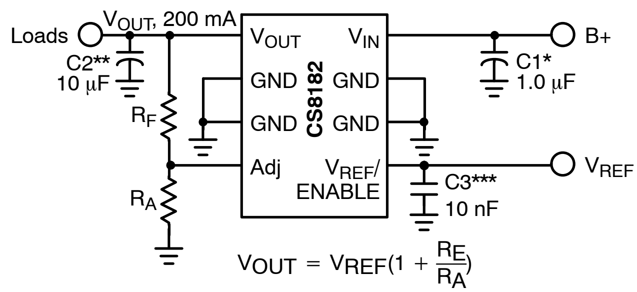


Figure 8. Tracking Regulator at Higher Voltages

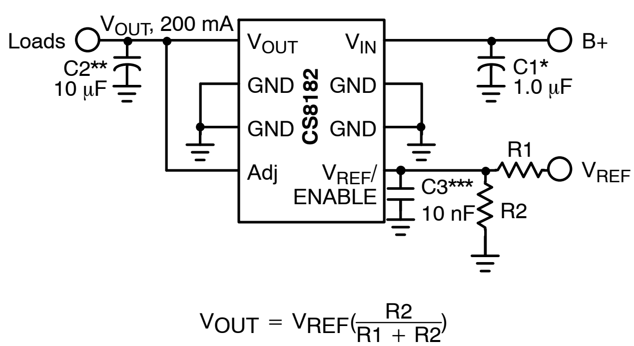


Figure 9. Tracking Regulator at Lower Voltages

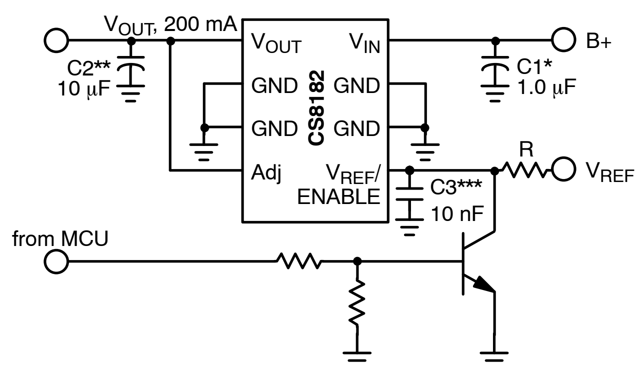


Figure 10. Tracking Regulator with ENABLE Circuit

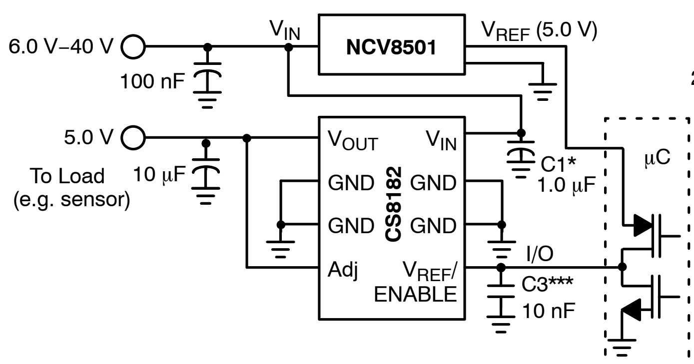


Figure 11. Alternative ENABLE Circuit

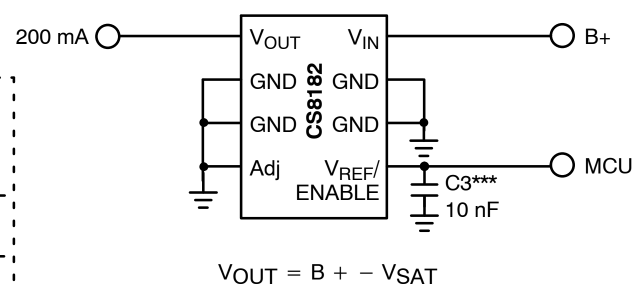


Figure 12. High−Side Driver

* C1 is required if the regulator is far from the power source filter.
** C2 is required for stability.
*** C3 is recommended for EMC susceptibility.

APPLICATION NOTES

V_{OUT} Short to Battery

The CS8182 will survive a short to battery when hooked up the conventional way as shown in Figure 13. No damage to the part will occur. The part also endures a short to battery when powered by an isolated supply at a lower voltage as in Figure 14. In this case the CS8182 supply input voltage is set at 7 V when a short to battery (14 V typical) occurs on V_{OUT} which normally runs at 5 V. The current into the device (ammeter in Figure 14) will draw additional current as displayed in Figure 15.

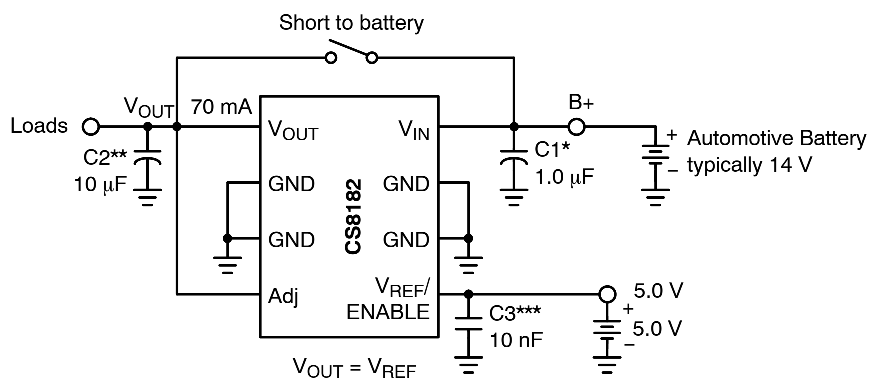
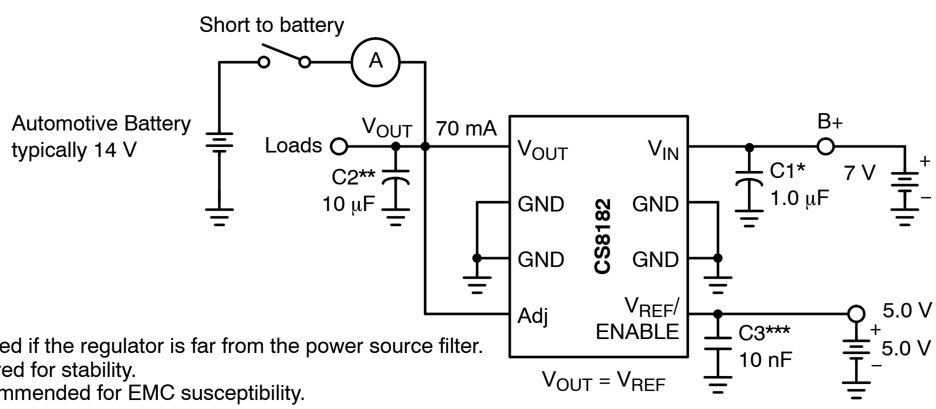


Figure 13.



* C1 is required if the regulator is far from the power source filter.
** C2 is required for stability.
*** C3 is recommended for EMC susceptibility.

Figure 14.

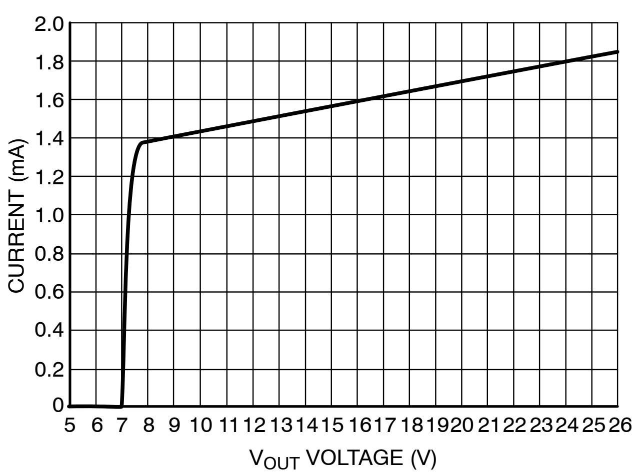


Figure 15. V_{OUT} Short to Battery

Switched Application

The CS8182 has been designed for use in systems where the reference voltage on the V_{REF}/ENABLE pin is continuously on. Typically, the current into the V_{REF}/ENABLE pin will be less than 1.0 μA when the voltage on the V_{IN} pin (usually the ignition line) has been switched out (V_{IN} can be at high impedance or at ground.) Reference Figure 16.

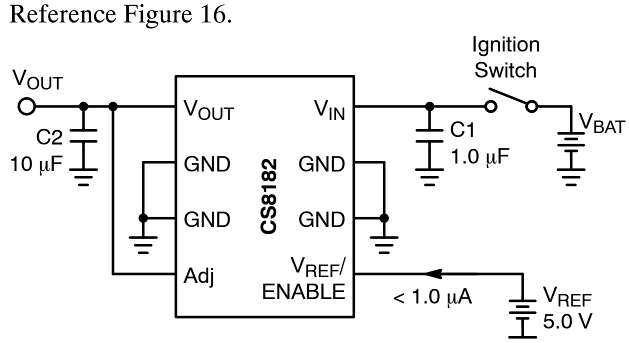


Figure 16.

External Capacitors

The output capacitor for the CS8182 is required for stability. Without it, the regulator output will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst−case is determined at the minimum ambient temperature and maximum load expected.

The output capacitor can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

The capacitor must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to −40°C, a capacitor rated at that temperature must be used.

Ceramic Capacitor Stability

The CS8182 has been verified to work with ceramic output capacitors with an additional series resistor simulating traditional ESR of tantalum capacitors; however, it has been determined the best operational performance is with a 330 mΩ series resistor (or parallel combination of three 1 Ω resistors) in conjunction with a 22 μF output capacitor. Values outside of this are known to have limited performance with respect to stability. For more information, please contact your local ON Semiconductor sales office.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 17) is:

$$P_D(max) = \{V_{IN}(max) - V_{OUT}(min)\} I_{OUT}(max) + V_{IN}(max) I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,
$V_{OUT(min)}$ is the minimum output voltage,
$I_{OUT(max)}$ is the maximum output current, for the application,and
I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of PD(max) is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required.

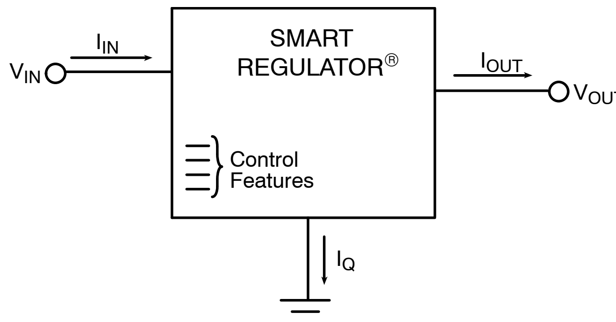


Figure 17. Single Output Regulator with Key Performance Parameters Labeled

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,
$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and
$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heatsink manufacturers.

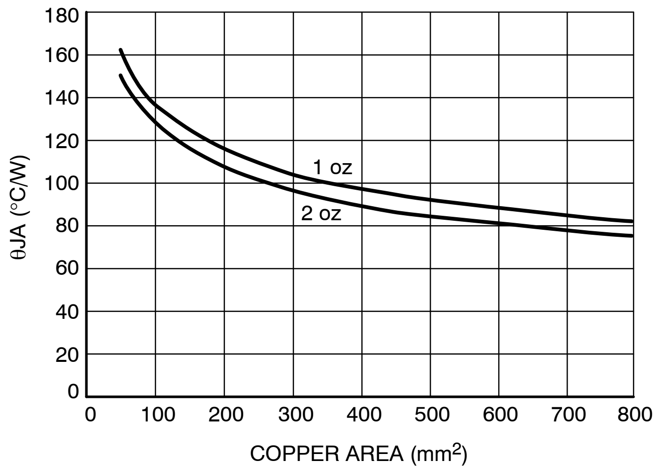


Figure 18. 8 Lead SOIC (Fused) Thermal Resistance

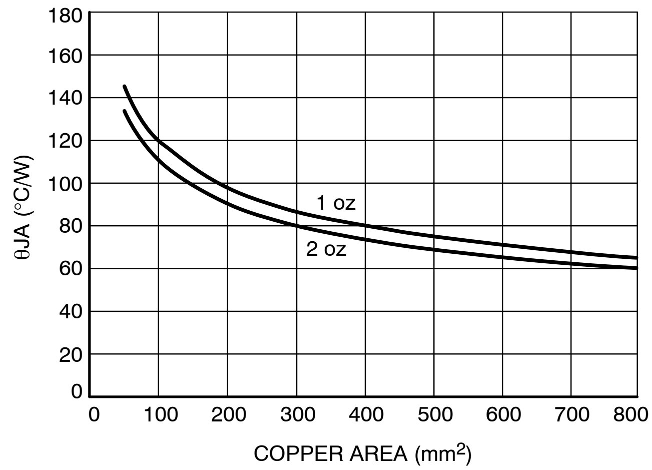


Figure 19. 5 Lead DPAK Thermal Resistance

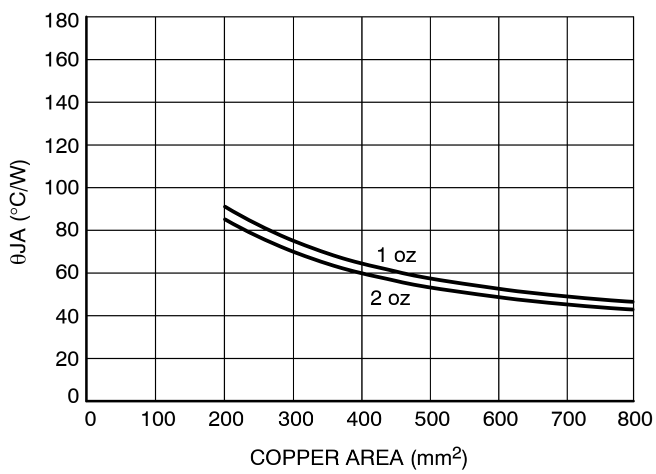


Figure 20. 5 Lead D^2PAK Thermal Resistance

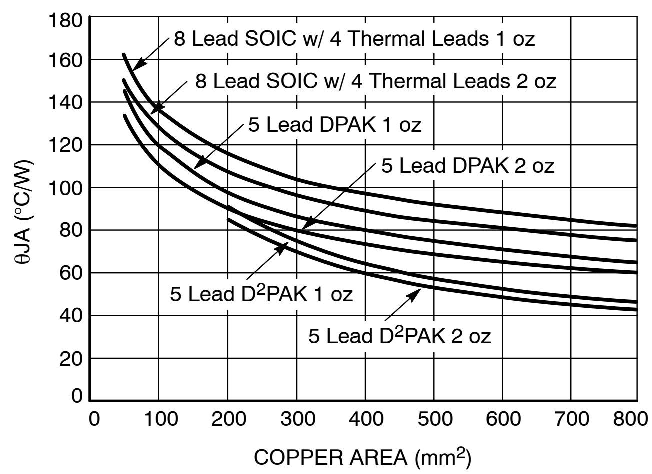


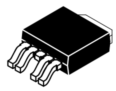
Figure 21. Thermal Resistance Summary

ORDERING INFORMATION

Device	Package	Shipping†
CS8182YDF8G	SO−8 (Pb−Free)	95 Units / Rail
CS8182YDFR8G	SO−8 (Pb−Free)	2500 / Tape & Reel
CS8182YDPS5G	D^2PAK 5−PIN (Pb−Free)	50 Units / Rail
CS8182YDPSR5G	D^2PAK 5−PIN (Pb−Free)	750 / Tape & Reel
CS8182DTG	DPAK 5L (Pb−Free)	50 Units / Rail
CS8182DTRKG	DPAK 5L (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DPAK−5, CENTER LEAD CROP
CASE 175AA
ISSUE B



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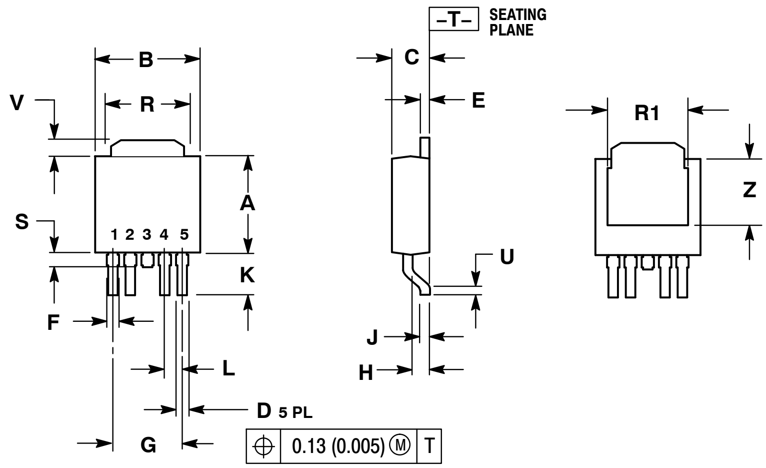
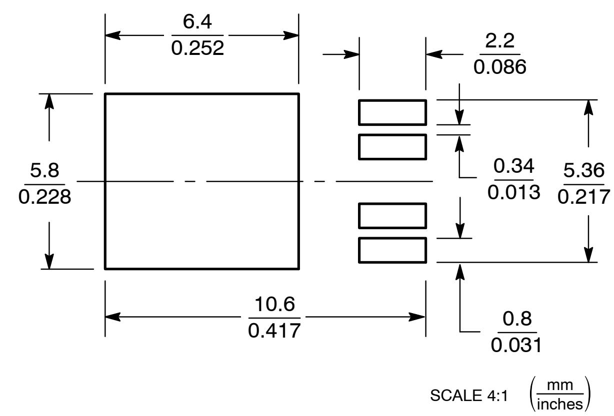


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

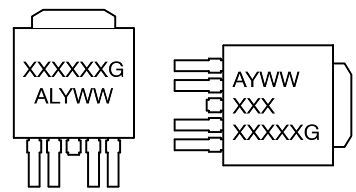
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAMS*



IC   Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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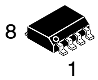
DESCRIPTION:	DPAK−5 CENTER LEAD CROP	PAGE 1 OF 1



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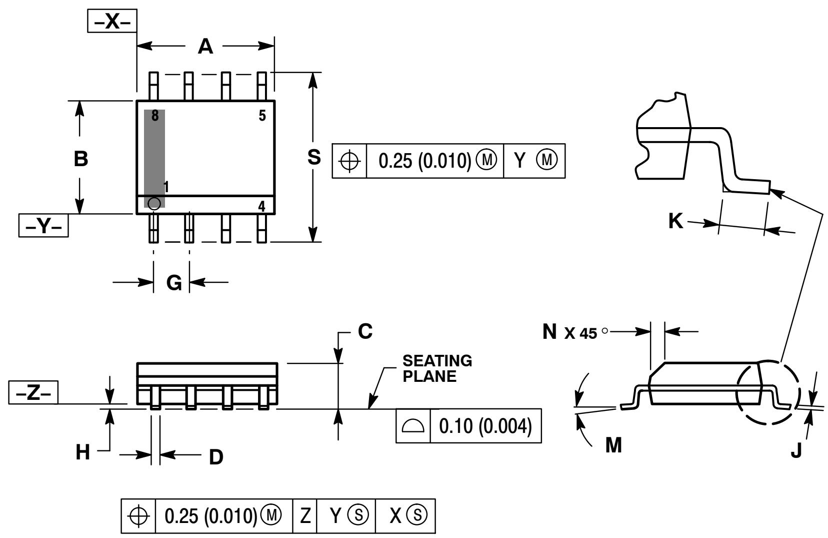
SOIC−8 NB
CASE 751−07
ISSUE AK

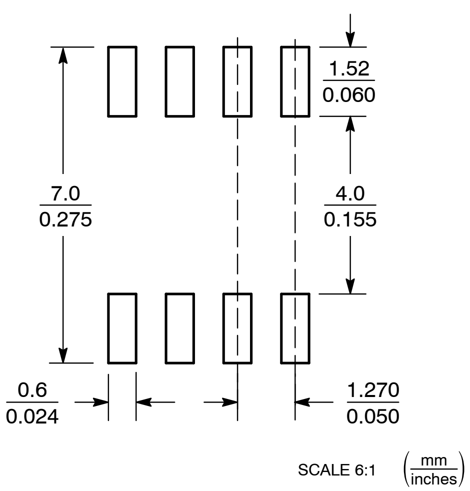
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

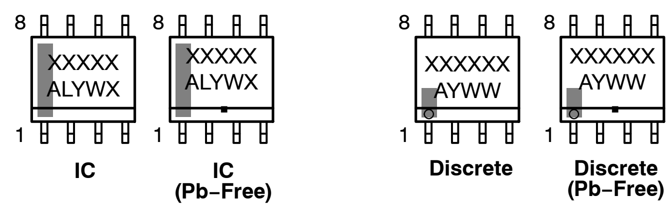
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOIC−8 NB	PAGE 1 OF 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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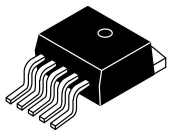
D²PAK−5
CASE 936AC−01
ISSUE A

DATE 10 SEP 2009



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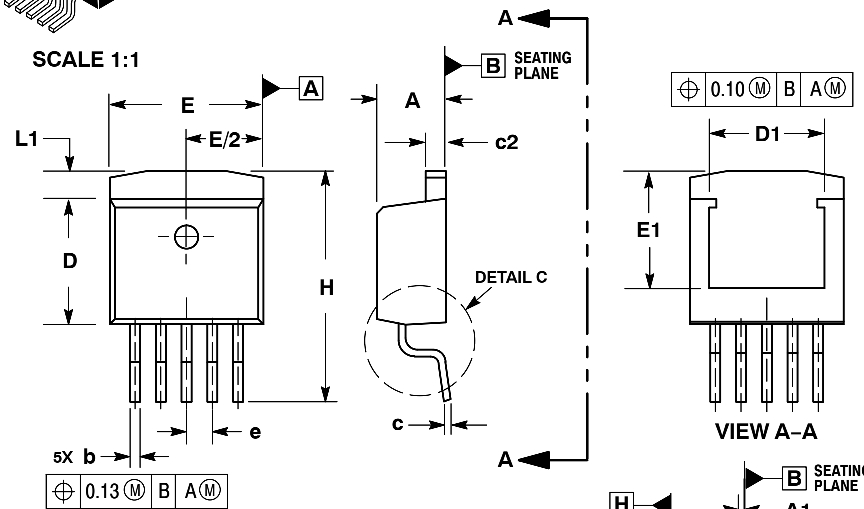
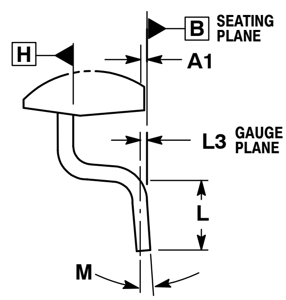


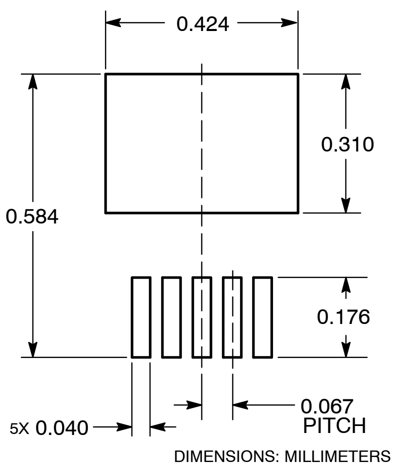


DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.005 MAXIMUM PER SIDE. THESE DIMENSIONS TO BE MEASURED AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1. DIMENSIONS D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THE THERMAL PAD.

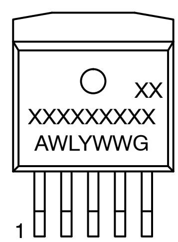
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.170	0.180	4.32	4.57
A1	0.000	0.010	0.00	0.25
b	0.026	0.036	0.66	0.91
c	0.017	0.026	0.43	0.66
c2	0.045	0.055	1.14	1.40
D	0.325	0.368	8.25	9.53
D1	0.250	---	6.35	---
E	0.380	0.420	9.65	10.67
E1	0.200	---	5.08	---
e	0.067 BSC		1.70 BSC	
H	0.580	0.620	14.73	15.75
L	0.090	0.110	2.29	2.79
L1	---	0.066	---	1.68
L3	0.010 BSC		0.25 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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